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Design and Characterization of 10 kV High Voltage 4H-SiC p-Channel IGBTs with Low V_F

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Abstract. The 10 kV silicon carbide p-channel insulated gate bipolar transistors (IGBTs) with low forward voltage drop (V_F) have been fabricated and characterized successfully. The novel edge termination structure of Four-Region Multistep Field Limiting Rings (FRM-FLRs) and the optimum JFET region design proposed in our previous work is adopted to improve the blocking performance and the on-state characteristics. The fabricated device with a chip size of 6 mm × 6 mm and an active area of 0.16 cm^2 exhibits a high blocking voltage of -10 kV with a small leakage current below -200 nA. Meanwhile, a low forward voltage drop of -8 V at the collector current of -10 A with a gate bias of -20 V is obtained at room temperature, corresponding to a current density of 62.5 A/cm^2. Besides, a lower gate leakage current is measured less than 2 nA at the gate voltage of -30 V. Experimental results demonstrate that a better trade-off between the blocking voltage and the on-state characteristics is achieved for the fabricated device, which is desirable for the high power applications.

Introduction

The increasing pursuit of the efficient power conversion for the high voltage applications like smart grid and traction has generated significant interest in the silicon carbide (SiC) devices due to its superior material properties, such as the wide bandgap, high critical electric field, and high thermal conductivity. Compared with SiC MOSFET, 4H-SiC IGBTs are considered to be favorable due to the low on-state loss because of their conductivity modulation [1]. Both p-channel and n-channel 4H-SiC IGBTs have been demonstrated with high voltage ability [2-4]. Meanwhile, the p-channel IGBTs have received much attention from some research groups due to the easier fabrication and low resistivity n-type SiC substrates [5]. In recent years, much research has been focused on achieving high blocking performance and low on-state characteristics simultaneously [6-9]. The first 5.8kV 4H-SiC planar p-IGBT was demonstrated in 2006 [10]. A 12 kV p-IGBT with the V_F of 5.3V at 100A/cm^2 was presented by Zhang *et al.* in 2008 [4]. Ryu *et al.* has reported the 20kV n-channel SiC IGBT with the on-state voltage of 6.4V in 2014 [7]. Recently, the blocking voltage of 27kV and the V_F of 11.7V at 20A has been achieved by Brunt *et al.* [9]. However, some issues should still be solved to improve the performance of SiC IGBTs, such as the low carrier lifetime, the low channel mobility, relatively high leakage current and forward voltage drop (V_F). To achieve the best device performances, many technical solutions have been made to pursue a better trade-off between the high blocking ability and low V_F [11,12].

In this paper, a domestic 10kV 4H-SiC p-channel IGBTs with low V_F is designed by using Silvaco TCAD simulation and fabricated with experimental verification. Experimental results indicate that a better trade-off between the blocking voltage and the on-state characteristics is achieved.

Design and Fabrication

Fig. 1 shows a schematic structure of the 4H-SiC p-channel IGBT. The epitaxial layers were grown on a 4-inch n-type 4H-SiC substrate with 4°off axis. The 100 μm thick p-type drift layer with a doping concentration of 4×10^{14} cm^{-3} and a 2.5 μm thick p-type buffer layer at a doping concentration of 1.5×10^{17} cm^{-3} were utilized for the device fabrication [13]. The n-type substrate served as the electron injector layer for the p-IGBTs. The n-base with a retrograde profile was formed by implantation of nitrogen (2.8×10^{13} cm^{-2}) to meet the needs of the threshold voltage and blocking voltage. The n+ contact and p+ emitter were implanted with nitrogen (4.35×10^{15} cm^{-2}) and aluminum (7×10^{14} cm^{-2}), respectively [13]. All the implants were activated at 1800 ℃ with a carbon capping on the surface to avoid the step-bunching effect [14]. The channel length was about 1 μm formed by a non-self-aligned implantation technique. A four-region multistep field limiting rings (FRM-FLRs) termination structure demonstrated in our previous work was used around the device periphery to relieve the electric field crowding and decrease the leakage current at high blocking voltage [15]. The gate oxide with a thickness of 50 nm was grown by dry thermal oxidation and then annealed in nitric oxide at 1300 ℃ to reduce the density of interface states and improve the channel carrier mobility. Polysilicon was deposited as a gate. Al/Ti contacts were deposited as the p-type ohmic metal, and Ni was deposited as the n-type collector contact metal. The fabricated IGBT has a chip size of 6 mm × 6 mm and an active area of 0.16 cm^2. Fig. 2 shows the photograph of the fabricated 4H-SiC p-IGBT wafer and the top view of a 4H-SiC p-IGBT.

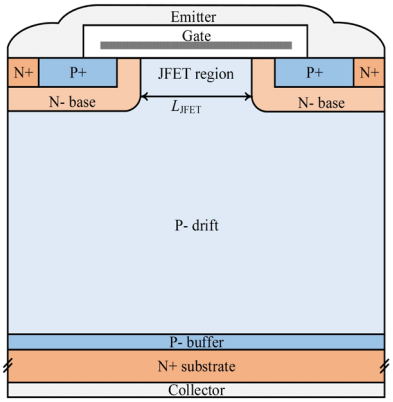
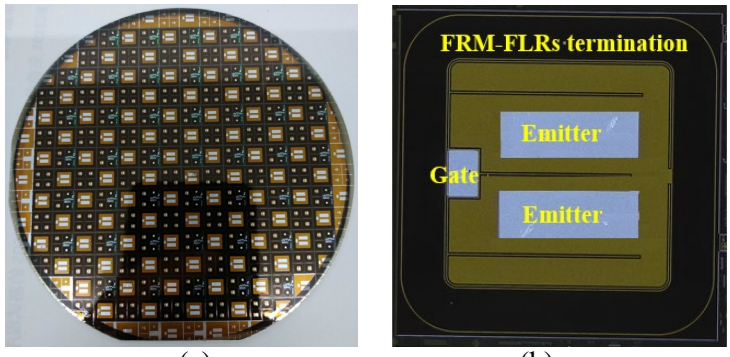


Fig. 1. Schematic structure of the 4H-SiC p-IGBT



(a) (b)

Fig. 2. Photograph of the fabricated SiC p-IGBT wafer (a) and top view of the SiC p-IGBT (b)

In order to obtain a better trade-off between breakdown voltage (BV) and V_F, the device structure is optimized by TCAD simulation based on our previous work [13]. The bandgap narrowing model, Auger recombination (AUGER) and Shockley-Read-Hall (SRH) recombination model, incomplete ionization model, doping and temperature dependent mobility models are used in the ATLAS device simulator. The material parameters of 4H-SiC used in the device simulations are presented in Table 1.

Table 1. 4H-SiC parameters used in p-IGBT simulations

Parameters	Value	Meaning
Eg300 (eV)	3.26	Band gap at 300K
Permittivity	9.8	Permittivity
Affinity	3.7	Affinity
AUGN (cm^6/s)	5×10^{-31}	Auger recombination parameter for electrons
AUGP (cm^6/s)	2×10^{-31}	Auger recombination parameter for holes
TAUN0 (s)	1.2×10^{-6}	Lifetime model parameter for electrons
TAUP0 (s)	1×10^{-7}	Lifetime model parameter for holes
Nsrhn (cm^{-3})	3×10^{17}	SRH concentration-dependent lifetime model for electron
Nsrhp (cm^{-3})	3×10^{17}	SRH concentration-dependent lifetime model for holes

The width of the JFET region (L_{JFET}) dependence of the BV and the V_F are investigated particularly. Fig. 3 shows the BV and the maximum gate oxide electric field (E_{OX}) above the JFET region with the variations of L_{JFET}. As L_{JFET} increases, the BV decreases gradually, while the E_{OX} is increasing.

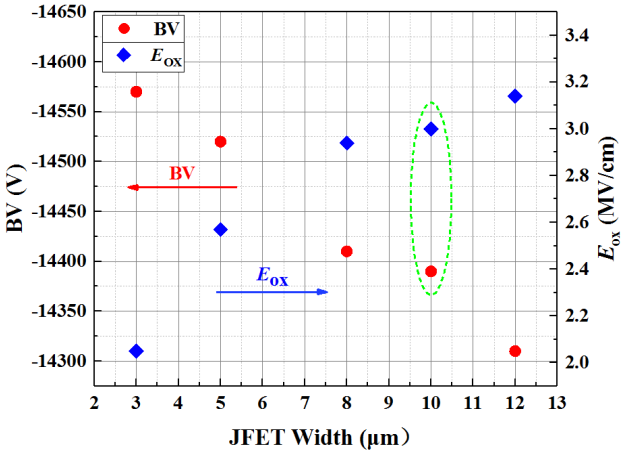


Fig. 3. Simulation results of BV and maximum E_{OX} with different L_{JFET}

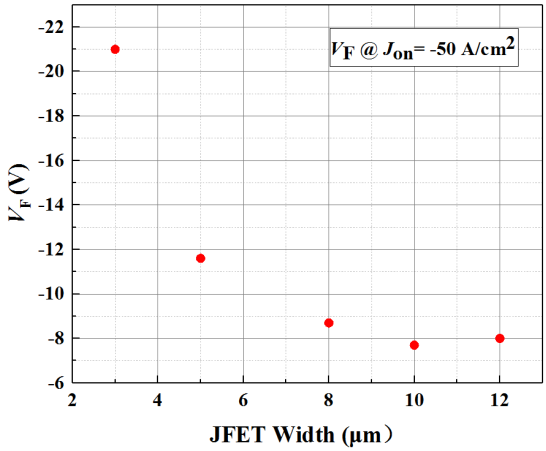


Fig. 4. Effect of L_{JFET} on the V_F at -50 A/cm^2 of current density

Fig. 4 shows the effect of L_{JFET} on the V_F at -50 A/cm^2 of current density. It can be seen that the V_F decreases gradually with the increase of L_{JFET} due to the decrease of JFET resistance. According to the simulation results, the L_{JFET} of 10 μm was adopted as the optimum structure to fabricate the 4H-SiC p-IGBT. Simulation results reveal that the BV of -14.38 kV and V_F of -7.7V at the collector current density of -50 A/cm^2 is achieved, while the E_{OX} is 3 MV/cm at the -10 kV blocking voltage, which is a widely accepted criterion for long-term gate oxide reliability [16].

Results and Discussions

Fig. 5 shows the blocking characteristics of the fabricated 4H-SiC p-IGBT at room temperature. The IGBTs were tested with the gate grounded to the emitter and the high voltage applied to the collector by using Agilent B1505A at a wafer-level chip. During the blocking characteristic measuring, the devices were immersed in Fluorinert liquid to prevent arcing in air. It can be seen that the leakage current is lower than -200 nA at -10 kV without a distinct breakdown behavior. It should be noted that a higher bias voltage (>10 kV) is limited owing to the maximum equipment ability. That means a higher blocking ability can be achieved by using the FRM-FLRs termination structure, which is illustrated in detail in our previous work [15]. As seen in Fig. 6, the FRM-FLRs edge termination is divided into four regions. Each region includes multistep field limiting rings. Therefore, the surface electric field of the FRM-FLRs is more uniform to reduce the electric field crowding around the device periphery effectively and achieve a higher blocking voltage of -16 kV shown in Fig. 7.

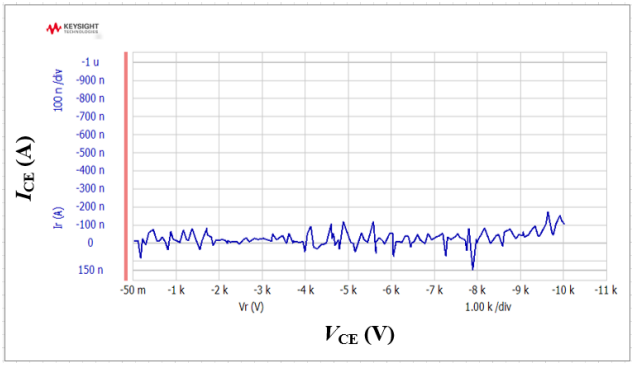


Fig. 5. Blocking characteristics of the 4H-SiC p-IGBT at 25 ℃

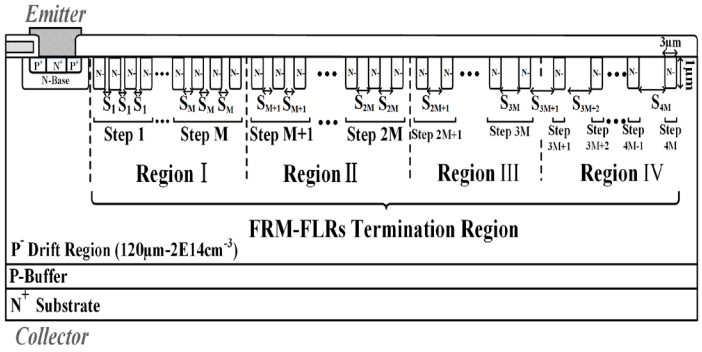


Fig. 6. Schematic cross-section of FRM-FLRs applied in 4H-SiC IGBT [15]

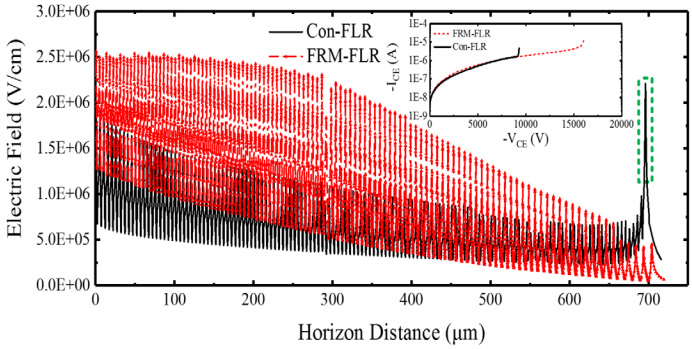


Fig. 7. Comparison of electric field distribution and blocking characteristics for FRM-FLRs and Con-FLRs [15]

Fig. 8 shows the experimental and simulated forward I-V characteristics of the p-IGBT with a negative gate bias at room temperature. It can be seen that the I-V characteristic of simulation indicates a good fitting effect with the result from the experiment. The measured V_F is -8 V at a collector current (I_C) of -10 A with a gate bias of -20 V, corresponding to a current density of 62.5 A/cm^2. The on-state current density (J_{ON}) characteristics are also shown in Fig. 8. Experimental results prove that the fabricated p-IGBT has the V_F of -7.1 V at J_{ON} of -50 A/cm^2 with a gate bias of -20 V.

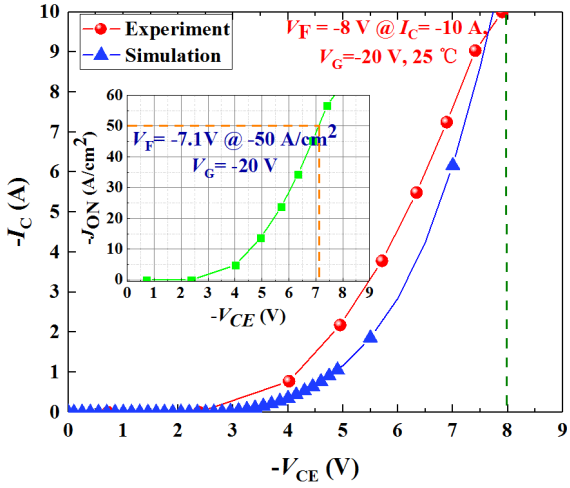


Fig. 8. On-state I-V characteristics of the fabricated p-IGBTs

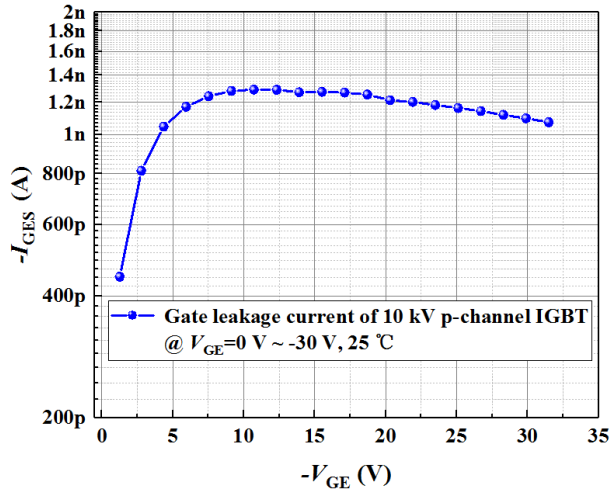


Fig. 9. Experiment result of I_{GES} under V_{GES} pressure

Fig. 9 shows the gate leakage current characteristics of the fabricated device at the gate-emitter voltage testing, which is important to evaluate the gate oxide reliability. It can be seen that the gate leakage current of a p-IGBT is lower than -2 nA at the gate bias voltage from 0 to -30 V, which meets the reliability requirement for the actual application.

Conclusion

A 4H-SiC p-channel IGBT with 10 kV blocking voltage and low V_F has been designed, fabricated and characterized in this paper. The device with a chip size of 6 mm × 6 mm and an active area of 0.16 cm^2 shows that the blocking voltage is -10 kV with a small collector leakage current, which is attributed to the FRM-FLRs termination structure design given by our previous work. Moreover, the V_F of -8 V is achieved at I_C= -10 A and V_{GS} = -20V, indicating a current density of 62.5 A/cm^2. The measured gate leakage current of lower than -2 nA at V_{GS} = -30V is reliable for the actual application. Most importantly, the better trade-off characteristics of the fabricated p-IGBTs are acquired, which is desirable for use in high power electric systems.

Acknowledgments

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