

Experimental Investigation of a 10 kV-70A Switch with Six SiC-MOSFETs in a Series-Connection Configuration

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Abstract. In this paper, a prototype of 6 series-connected SiC-MOSFETs for double pulses test purpose is presented. This prototype represents many challenges amongst which the measurements of voltage sharing and the EMI issues due to high dv/dt . High voltage tests are performed up to 8 kV at 65A and voltage balancing, losses and switching speeds are evaluated. Switching speed up to 520 V/ns are recorded.

Introduction

In the context of the development of converters in the range of mega-Watt for grid applications with voltage ratings up to tens of kV, SiC-MOSFETs are considered as a promising option. Series-connection of MOSFETs has similar conduction resistance at on-state compared to single High-Voltage MOSFET for the same breakdown voltage and the same active chip area [1]. Switching performances are expected to be high. Unfortunately, some solutions applied to reach accurate voltage balancing decrease the switching speeds. Switching performances remain highly better than high-voltage Si-IGBT allowing switching frequency up to hundreds of kHz.

To reach a breakdown voltage of 10kV, 6 SiC-MOSFETs (1.7 kV 45mΩ from Wolfspeed) are connected in series. These MOSFETs have a breakdown voltage above 2.2 kV allowing to safely work at 8 kV with 6 MOSFETs. In order to evaluate performances of series-connected SiC-MOSFET with the simplest and reliable drain-source voltage balancing, a prototype is developed with passive snubbers. The focus is made on voltage balancing, gate-drivers supplies and measurement issues. This prototype is designed for 10 kV and tests are performed up to 8 kV. Fast switching speeds are obtained as expected with SiC-MOSFET devices leading to significant common mode current through insulation barriers and measurement equipment.

Voltage Balancing

Snubber circuits. Snubber circuits (Fig. 1) are commonly used to optimize switching trajectory and damp the voltage and current ringing but also to balance voltage across devices connected in series. Snubbers are simple, robust, cheap and simple to implement. In some cases, it is relevant to use a resistor-capacitor-diode (RCD) snubber to charge the capacitor through the diode reducing losses in the resistor at turn-off and then discharging the capacitor at turn-on into the resistor. RCD snubber allows dynamic voltage balancing of series-connected switches since it creates a capacitor voltage divider bridge. Static voltage balancing is then obtained thanks to parallel connected resistors that compose a voltage divider.

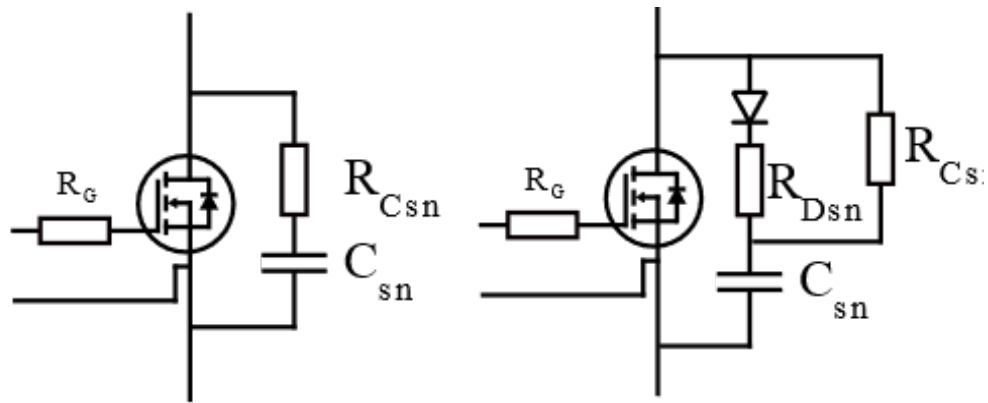


Fig. 1: RC snubber and RCD snubber

Selection of C_{sn} capacitance is different depending on the snubber objective. If the objective is to damp overvoltage then C_{sn} values is selected to be large enough to store the energy of the stray inductance [2]. Otherwise, if the goal is to balance voltages, the capacitor value is usually selected to be 5-10 times larger than output capacitance value at high voltage of the switching devices [3].

Prototype. The series-connection of MOSFETs is built on a PCB that allows fast and cheap manufacturing. MOSFETs and snubber diodes are soldered as surface mounted components by bending pins in this way there is no holes breaking epoxy isolation. Regarding gate-driver circuits, push-pulls with gate resistors are placed as close as possible to MOSFETs on the same PCB. Gate driver power supplies need high voltage insulation. Bespoke 15kV insulated flyback (with 9pF of isolation capacitance) are used to supply multiple gate drivers as described on Fig. 2. Each gate driver has small commercial isolated DC-DC converter. Gate signals are insulated thanks to Plastic Optical Fiber (POF). Gate-driver signals can be manually synchronized with nanosecond precision on the optical fiber emitter board that has been specifically designed.

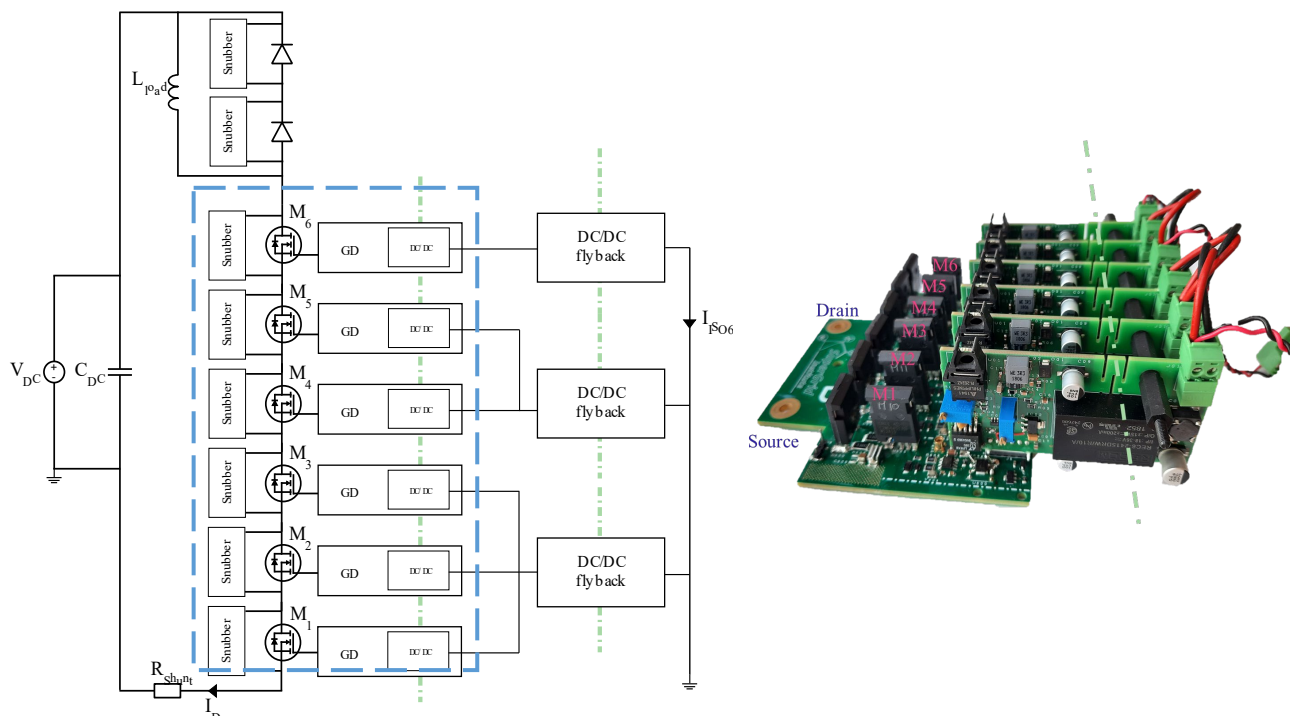


Fig. 2 : Series connected MOSFETs with gate-driver supplies in a double pulse test bench.

Double pulse test. The test bench is designed to perform short circuit and double pulse tests up to 10kV. The modularity of this platform means that the stray inductance is not optimized. Total loop inductance is estimated at 400 nH. The half-bridge is built with one or two SiC 10 kV PiN diodes from SuperGrid Institute [4] (used for freewheeling) on high side and the series connected MOSFETs on low-side. The load is a bespoke air-inductor with a value of 1mH.

Measurement. Current measurement is performed with a 25mΩ shunt resistor. Middle point voltage measurement is measured thanks to high-voltage passive probes P6015A (Tektronix) that have a 75 MHz bandwidth. However, these passive probes cannot be used to measure drain-source voltages sharing since they impact voltage balancing. Parasitic elements have a significant impact on switching behaviors [5] with high switching speed. Connected probes add small capacitance and common mode current path that impact deeply voltage balancing for this high switching speed applications.

One promising solution that is highlighted here is to use insulated differential probes. Such probes have no impedance between probe head and the oscilloscope because of the optical fiber isolation. Some parasites can remain by proximity of the probe head with the circuit. Measurement with high common mode voltage and dv/dt can be done in a non-intrusive way. The used probe is the *IsoVu* differential probe by Tektronix with the reference TIVP02 (200 MHz bandwidth, ± 2500 V differential voltage and ± 60 kV common mode voltage).

Switching Performances

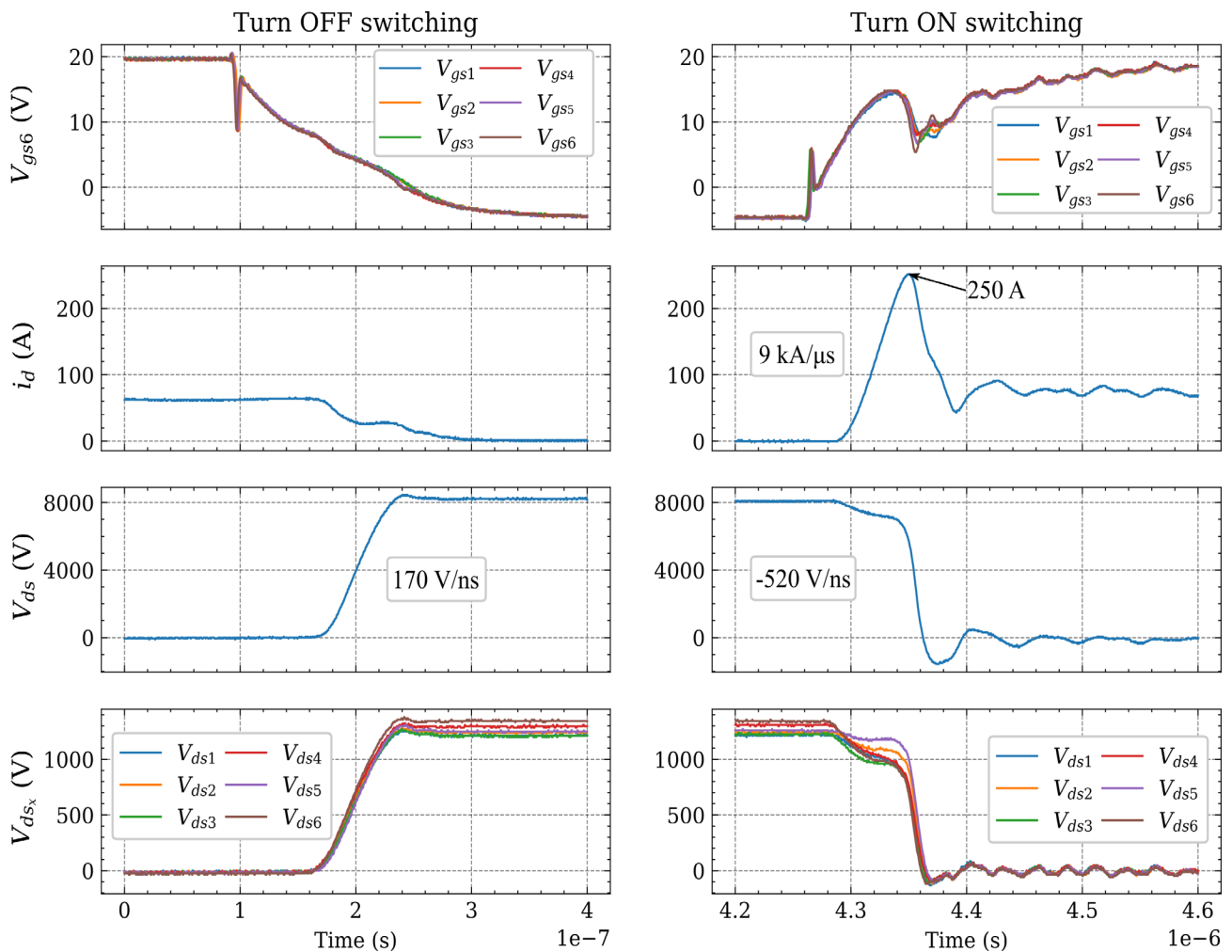


Fig. 3 : Switching waveforms measurement at 8kV and 65A.

Balancing. Thanks to these measurements, the voltage balancing can be quantified. Voltage balancing percentage is defined as follows:

$$Unbal_n(\%) = \frac{V_{dsOFFn} - \frac{V_{DC}}{N}}{\frac{V_{DC}}{N}} \cdot 100 \quad (1)$$

Where $Unbal_n(\%)$ is the balancing at off state of the n^{th} MOSFET. The most unbalanced MOSFET has the highest unbalancing percentage. Measurements of Fig. 3 show a maximum unbalancing percentage under 10%. The main voltage unbalance cause is parasitic capacitances though gate drivers supply insulation, other causes are minimized since components are selected, components are not heating and gate driver signals are synchronized.

Losses. An estimation of losses is made by post-processing of the voltage v_{ds} and current i_d . To get accurate results, delays between i_d and v_{ds} are compensated. At turn-off, the measured energy is $E_{OFF} = 13.5\text{mJ}$. This energy is mainly due to snubber capacitors charging. With 2.2nF for each MOSFET, capacitance energy is:

$$E_{Csn} = N \frac{1}{2} C * V_{dsOFF}^2 = \frac{6}{2} 2.2 \cdot 10^{-9} \cdot \left(\frac{8000}{6}\right)^2 = 11.7 \text{ mJ} \quad (2)$$

The remaining 1.8mJ is lost in the snubber resistor and the MOSFET itself. It could be optimized by reducing the value of R_{dsn} . E_{Csn} energy is dissipated at on-state.

Measured turn-on energy is $E_{ON} = 62.5 \text{ mJ}$. Turn-on loss is then: $E_{lossON} = E_{ON} + E_{Csn} = 74.2 \text{ mJ}$. E_{ON} value is mainly explained by the important recovery current of the diode.

Switching speed. With $I_D = 65\text{A}$ at turn-off switching, voltage rising slope reach 170 V/ns which is well limited by snubber circuit. Contrary to turn-on switching, falling speed is not limited by snubber: voltage speed reaches 520 V/ns . At this speed, a significant common mode current passes through the insulation barrier and can potentially damage driver circuits. It could also have functional impact on gate driver circuit and they must be designed with a strong EMI immunity.

Conclusion

A prototype of 6 series connected SiC-MOSFETs is designed, built and tested in double test up to a bus voltage of 8kV . It represents a challenge on multiples aspects: voltage balancing, dielectric consideration, EMC immunity and measurements. Thanks to isolated differential voltage probes, it is possible to measure V_{ds} of each MOSFETs in a non-intrusive manner. Balancing percentage is maintained under 10%, meaning that MOSFETs work in safe voltage condition with high switching speed up to 170V/ns at turn-off and 520V/ns at turn-on. Nevertheless, high switching speed represents an EMC risk. Electronic circuits must be designed with low parasitic capacitances (for insulation barriers) and strong EMI immunity and if not enough, switching speed must be slowed down, which unfortunately results in an increase of switching losses. Then snubber values can be optimized to get the best compromise between voltage balancing and switching losses. For this purpose, an optimization tool is under development to optimize the values of components of the snubber circuits based on accurate model of SiC-MOSFET and stray capacitances of the system.

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