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Comparison of the H3TRB Performance of Silicon and Silicon Carbide Power Modules

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Abstract. In this work, the H^{3}TRB performance of power modules with SiC MOSFET chips is investigated and compared to their silicon counterparts with similar electrical ratings. For this purpose, SiC MOSFETs and silicon IGBT chips are packaged in the same housing and with the same packaging technology and an H^{3}TRB test is performed on both types of test devices. The results show that while both types exhibit an excellent H^{3}TRB performance, the SiC MOSFETs had a significantly longer time to failure but also a wider failure distribution. Hence, the investigations presented in this paper confirm that properly designed SiC devices feature an equal or even better ruggedness against electro-chemical stress than standard silicon devics and are equally suitable for applications, which require operation in harsh environments.

Introduction

The robustness of power devices against electro-chemical stress is an important qualification criterion, particularly for applications such as wind power or traction, in which the power devices are exposed to harsh environmental conditions [1, 2, 3]. The standard test to evaluate the reliability under harsh environmental stress is the High Humidity High Temperature Reverse Bias (H^{3}TRB) test. During this test, the device is stored in a climate chamber at elevated temperature and humidity with a reverse voltage applied. The test is a common qualification test and test conditions are similarly defined by several standards (e.g. IEC 60749-5 [4]) with a relative humidity of 85 % and an ambient temperature of 85 °C. While the reverse bias is not specifically defined, a high reverse voltage was shown to be more stressful and hence, is commonly chosen in the range of 60 % to 80 % of the devices' nominal voltage [5]. So far, there are several reports on the H^{3}TRB performance of SiC devices, which show excellent results. The good performance however, leads to very long run times and therefore, most of those tests are not performed until end of life (EoL) but are terminated after a certain time, or the test is strongly accelerated by applying an even enhanced stress level [6, 7, 8]. On the other hand, in order to estimate the service life of SiC devices under thermo-mechanical stress and draw a comparison to their silicon counterparts, it is necessary to perform the tests until a sufficient amount of devices failed and a convincing failure statistics can be derived. In this work, the difference in robustness against electro-chemical stress of silicon and SiC power devices is investigated by means of H^{3}TRB testing of comparable Si IGBTs and SiC MOSFETs in identical packages.

Device Under Test

As devices under test (DUTs), Si IGBTs and SiC MOSFETs with the same voltage rating of 1200 V and current rating of 25 A were used. Both chips were packaged in identical packages, a baseplateless module with soldered chips, DCB substrate and silicone gel as filler material. A total of 5 modules with silicon IGBTs and 16 modules with SiC MOSFET chips were considered. Some of the SiC MOSFETs modules were exposed to some degree of thermo-mechanical stress prior to H^{3}TRB testing. However,

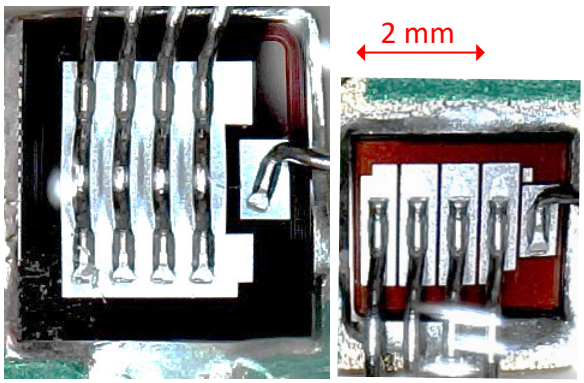


Fig. 1: Comparison of the chip size of the tested silicon IGBT and SiC MOSFET chips

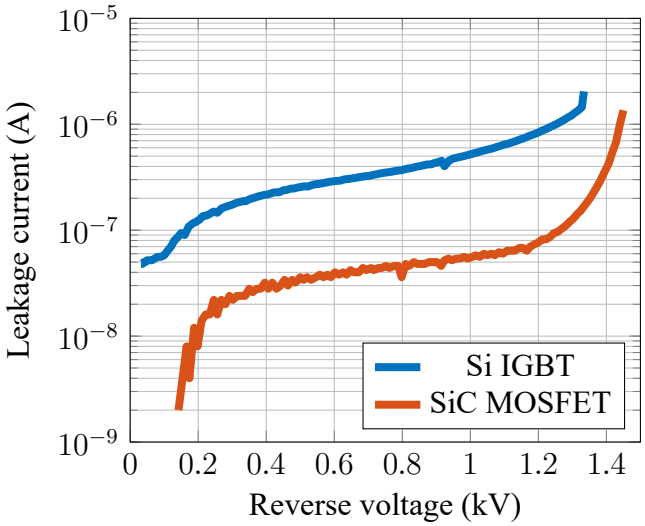


Fig. 2: Comparison of the blocking characteristics of one typical silicon IGBT and SiC MOSFET chip, respectively

the failure statistics did not indicate any impact on the H^{3}TRB lifetime, which is consistent with previously reported results for Si devices [9]. Hence, all SiC devices are treated as a single test batch. The devices with the silicon IGBTs are commercially available (SKiiP 13AC12T4V1), and the SiC MOSFET modules are engineering samples, but were manufactured with the same packaging technology. An image of both chips is shown in fig. 1. It is visible that the SiC MOSFET chip is significantly smaller, and even though both devices have comparable electrical ratings, the area of the SiC MOSFETs is only approximately 50 % of the silicon IGBT, which shows the general advantages of SiC as a semiconductor material in comparison to silicon. The blocking characteristics of both device types are shown in comparison in fig. 2. The SiC MOSFETs exhibit a significantly lower leakage current and slightly higher avalanche voltage compared to the Si IGBTs. While the former is a result of the low intrinsic carrier concentration and hence, a material related property, the higher avalanche voltage is likely a result of a more conservative junction termination design, owed to the less mature manufacturing processes for SiC semiconductors.

Test Conditions

To assess the DUTs ruggedness against electro-chemical stress an H^{3}TRB test was performed on both types. The tests conditions were identical for both device types with a relative humidity of 85 %, an ambient temperature of 85 °C and a test voltage of 960 V, which corresponds to 80 % of the devices' nominal blocking voltage. During the test, the leakage current of the devices was monitored and as a failure criterion an increase in leakage current of one order of magnitude was considered. Intermediate measurements (IM) of the blocking characteristics were performed at room temperature every 500 h. Prior to those measurements, the DUTs had been dried at 10 % relative humidity and 50 °C ambient temperature for 24 h. After the measurements, the environmental test conditions temperature and humidity were applied and settled for 24 h before the test was resumed by reapplying the test voltage.

Test Results

This work focus on a detailed discussion of the test performed on the SiC MOSFETs and the results of the Si IGBTs are used as a reference. A detailed report on the H^{3}TRB test on the Si IGBTs is given in [9].

The leakage current of the SiC MOSFETs at room temperature at 1200 V over the course of the IMs is shown in fig. 3. The characteristics indicate a general trend of the devices to a slight increase in leakage current with more accumulated time under H^3TRB stress. While the leakage current logging is quite consistent for almost all DUTs, one DUT (solid yellow line in fig. 3) showed a peculiar characteristics with a generally higher leakage current and more variability.

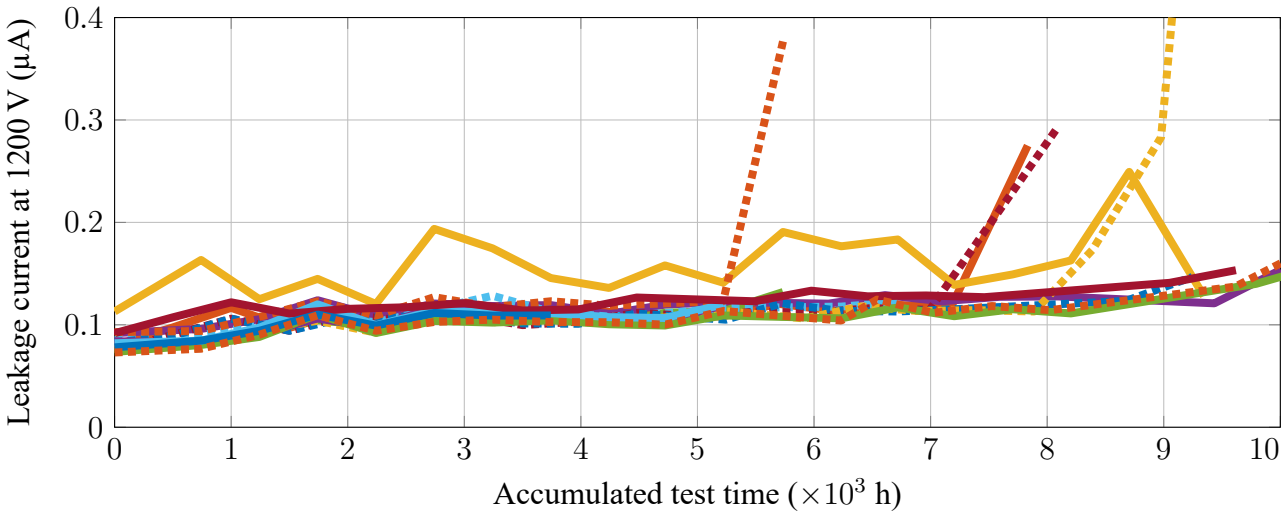


Fig. 3: Characteristics of the leakage current of the SiC MOSFETs at 1200 V initially, and for all intermediate measurements, taken every 500 h over the course of the H^3TRB test

During 10 000 h of testing, only 11 out of 16 SiC MOSFETs failed. The measurement of the blocking characteristics at room temperature revealed differences among the failed DUTs. The blocking characteristics of three of the failed SiC MOSFETs initially and after EoL, shown in fig. 4, represent the different changes in blocking characteristics occurred during the test. All failed devices exhibit an increase in leakage current towards their EoL. Some of the failed devices exhibit virtually no remaining blocking capability (blue curve in fig. 4), while for other devices the blocking capability was significantly reduced (orange curve in fig. 4). In contrast, some devices still maintained their full blocking capability at room temperature even after device failure (yellow line) but exhibited a significant increase in leakage current.

The propagating degradation of the DUTs also impacted their leakage current characteristics during re-initialization of the test after the intermediate measurements. The initialization characteristics of one DUT is shown in fig. 5. Before the test initialization the climate conditions were settled for 24 h. During the initialization the voltage is increased from 0 V to the test voltage of 960 V with 25 V s^{-1}. The characteristics at the beginning of the test (blue line in fig. 5) show a stable leakage current level as soon as the test voltage was reached. After 5200 h of cumulative H^3TRB stress, The DUT exhibited a small overshoot (orange line) and the leakage current stabilized after some time to a slightly elevated leakage current level. After 7800 h of cumulative H^3TRB stress the overshoot is even more pronounced and a further increase in steady-state leakage current level can be observed (yellow line). This behavior can be an indicator of a local degradation, which increases leakage current initially but is self-limiting due to heat generation.

Failure Analysis

In order to investigate the failure mechanisms, some of the failed devices were decapsulated and visually inspected with an optical microscope. The images, shown in fig. 6 revealed different degradation patterns. Fig. 6a shows dendrite growth with two dendrites reaching from the unprotected part of the

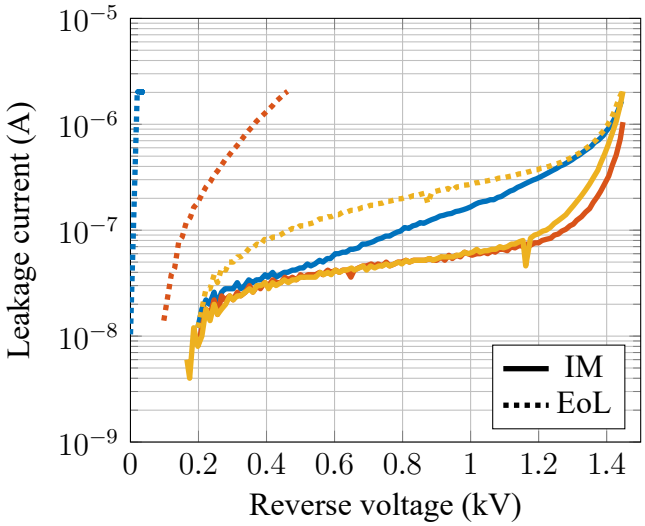


Fig. 4: Blocking characteristics before and after H^3TRB for three of the failed SiC MOSFETs

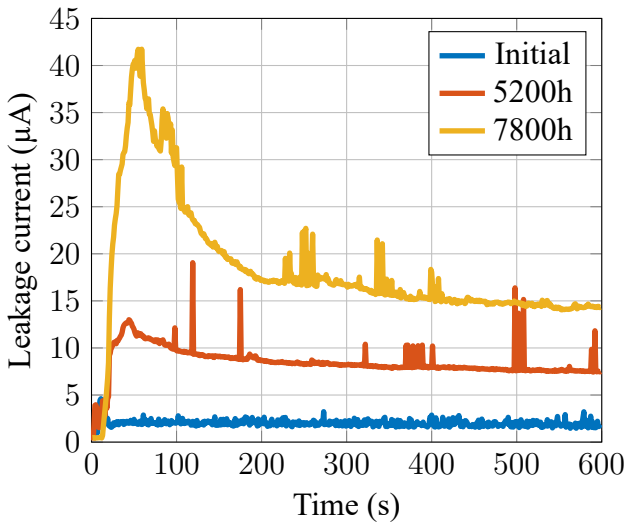
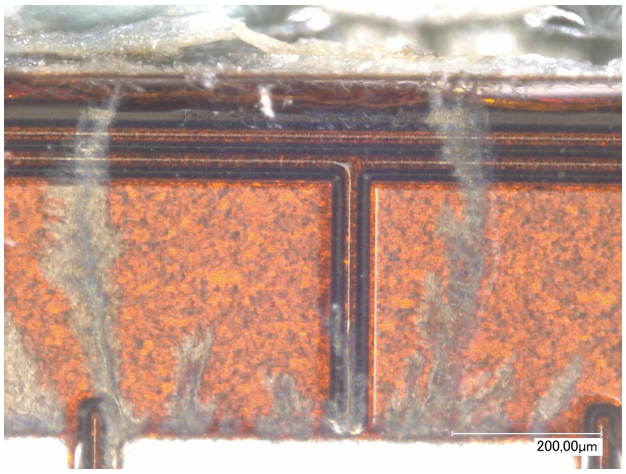
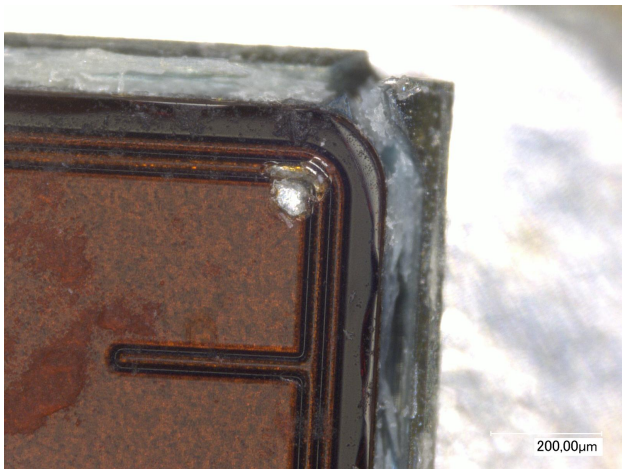


Fig. 5: Characteristics of the DUTs upon test resumption after the intermediate measurements



(a) Two silver dendrites reaching from the unprotected metallization to the edge of the chip



(b) Degradation of the passivation at the corner of the chip

Fig. 6: Microscope images of part of the junction termination of two selected chips after the test

top side metallization to outer edge of the chip. Further EDX analysis revealed that the dendrites are composed of silver and grew on top of the polyimide passivation layer. Silver dendrites are a well-known degradation mechanism and are a classical cause of failure for silicon power semiconductors as well [10]. In fig. 6b a damage of the polyimide coating at the corner of the chip is visible. While the chip with the dendrite showed effectively no remaining blocking capability after EoL, the chip with the damaged polyimide maintained its blocking capability but exhibited an increase in leakage current. This can indicate there might be a correlation between failure mode and failure pattern. However, the data set it not sufficient and further investigations are necessary before a final conclusion can be drawn.

Statistical Analysis

In order to compare the failure times of the tested SiC MOSFETs with the silicon IGBTs, the Weibull statistics of both tests are considered. The Weibull distribution of the time to failure during H^3TRB

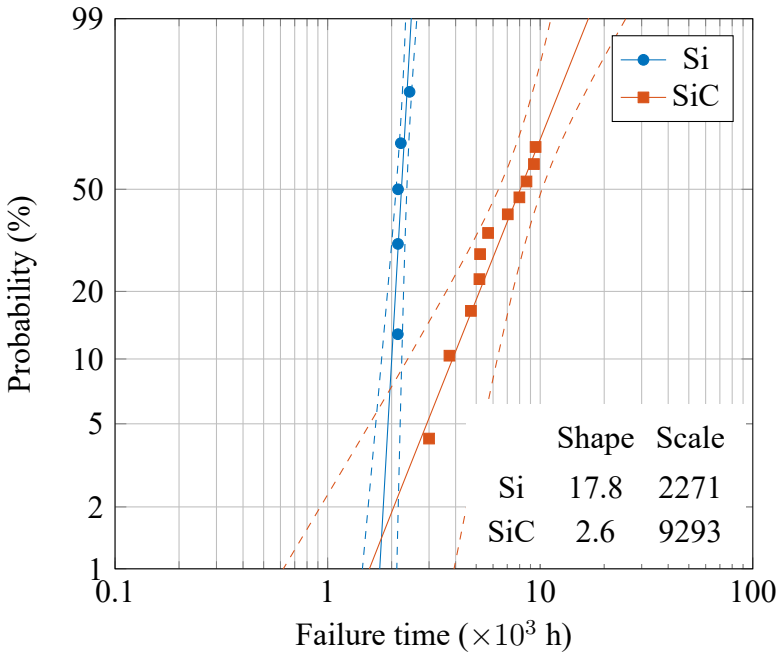


Fig. 7: Weibull plot of the H³TRB results of both test splits. The dashed lines indicate the confidence interval of 95 %.

for the Si IGBTs and the SiC MOSFETs is shown in fig. 7. The Weibull shape factor is significantly higher for the silicon IGBTs is due to a narrower failure distribution. This can be a result of the more mature processing technology of silicon devices, which results in smaller manufacturing tolerances and hence, more homogeneous device characteristics. In contrast, the Weibull scale factor, indicating the time, at which 63.2 % of the test population has failed, is by a factor of around 4 higher for the SiC MOSFETs, indicating a higher robustness of the SiC devices against electro-chemical stress. While none of the silicon IGBTs survived more than 2500 h during the reference test, all tested SiC devices survived more than 3000 h of cumulative H³TRB stress.

Summary and Conclusion

In this work, the difference in robustness against electro-chemical stress of silicon and SiC power semiconductors is investigated by performing H³TRB tests on comparable silicon IGBT and SiC MOSFET chips in identical packages. The results of this work show, that while both device types exhibit an excellent H³TRB performance far beyond the typical qualification criterion of 1000 h under the applied test conditions, the SiC MOSFET clearly surpassed the Si IGBTs with respect to the time to failure during the test. The significantly better H³TRB performance of the SiC MOSFETs is consistent with other investigations [2], but counter intuitive due to the smaller junction termination (JT) of the SiC MOSFETs and the much higher electric fields. However, the module with silicon IGBTs is a commercially available product, which had been on the market for some time and hence, does not utilize the most recent silicon IGBT generation. In contrast the tested SiC MOSFETs featuring a state-of-the-art design. Recent results on next generation Si devices [11, 12] indicate that standard JT of Si IGBTs are prone to electro-chemical degradation and that the next generation of the JT offer an order of magnitude better performance – which would then also fit intuition. Hence, the difference in H³TRB cannot necessarily be attributed to the semiconductor properties but is likely a result of the advanced JT design of state-of-the-art power electronic devices. In any case, the results of this work clearly show that SiC power devices can be designed to exhibit excellent ruggedness against electro-chemical stress and are well-suited for applications, which require operation in harsh environments.

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