Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 493-497
doi:10.4028/p-ztr5d7
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Submitted: 2021-10-13
Revised: 2022-02-22
Accepted: 2022-03-17
Online: 2022-05-31

Investigation of SiC Thyristors with Varying Amplifying Gate Design

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Keywords: Thyristor, Amplifying gate, Device fabrication, Etched JTE, Turn-on characteristic, On-state characteristic.

Abstract. This paper presents experimental 1.2 kV, 10 A SiC thyristors with different amplifying gate design. In contrast to comparative devices (with simple gate) the amplifying gate thyristors show a characteristic snap-back and a higher gate current to trigger. Their gate-anode I-V characteristics comply with the underlying design constraint, regarding the resistances of pilot and main thyristor: $R_P > R_M$. Moreover, the turn-on waveforms of well-designed amplifying gate thyristors reveal peak-shaped inversions in the gate current and voltage transients, providing clear evidence of the successive triggering of pilot and main thyristor.

Introduction

Due to their superior performance in terms of current density and blocking voltage, silicon carbide (SiC) thyristors are of particular interest for pulsed power applications [1-3]. Furthermore, in view of the tremendous progress made in SiC crystal quality and wafer size, large-area SiC thyristors appear to be in reach today. In this context, both electrically and optically triggered SiC thyristors require adequate amplifying gate structures. With the aim to investigate this aspect, a mask set featuring numerous SiC thyristor devices with varying amplifying gate structures has been conceived [4]. And based thereon, a 100 mm epitaxial SiC wafer was processed recently. Resulting from this process run, the present paper reports on the electrical characteristics measured on-wafer as well as on singularized and encapsulated SiC thyristor devices with and without amplifying gate.

Device Fabrication and Structure

The fabricated devices are asymmetrically blocking, vertical SiC thyristors, of which the 10 µm thick p-base (drift) layer (5×10^{15} cm^{-3}) is separated by a 4 µm p-type buffer (5×10^{17} cm^{-3}) from the wafer substrate (> 1×10^{19} cm^{-3}). The n-base (gate) and the anode layers have a nominal thickness (and doping concentration) of 2 µm (1×10^{17} cm^{-3}) and 1 µm (1×10^{19} cm^{-3}), respectively. The gate and the single-step junction termination extension (JTE) are formed simultaneously by reactive ion etching (RIE). A second RIE step was used to define the JTE length and thus the device mesa. Following the etching, the primary metallization of gate/cathode (Ti/Ni) and anode (Ni/Ti/Al) was realized separately by e-beam evaporation, lift-off, and subsequent annealing. The surface was passivated with 1 µm thick, deposited SiO_2. The over-metallization consists of 1 µm Al and 0.7 µm Ti/Ni/Au on the top-side (anode/gate) and the backside (cathode) contacts, respectively.

Fig. 1 shows a scheme of a circular SiC amplifying gate thyristor with characteristic dimensions (radii). All fabricated amplifying gate thyristors have a central, circular gate (G) with a radius of r_{EA} = 160 µm and a main anode (A), expanding from an inner radius of r_{EM} = 500 µm to a distance of r_{SM} = 1200 µm. Therefore, all devices have the same size of the anode and thus the same resistance R_M of

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the main thyristor (*cf.* cross-section in Fig.1). At the distance of r_{SM}, either ring-shaped or dotted anode shorts are situated for devices with a circular or a square-shaped anode, respectively. With a JTE length of 150 µm and a security margin to the cutting edge, the die size measures 3.2 mm × 3.2 mm (0.1 cm^2). Fig. 2 depicts one of the experimental amplifying gate thyristors with square-shaped anode and dotted anode shorts.

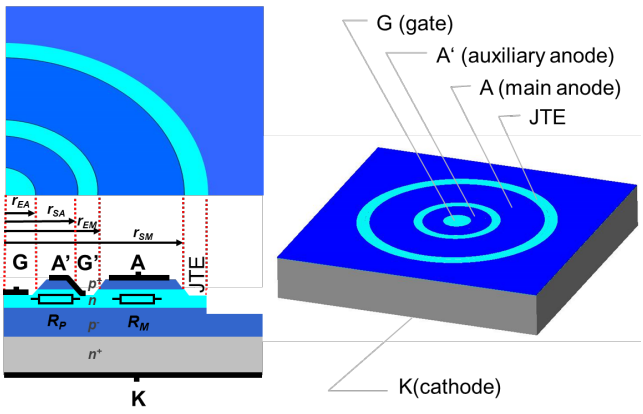

Fig. 1. Scheme of an SiC amplifying gate thyristor, consisting of a pilot thyristor (index P) in the centre and a main thyristor (index M) with the characteristic resistances R_P and R_M.

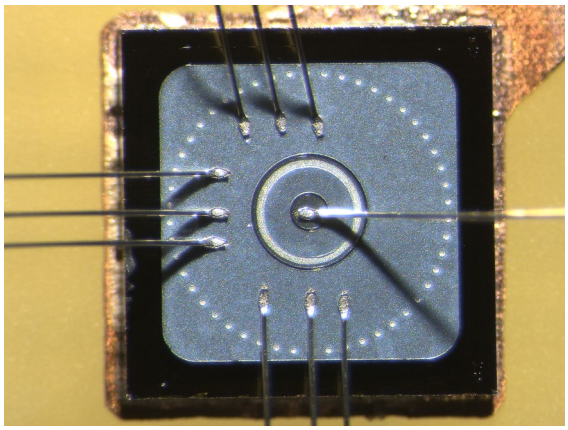

Fig. 2. Micrograph of an experimental, 3.2 × 3.2 mm^2 SiC amplifying gate thyristor with square-shaped anode and dotted shorts (r_{SA} = 400 µm). Gate (centre) and anode wedge-bonded with 50 µm Al wires, cathode (backside) solder attached.

In-between gate and main anode, the amplifying gate is located, consisting of the anode A' of the pilot thyristor and the auxiliary gate G'. The etch-step separating A' and G' forms a circle with varying radius of r_{SA}. This way, the resulting thyristors meet the amplifying gate design criterion ($R_P > R_M \Rightarrow r_{SA}/r_{EA} > r_{SM}/r_{EM}$)* [4, 5] to different degrees:

- safe (r_{SA} = 460 µm): the pilot thyristor always triggers the main thyristor
- adequate (r_{SA} = 400 µm): still ok, but susceptible to technological uncertainties
- non-adequate (r_{SA} = 300 µm): the pilot is less sensitive than the main thyristor, which may reverse the triggering order, negating the benefits of the pilot.

Electrical Characterization

On-wafer (in a vacuum probing chamber), the best devices demonstrated stable blocking up to 2 kV. After dicing, bonding, and encapsulation they were repeatedly tested up to 1.2 kV, the nominal voltage they were conceived for. Fig. 3 exemplarily shows the blocking characteristics (on-wafer and encapsulated) of a square-shaped SiC thyristor with safely designed (r_{SA} = 460 µm) amplifying gate and dotted anode shorts (device A). For comparison, the characteristic of a thyristor without amplifying gate is shown (device B), representing one of the best devices in terms of blocking capability. The higher leakage current of encapsulated devices is due to the lower current resolution of the curve tracer. The real leakage current (measured using an SMU on an equivalent device) is in the order of some nanoamperes (not shown), and thus only slightly higher than that one measured on-wafer under vacuum.

Fig. 4 shows on-state characteristics (at varying gate currents) of the same amplifying gate thyristor (bottom graph) as in Fig. 3 (device A), compared to a device without amplifying gate (top graph). As expected, the amplifying gate thyristor shows a characteristic snap-back. Note that the difference in the differential on-resistance is due to a spread between samples and not a characteristic difference between the two device types.

* The radius r_{SA} is the only varying parameter. The other radii, r_{EA}, r_{SM}, and r_{EM} are constant for all devices (cf. text).

By contrast, the fact that the amplifying gate thyristor requires a higher gate current to trigger, means a characteristic difference. For comprehension, note that the amplifying gate thyristors under investigation are experimental devices with a small periphery (main thyristor). They have been conceived only for the purpose of examining the design constraint. Their amplifying gate has about the same size as the gate of the comparative thyristor (without amplifying gate), but due to the parallel current path formed by R_P and R_M, they require a larger gate current to trigger. In terms of a reduced gate current, the amplifying gate only takes advantage when it supplies the gate current via an interdigitated structure to a large area (main) thyristor.

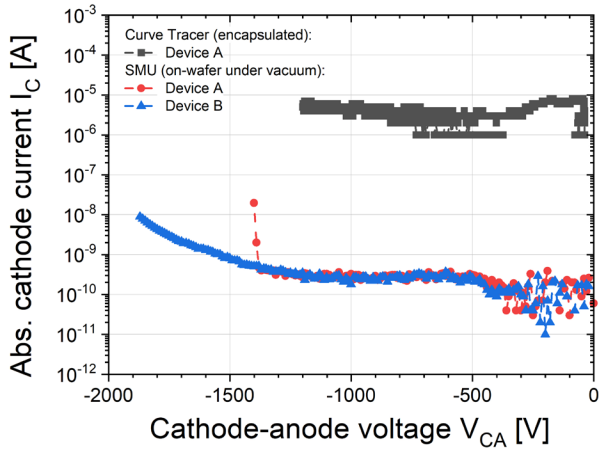

Fig. 3. Forward blocking characteristics of two SiC thyristors measured on-wafer with an SMU (up to breakdown) and after bonding and encapsulation with a curve tracer (limited to 1.2 kV).

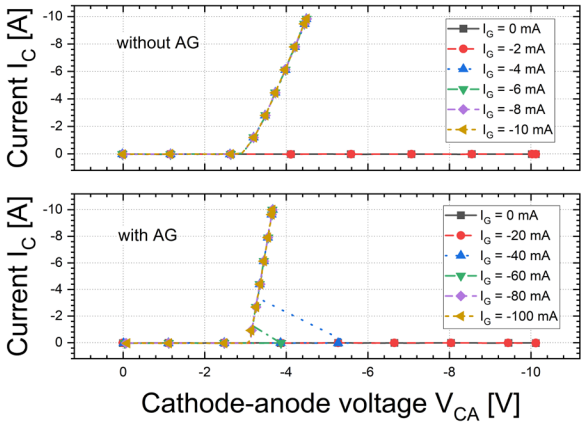

Fig. 4. On-state characteristics of encapsulated SiC thyristors with and without amplifying gate (AG).

Fig. 5 shows the gate-anode I-V characteristics of three SiC thyristors with differently dimensioned amplifying gate (non-adequate, adequate and safe, *cf*. above), allowing to determine the characteristic resistances R_P and R_M of pilot and main thyristor, respectively. R_P is directly derived from the slope of the I-V characteristic measured between the gate contact G (in the centre) and the ring shaped anode A' of the pilot thyristor (*cf*. Fig 1). In the same way, $R_P + R_M$ (and thus R_M) is determined from the slope of the I-V characteristic measured between G and the main anode A. Tab. 1 summarizes the extracted values which confirm the compliance to the above mentioned design rule ($R_P > R_M$).

Finally, Fig. 6 shows turn-on characteristics of circular and square SiC thyristors disposing of ring-shaped and dotted anode-shorts, respectively. For each of these two types, the curves of three devices with differently dimensioned amplifying gate are shown. Note, that though giving the impression of a logical sequence, there is no coherence of the turn-on delay time with the individual device dimensions. It appears rather that devices with adequately and safely designed amplifying gate reveal a peak-shaped inversion in the gate current and voltage transients, while non-adequately designed devices do not. These peaks originate from the current passing through the anode A' of the pilot thyristor, delivering the gate current for the main thyristor. This way they prove evidence that the pilot thyristor is triggered in advance of the main thyristor, which obviously does not emerge for thyristors with non-adequately designed amplifying gate.

Conclusion

The results presented in this paper demonstrate that the experimental SiC amplifying gate thyristors under investigation can be triggered adequately fully compliant to the underlying design constraints. Furthermore, the measurements reveal relatively large resistances R_P and R_M of pilot and main thyristor, respectively, being causal for meeting these constraints. Anyway, the main part of the resistance, here quantitatively about 70%, is determined by the sheet resistance of the n-base layer (gate) underneath the two sub-thyristors. The rest, however, as calculations based on TLM

measurements indicate, must be attributed to the contact resistance to the n-base layer. Nevertheless, this relatively high amount does not negatively affect the adherence to the design rule. In so far, the conceived amplifying gate structures can be used as design building blocks for larger area, electrically or optically triggered SiC thyristors.

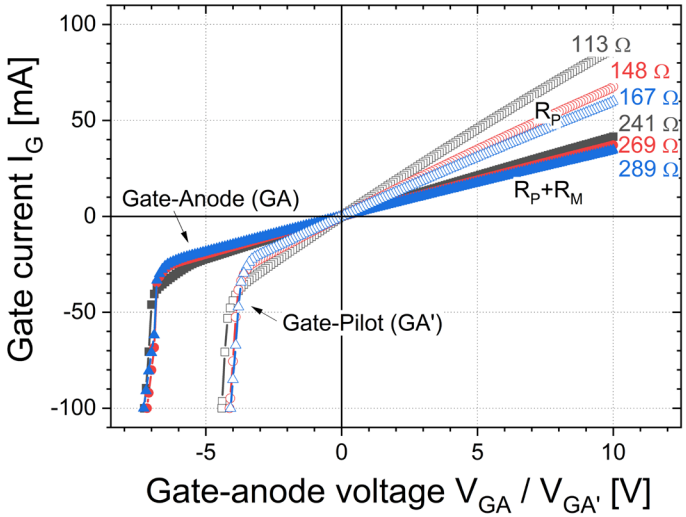

Fig. 5. Gate-anode characteristics (measured on-wafer) of SiC thyristors with differently dimensioned amplifying gate (*cf.* Tab.1).

Tab. 1. Resistance R_P and R_M extracted from Fig. 5.

	Non-adequate	Adequate	Safe
R_P	113 Ω	148 Ω	167 Ω
R_M	125±3 Ω		

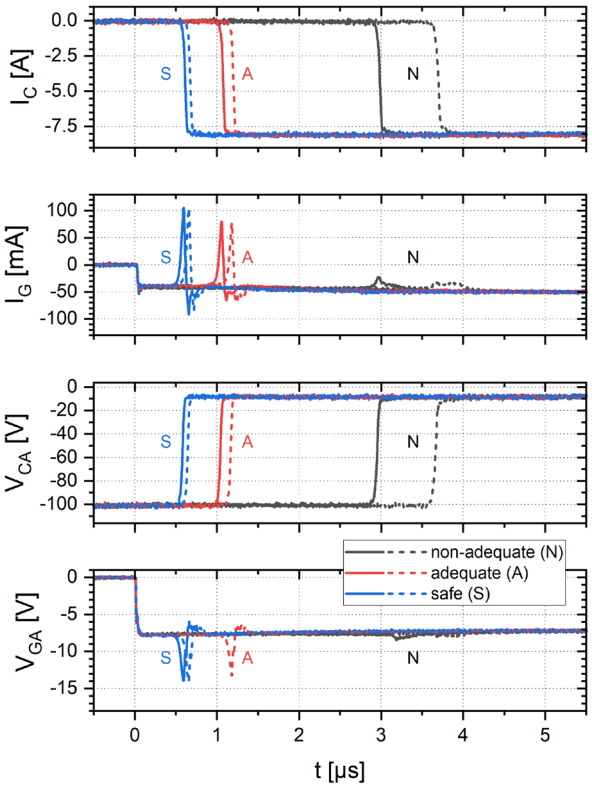

Fig. 6. Turn-on characteristics ($V_{CA,0}$ = -100 V, $I_{C,on}$ = -8 A) of encapsulated SiC thyristors with circular (solid lines) and square-shaped (dotted lines) anode, each with differently dimensioned amplifying gate (*cf.* legend).

Acknowledgement

Financial support provided by the French DGA under the research program ASTRID, contract no. ANR-11-ASTR-0011, is gratefully acknowledged.

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