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Gate Oxide Reliability and V_{TH} Stability of Planar SiC MOS Technology

M. Domeij[1,a,*], J. Franchi[1,b], S. Masloughkas[1,c],
P. Moens[2,d], J. Lettens[2.e], J. Choi[3,f], F. Allerstam[1,g]

[1]ON Semiconductor, Isafjordsgatan 32C, 16440 Kista, Sweden

[2]ON Semiconductor, Westerring 15, 9700 Oudenaarde, Belgium

[3]ON Semiconductor, 333 Western Avenue, 04106-1705 Maine, USA

E-mail: [a]martin.domeij@onsemi.com, [b]Jimmy.Franchi@onsemi.com,
[c]sotirios.masloughkas@onsemi.com, [d]peter.moens@onsemi.com, [e]jan.lettens@onsemi.com,
[f]jake.choi@onsemi.com, [g]Fredrik.Allerstam@onsemi.com

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Abstract. Similar charge to failure distributions with mean values of about 50 C/cm^2 were measured for planar SiC MOSFETs and MOS capacitors. Fast occurring and saturating negative flatband and threshold voltage drops were found in time resolved 1 second long pulsed gate current stress with I_G=1 mA/cm^2 at T=150 ºC. No substantial difference in V_{TH} drift rate with V_{GS}=28 V at T=150 ºC was found after about 10 s recovery period for I_G stressed devices compared with unstressed devices. Additionally, I_G stressed and unstressed devices did not differ in final V_{TH} shift at T=25 ºC after V_{GS}=28 V stress (during 3 hrs or 31 hrs). More gate oxide reliability characterization is important to determine if 1 mA/cm^2 pulsed gate current stress creates any permanent changes to the SiC MOSFET device behaviour. Additionally, parametric shifts in V_{TH} and R_{DSon} was examined after long-term AC gate bias stress by a gate driver switching between -8V and 20V for four different commercially available SiC MOSFETs.

Introduction

Electrical characterization of SiC gate oxides at high electric fields is important for oxide lifetime modeling, for quality sampling and for screening of potentially unreliable SiC MOSFET chips. Forced gate current (I_G) stress [1-2] with measurement of charge to failure (Q_{BD}) is a way to monitor gate oxide quality with reduced influence of oxide thickness variations. In this work, Q_{BD} results are shown for planar SiC MOSFETs in comparison with n-type MOS capacitors (MOScaps) and Si MOSFETs. I_G stress of SiC MOSFETs at high oxide fields has been reported to cause significant negative shifts of threshold voltage (V_{TH}), and this effect has been attributed to oxide trapping of impact ionization generated holes [3]. To study this effect, transient measurements of gate voltage (V_G) during I_G stress were carried out for n-type SiC MOScaps and planar MOSFETs to monitor shifts in flatband voltage (V_{FB}) and V_{TH} respectively. Additionally, V_{TH} was measured during positive V_G stress for previously I_G stressed SiC MOSFETs to examine V_{TH} recovery, and to compare V_{TH} drift during positive V_G stress with unstressed devices.

Another important type of gate bias induced parametric drift of SiC MOSFETs is V_{TH} and on-resistance (R_{DSon}) increase after AC gate bias stress [4-5]. This type of drift has been studied for commercially available SiC MOSFETs subjected to stress using a -8V/20V operating gate driver.

Experimental Results

Gate oxide charge to failure (Q_{BD}). Constant I_G stress until failure was performed for SiC MOSFETs, SiC MOScaps and Si MOSFETs. The SiC MOSFETs are vertical planar channel 1200 V devices with $V_{TH}\approx$3 V and R_{DSon} of about 40 mΩ. The large area (0.0729 cm^2) MOScaps were fabricated on an n-type epilayer with the same doping concentration as the drift layer of the SiC MOSFETs. The MOScaps have about 10 % thicker gate oxide than the MOSFETs and the gate oxide process is otherwise similar. The Si MOSFETs are a discrete product, and all three types of devices

have been fabricated in the same wafer fab at onsemi. The tested MOScaps were pre-screened with V_G=28 V and the SiC MOSFETs have passed a production type wafer sort program.

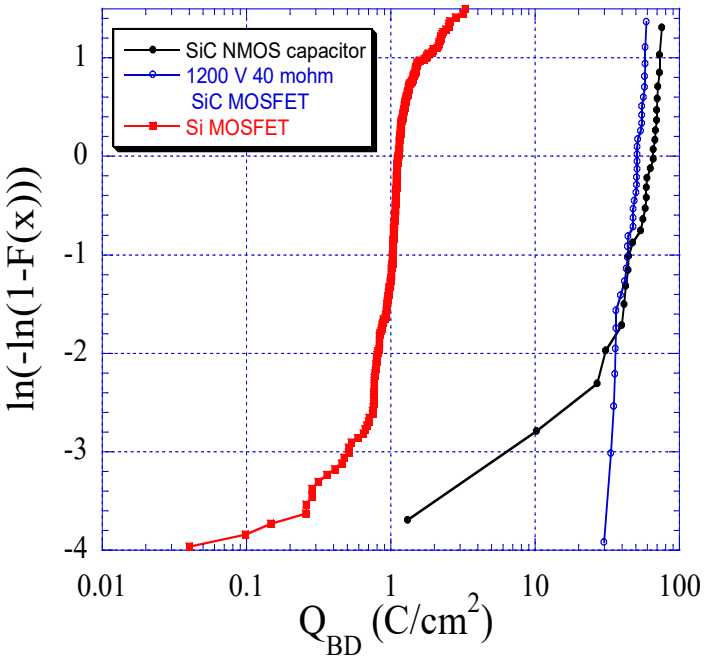

Fig. 1. Q_{BD} measured for SiC MOSCAPs (28 pcs), 1200 V 40 mΩ SiC MOSFETs (35 pcs) and a Si MOSFET product when forcing I_G=5 mA/cm^2.

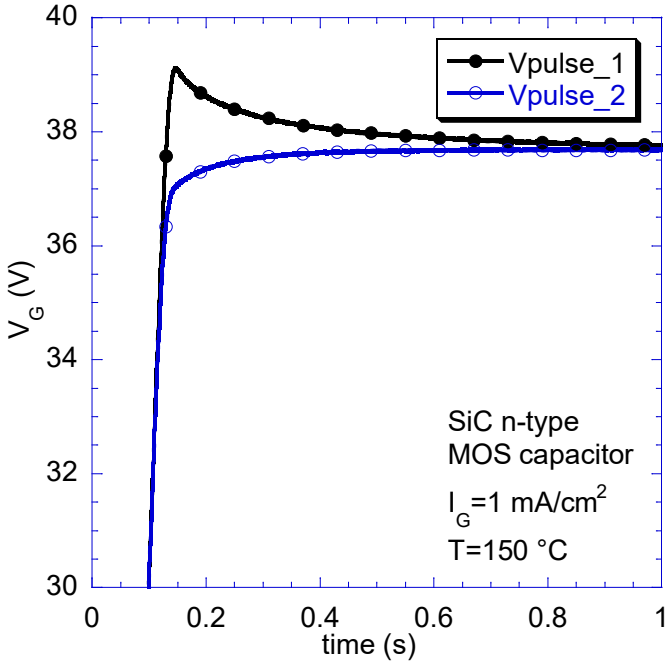

Fig. 2. V_G vs. time for 0.0729 cm^2 n-type MOScaps during 1 second pulses of forced gate current stress I_G=1 mA/cm^2 at T=150 ºC

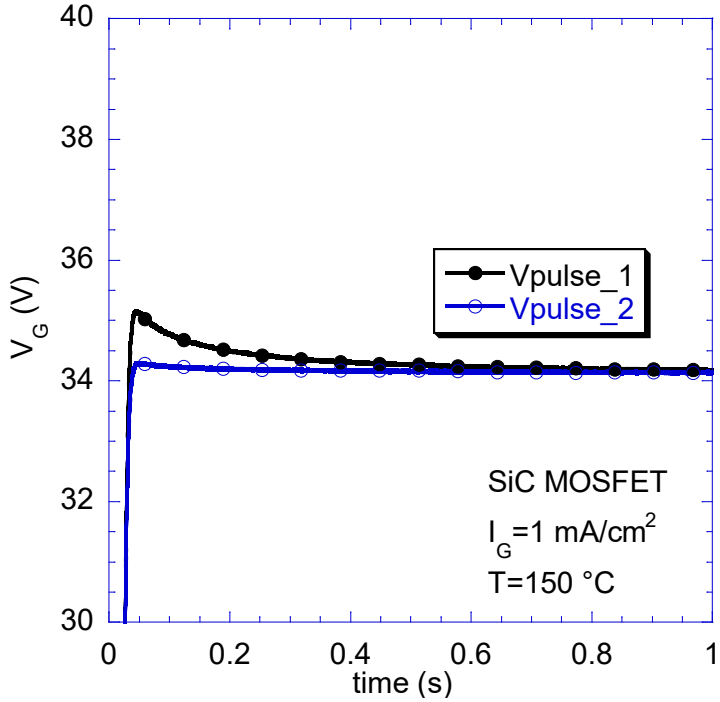

Fig. 3. V_G vs. time for 1200 V 40 mΩ SiC MOSFETs during 1 second pulses of forced gate current stress I_G=1 mA/cm^2 at T=150 ºC

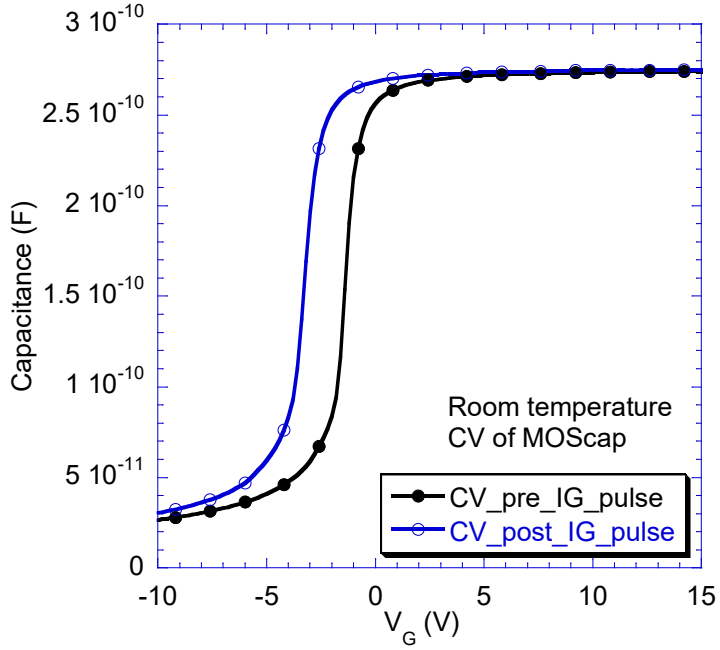

Fig. 4. Room temperature CV sweep of MOScap before and after 1 second pulses of forced gate current stress I_G=1 mA/cm^2 at T=150 ºC

Fig. 1 shows measurements of Q_{BD} after forced I_G stress with 5 mA/cm^2 (gate area) at T=25 ºC for all three device types. The SiC MOSFET Q_{BD} value of 50 C/cm^2 is state-of-the-art, slightly exceeding [1]. The tail-free distribution indicates that the device chips are free from locally weak spots and are well matching the planar MOScaps. Fig. 1 illustrates that the SiC MOS technology exceeds the Si MOSFET product in terms of Q_{BD} by 50x.

Analysis of pulsed I_G stress. Positive gate bias stress with moderate oxide fields typically cause positive V_{FB} shifts due to trapping of electrons in near interface traps [6]. The gate oxides studied in this work have electric fields around 9 MV/cm during I_G stress in the mA/cm^2 regime, and for such high oxide fields we can expect negative shifts of V_{TH} as reported in [3]. Figs. 2-3 show measurements

of transient V_G during 1s long pulsed I_G stress with 1 mA/cm^2 at T=150 ºC for the same type of SiC MOScaps and SiC MOSFETs as in Fig. 1. In both cases we see transient decrease of V_G during the 1st pulse, presumably due to gradually reduced V_{FB} and V_{TH} values caused by trapping of positive hole charge or emission of negative trapped charge. It is interesting to note that the V_G levels saturate after a few 100 ms for both MOScap and MOSFET. No voltage peak occurred during a 2nd I_G pulse (see Figs. 2-3) and the voltage levels at the end of the 1st and 2nd pulses are very similar. A possible explanation for this observed voltage saturation during the 1s pulsed I_G stress is filling of pre-existing traps by holes generated by impact ionization [3] or by anode hole injection [7].

Fig. 4 shows room temperature CV sweeps for a MOScap before and after a 1 s pulse with I_G=1 mA/cm^2 at T=150 ºC. The resulting negative V_{FB} shift of 1.95 V is qualitatively well in line with the observed voltage drop of about 1.4 V from peak to plateau during I_G stress (at T=150 ºC) in Fig. 2. For the SiC MOSFET, V_{TH}=2.34 V was measured at T=150 ºC before and V_{TH}=2.25 V was measured after the 1 s I_G pulse. From these results it can be concluded that the observed voltage drops during I_G stress in Figs. 2 and 3 are linked to reduced V_{FB} and V_{TH} respectively. The 0.09 V negative V_{TH} shift of the MOSFET is much smaller than the voltage drop of about 0.9 V observed during the I_G pulse in Fig. 3. A possible explanation for this fast V_{TH} recovery of the MOSFET is capture of electrons supplied to the channel from the highly doped source during the V_{TH} measurement.

Recovery and drift of V_{TH} after forced I_G stress. Positive gate bias stress with V_{GS}=28 V was carried out at T=150 °C for SiC MOSFET devices previously stressed with I_G=1 mA/cm^2 during 1 second and unstressed devices (2 of each type). Fig. 5 displays V_{TH} vs. time where the stressed devices recover and V_{TH} reaches the value the unstressed ones after 10-20 s. Despite the faster initial V_{TH} shift of the stressed devices, the drift curves later proceed in parallel, showing no significant difference in V_{TH} drift rate. The summary in Table 1 shows that there are only small V_{TH} differences at T=150 C after stress with V_{GS}=28 V at T=150 ºC during 1.11e4 s (~3 hrs), and the finally measured V_{TH} shift at T=25 ºC is identical for I_G stressed and unstressed devices. These results indicate that the V_{TH} drop resulting from the pulsed stress with I_G=1 mA/cm^2 (see Fig. 3) does not cause any permanent changes to V_{TH} and V_{TH} stability as it is measured in regular slow V_{TH} measurements. Additional characterization such as ultra-fast BTI measurements and time dependent dielectric breakdown (TDDB) is important to detect possible effects on device behaviour by the I_G pulse. Degradation of TDDB characteristics is, however, not expected due to the low charge of about 1mC/cm^2 for the I_G pulse compared with the measured mean Q_{BD} of 50 C/cm^2 (see Fig. 1).

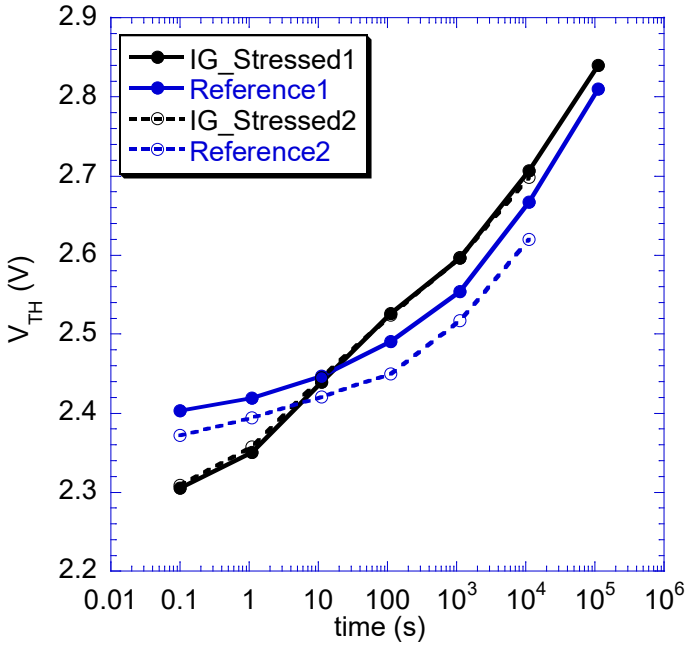

Fig. 5. V_{TH} vs. time during stress with V_{GS}=28 V at T=150 ºC for two devices previously stressed with I_G=1 mA/cm^2 for 1 second and two unstressed devices

Table 1. V_{TH} measured before and after the performed tests including I_G=1 mA/cm^2 at T=150 ºC for 1 s, and the following stress with V_{GS}=28 V at T=150 ºC

	Measured V_{TH} (V)			
Test sequence/Device ID	**IG_stressed1**	**Reference1**	**IG_stressed2**	**Reference2**
T=25 °C before I_G stress	3.00	3.00	3.00	2.96
T=150 °C before I_G stress	2.34	2.34	2.35	2.32
T=150 °C after I_G stress	2.25	NA	2.25	NA
T=150 °C after V_{GS}=28 V at T=150 °C for 1.11e4 s	2.71	2.67	2.70	2.62
T=25 °C after V_{GS}=28 V at T=150 °C	3.22 after **1.11e5** s	3.22 after **1.11e5** s	3.05 after **1.11e4** s	3.01 after **1.11e4** s

AC gate bias stress. A different type of parametric drift under AC gate bias V_{GS} stress (between negative and positive V_{GS}) with moderate oxide fields is described in ref. [4-5], where a positive drift of V_{TH} and R_{DSON} was reported. The number of switching cycles, the level of negative V_{GS}, and V_{GS} voltage over- and undershoots are pointed out as key factors for this type of drift [4-5]. A transient and overshoot free V_{GS} stress was performed at T=25 ºC with V_{DS}=0 V using a gate driver switching between -8 V and 20 V with 50 % duty cycle. The stress measurements were interrupted after different time intervals to run a test program consisting of V_{TH} and R_{DSon}. Delta shifts of V_{TH} and normalised R_{DSon} shifts are shown in Fig. 6 for onsemi's commercially available 1200 V 80 mohm SiC MOSFET together with 1200 V SiC MOSFET products from three other manufacturers. The results are qualitatively well in line with ref. [5], and it should be noted that V_{GS}= -8 V is outside the datasheet rating for two of the tested SiC MOSFETs.

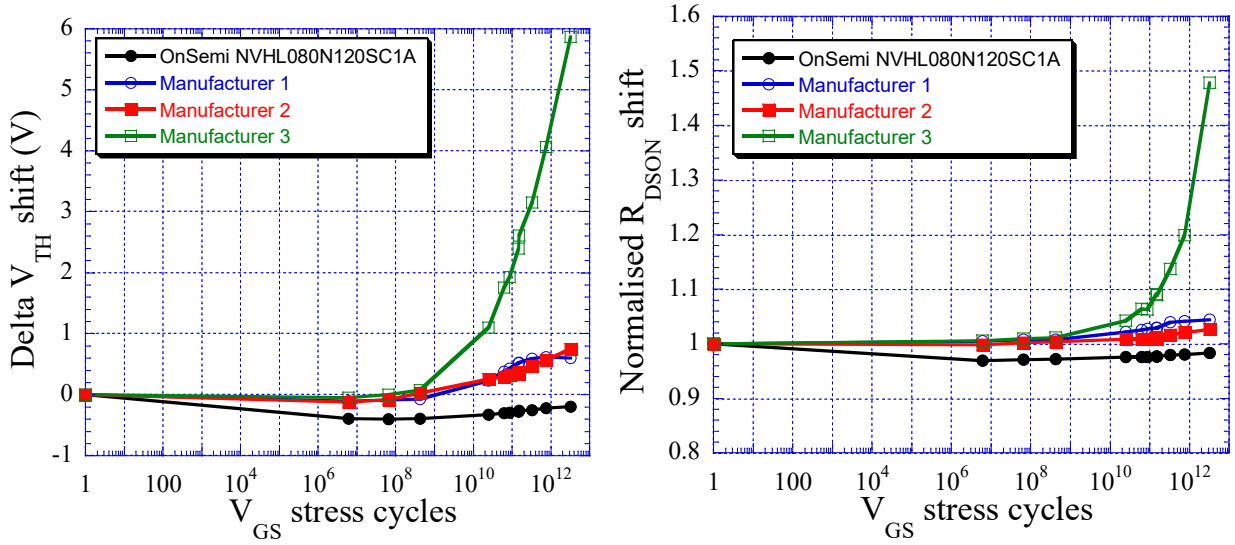

Fig. 6. Delta V_{TH} shift and R_{DSON} vs. cycles of transient V_{GS} between -8 V/20 V (50 % duty cycle) at T=25 ºC (the initial condition is plotted as 1 cycle due to the log scale). V_{TH} and R_{DSON} values were recorded by moving the device to an ATE socket and running a program consisting of V_{TH} and R_{DSon}.

Summary

Q_{BD} distributions were measured for SiC MOScaps and MOSFETs with state-of-the-art mean values of about 50 C/cm^2. Fast and quickly saturating negative flatband and threshold voltage drops were found for MOScaps and MOSFETs in time resolved pulsed gate current stress with I_G=1 mA/cm^2 at T=150 ºC during 1 second. No substantial difference in V_{TH} drift rate with V_{GS}=28 V at T=150 ºC was found after a 10-20 s recovery period for the I_G stressed compared with unstressed devices. Additionally, I_G stressed and unstressed devices did not differ in final V_{TH} shift at T=25 ºC

after V_{GS}=28 V stress at T=150 ºC (during 3 hrs or 31 hrs). Additional characterization is needed to determine if any permanent change to the device behaviour is caused by the 1 s pulsed I_G stress using 1 mA/cm^2 with its observed negative V_{TH} drop. Finally, parametric shifts in V_{TH} and R_{DSon} was examined after long-term AC gate bias stress by a gate driver (switching between -8 V and 20 V) for 4 different commercially available SiC MOSFETs.

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