Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 519-522
doi:10.4028/p-2pm0e2

Submitted: 2021-10-15
Revised: 2022-02-23
Accepted: 2022-03-17
Online: 2022-05-31

DC Modeling of 4H-SiC nJFET Gate Length Reduction at 500°C

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Keywords: Turn-Off Characteristics, COMSOL, Shallow Nitrogen Implant, Phosphorous Implant

Abstract. The development of robust, high-performance integrated circuits (ICs) will enable numerous potential NASA missions of current interest, including long-duration robotic missions exploring the 460 °C surface of Venus. Currently, NASA is looking towards SiC-based devices to provide such a solution. However, the current NASA silicon carbide (SiC) JFET device with a channel length of 6 µm (recently fabricated Gen. 11 ICs) limits mission-relevant circuit capabilities. In this study, we combined experiments with simulations to explore two straightforward fabrication strategies (shallow n^- and extended n^+) to reduce the SiC JFET channel length while maintaining the turn-off behavior needed to realize 500°C circuit operation. COMSOL Multiphysics was used to simulate the transfer characteristics and maximum potential below the gate of a 4H-SiC nJFET at 500°C, and a 1 µm gate length nJFET with turn-off performance comparable to the state-of-the-art is suggested.

Introduction

NASA is exploring silicon carbide, a wide band-gap semiconductor material capable of operating at high temperatures, to create robust, high-performance electronics that can work in harsh environments (high radiation levels and high Venusian surface temperatures) [1]. A step towards this goal is to substantially reduce the channel length of 4H-SiC nJFETs recently fabricated in the Gen. 11 ICs [2] from 6 µm to 1 µm. There are various strategies to reduce the gate length and feature size of a 4H-SiC JFET [3]. This paper presents a study on reducing the gate length of a lateral nJFET by comparing and contrasting two fabrication strategies. The first fabrication strategy uses a shallow self-align nitrogen implant (SN, Fig. 1a) along the device's top surface but not below the gate combined with a high-dose phosphorous implant directly below the source and drain contacts, while the second strategy (Fig. 1b) uses high-dose phosphorous implants that extend from below the contacts up to the gate

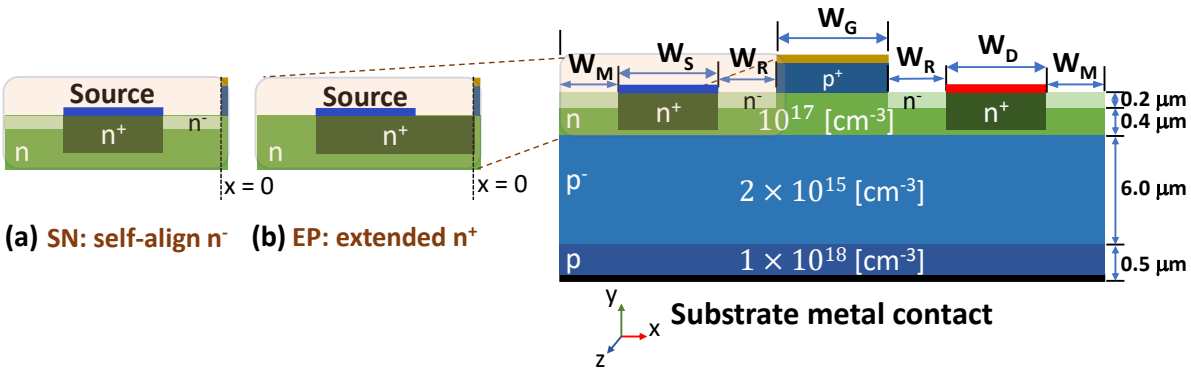

Fig. 1: Schematic for the 4H-SiC nJFET device with two doping strategies: a) self-align nitrogen (SN) and b) extended phosphorous (EP). The different layers are p substrate (blue), p^- sub-channel layer (light blue), n epitaxial layer (green), n^+ source and drain epilayer (dark green), n^- nitrogen self-align implant (light green), and p^+ gate epilayer (dark blue).

edges. These two doping strategies are explored in order to shorten gate length while maintaining or improving nJFET's turn-off performance. For this study, twelve variations of lateral epitaxial 4H-SiC nJFETs with different fabrication strategies, gate lengths, and geometric properties were simulated in COMSOL. However, only a few key results are shown for brevity.

Methodology

Experiment. The first fabrication strategy uses a shallow self-align nitrogen implant (Figure 1a) along the device's top surface but not below the gate combined with a high-dose phosphorous implant directly below the source and drain contacts. The SN device structure is consistent with experiments by NASA GRC in prototype IC generations 10 and 11 [2]. The experiments were performed at $500\,°\text{C}$ and the n epilayer thickness of the device was $0.42\,\mu\text{m}$.
Simulations. The 4H-SiC nJFET was simulated using COMSOL Multiphysics v5.6 with the semiconductor module. The material parameters and the physical models used to simulate the electrical potential and carrier concentration profiles were taken from Ref. [4]. The models used to simulate the physics for nJFET were: Auger recombination, Shockley-Read-Hall (SRH) recombination, incomplete ionization, and low-field mobility. The details of the model, its implementation, and the simulation protocol for simulating a 4H-SiC nJFET in COMSOL are available on reasonable request.

Results and Discussion

Before the gate length reduction studies, the turn-off and transfer characteristics of the COMSOL simulations were validated with the measured data of a 4H-SiC nJFET with the SN strategy at $500\,°\text{C}$, and the results are presented in Fig. 2. The threshold voltage (V_{th}) were computed using the saturation extrapolation technique. Using this method, the simulated (experimental) values of V_{th} are computed to be $-9.83\,\text{V}$ ($-9.66\,\text{V}$), when $V_s = -25\,\text{V}$, and $-11.26\,\text{V}$ ($-10.68\,\text{V}$), when $V_s = -15\,\text{V}$. While the values of I_{dss} are $13.11\,\mu\text{A}\,\mu\text{m}^{-1}$ ($11.46\,\mu\text{A}\,\mu\text{m}^{-1}$) and $15.03\,\mu\text{A}\,\mu\text{m}^{-1}$ ($13.02\,\mu\text{A}\,\mu\text{m}^{-1}$), respectively.

The simulations show that the V_{th} is similar for both the doping strategies, while the saturated drain current (I_{dss}) is about 10% higher for the EP strategy. The higher value of I_{dss} results from the deeper and higher concentration of dopants used in the EP strategy. The fit with the experiments validates the 4H-SiC nJFET model implementation and the simulation protocol. Note that the high

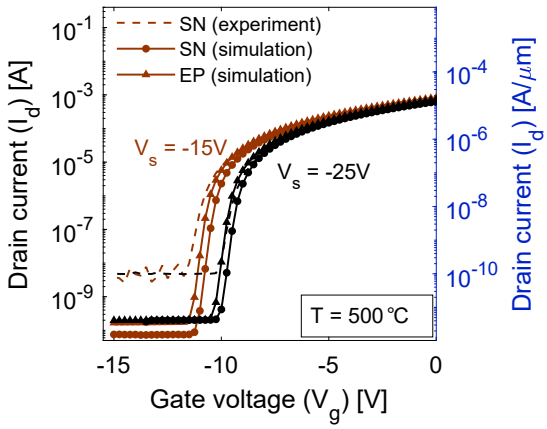

Fig. 2: The $V_d = 20\,\text{V}$ transfer characteristics for a $6\,\mu\text{m}$ gate length 4H-SiC nJFET with self-align N (simulation results from the EP strategy is shown for comparison) is validated with measured experiments for two substrate biases, $-25\,\text{V}$ (black) and $-15\,\text{V}$ (brown), at $500\,°\text{C}$. Left axis shows the total I_d ($48\,\mu\text{m}$ wide device) while the right axis shows normalized I_d. Note that measured current floor was limited by package leakage extrinsic to the device and was not simulated.

Table 1: Transfer characteristics for various 4H-SiC nJFET designs simulated at 460 °C. SN and EP were the two implant strategies used to reduce gate-to-source resistance. The parenthetical values are for the SN strategy. For the * case, the n epilayer thickness was reduced from 0.40 µm to 0.34 µm.

#	Type	W_M [µm]	W_S [µm]	W_R [µm]	W_G [µm]	$-V_{th}$ [V]	I_{dss} [A/m]
1	SN	3.0	6.0	3.0	6.0	8.2	11.8
2 (3)	EP (SN)	3.0	6.0	4.5	3.0	8.8 (8.8)	28.6 (22.9)
4 (5)	EP (SN)	3.0	3.0	5.5	1.0	14.1 (15.8)	105.9 (66.3)
6* (7*)	EP (SN)	3.0	3.0	5.5	1.0	8.8 (9.4)	63.2 (36.6)

value of the turn-off current floor in the experiments was a result of the package leaking current [5]. Thus, the simulation model parameters were not modified to quantitatively match the experimental off-state current floor.

Table 1 compares the DC electrical performance of nJFETs with decreasing gate length for each of the doping strategies. These results are consistent with short-channel device physics reported in the literature for other types of field-effect transistor structures. In other words, the ability of the negative gate bias to impose a higher potential barrier to inhibit electron transport from source to drain diminishes as channel length shrinks. This barrier reduction is evident in Figs. 4a-c. However, thinning the n epilayer channel does increase the potential barrier, as seen in devices as seen in devices #6* (Fig. 4d) and #7* (not shown). Note that this approach significantly tightens the processing margins and risk associated with still-maturing SiC epilayer thickness tolerance/control as well as the gate finger etch depth. While increasing the p-layer doping might also improve device turn-off performance, this would also increase the magnitude of substrate body bias effect that would present additional circuit design challenges. Another experimental risk of the EP strategy is the higher electric field and leakage currents it might impose where the EP implant borders the edge of the gate. While this has not been a problem in experimentally realized SN devices operated at 500 °C, the increased doping of the EP devices could raise the peak electric field in this region. Therefore, a further study of the EP approach is planned to elucidate its leakage and breakdown properties.

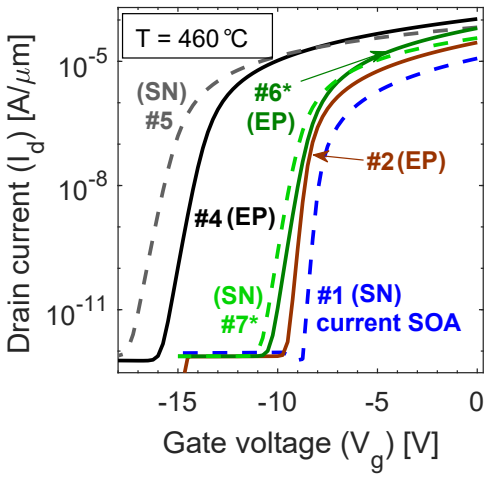

Fig. 3: The simulated turn-off characteristics for selected designs, each I-V curve is annotated with its device number from Table 1. Simulation results from the nitrogen self-align strategy are shown using dashed lines, while the extended phosphorous strategy results are shown using solid lines. Other simulation parameters were: $V_s = -25$ V, $V_d = 20$ V, and $T = 460$ °C.

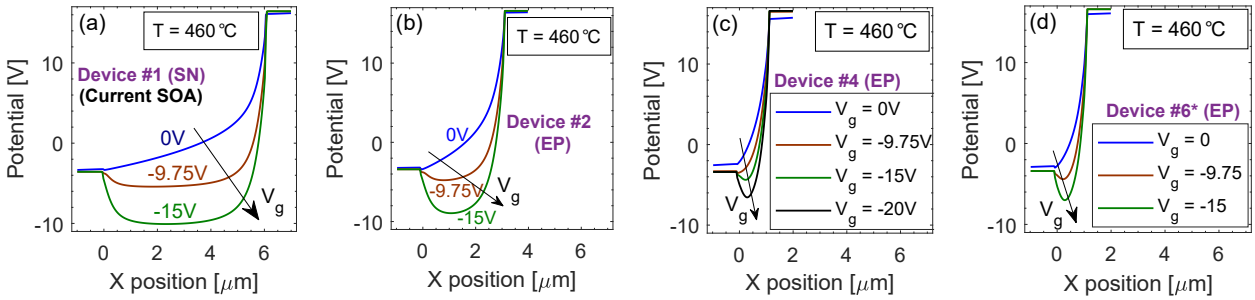

Fig. 4: The value of the maximum potential below the gate for the selected devices (1, 2, 4, and 6) listed in Table 1. Other simulation parameters were: $V_s = -25$ V, $V_d = 20$ V, and $T = 460$ °C.

Conclusions

This paper explored design strategies to optimize the lateral-gate-length of a 4H-SiC nJFET operating at 500 °C using COMSOL multiphysics. We compared the turn-off characteristics of two fabrication strategies, SN and EP, with gate length decreasing from 6 µm to 1 µm. The results show that the deeper and high concentration of phosphorous dopants combined with a thinner n epitaxial channel led to a better turn-off response when decreasing gate length. Simulations resulted in a 4H-SiC nJFET design with a 1 µm gate length without compromising the turn-off performance.

Acknowledgments

Computational work was performed at NASA Ames Research Center with financial support from the Center Innovation Fund (CIF), NASA Ames Research Center, while the experimental work was performed at NASA Glenn Research Center with funding from the NASA Science Mission Directorate under Long-Lived In-Situ Solar System Explorer (LLISSE).

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