Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 528-532
doi:10.4028/p-oajc69

Submitted: 2021-10-22
Revised: 2022-02-25
Accepted: 2022-03-17
Online: 2022-05-31

Multi-Layer High-K Gate Stack Materials for Low D_{it} 4H-SiC Based MOSFETs

Lakshmi Kanta Bera[a*], Navab Singh[b], Zhixian Chen[c], Calvin Chua Hung Ming[d], King Jien Chui[e], Ravinder Pal Singh[f], Yee Ye Sheng[g], Surasit Chung[h], K. Michael Han[i], Karen Chong[j] and Dim-Lee Kwong[k]

Institute of Microelectronics, 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634

[a*]beralk@ime.a-star.edu.sg, [b]navab@ime.a-star.edu.sg, [c]chenzx@ime.a-star.edu.sg, [d]chuahm@ime.a-star.edu.sg, [e]chuikj@ime.a-star.edu.sg, [f]ravinderps@ime.a-star.edu.sg, [g]Yee_Ye_Sheng@ime.a-star.edu.sg, [h]surasit_chung@ime.a-star.edu.sg, [i]Michael_Han@ime.a-star.edu.sg, [j]Karen_Chong@ime.a-star.edu.sg, [k]kwongdl@ime.a-star.edu.sg

Keywords: Silicon Carbide, High-k, multi stacks, interface traps.

Abstract. Metal-oxide-semiconductor capacitors with single and multi-layer high-K gate dielectrics on Si (0001) face of n-type 4H-SiC substrates have been investigated. Multi-layered nanolaminated gate-stack comprises alternating ultrathin (6nm) Al_2O_3 and HfO_2. A 5nm thick interfacial silicon oxynitride is deposited prior to laminated films to investigate interface trap properties and tuning of flat band voltage. Total thickness of gate-stack films including interfacial layer is 55nm. The thermal stability of multi-layered nanolaminated film is investigated using XTEM. Localized crystallization of HfO_2 is visible after RTA at 900°C while Al_2O_3 remains fully amorphous. Some of HfO_2 grains have extended into Al_2O_3 layer but was not able to crossover. The measured accumulation capacitance of 55nm thick gate dielectric gives an effective dielectric constant value of 9.6 and an equivalent oxide thickness of 22nm from high-frequency capacitance-voltage measurements. A positive flat band voltage (V_{FB}) of 12.2V and 10.6V are observed from both single layer HfO_2 and Al_2O_3 dielectrics, respectively due to presence of negatively charged oxygen interstitial defects generated during atomic layer deposition process. However, V_{FB} shifted towards negative voltage -7.6V for multi-layered Al_2O_3/HfO_2 stacks probably associated with positive Al and Hf interstitials at interface of Al_2O_3/HfO_2. Ultrathin interfacial oxynitride films is effective to reduce D_{it} to 3×10^{11}/eVcm^2 and tuning of V_{FB}. The breakdown field of stacked gate dielectric on 4H-SiC is 10.0 MV/cm.

Introduction

Silicon carbide is one of the most promising semiconductor materials used commercially for fabrication of high-power, high frequency, and high-temperature MOSFETs because of its wide band gap, high breakdown field, high thermal conductivity and ability to grow thermal SiO_2 for gate insulator. However, high temperature thermal oxidation processes cause residual carbon related defects at and near the SiO_2/SiC interface leading to high interface state density (D_{it}) and mobility degradation [1]. In addition, 2.5 times higher dielectric constant of SiC than SiO_2 predominantly increases electric field at gate insulator by the same order. These issues can be resolved through integration of high-K gate stacks with dielectric constant higher than that of SiC so that the electric field at the gate stack will be lower than the adjacent SiC and thus reduces dielectric stress. Lori et. al. studied several high-K gate stacks on SiC using MOCVD and PVD techniques but all the gate stack materials resulted in high gate leakage current [2]. Recent studies on (AlON) shows N-related defects leading to significant hole conduction. Hf was then incorporated into AlON to form HfAlON to reduce N-related defects and to improve insulating properties of the dielectric [3-4]. In this work, we developed multi-layer high-K gate dielectrics for 4H-SiC MOSFETs applications.

Experiment

Metal-oxide-semiconductor (MOS) capacitors were fabricated on Si-face (0001) n-type 4H-SiC substrates with 10-μm thick epitaxial layer. The samples were cleaned using piranha solution (H_2SO_4:H_2O_2=3:1) at 130°C for 10 minutes followed by rinsing with DI water and drying using N_2 gun. Native oxide was removed using dilute HF (DI:HF=50:1) for 60 sec prior to dielectric deposition. Multiple stacks of Al_2O_3/HfO_2 with an interfacial oxynitride (SiO_xN_y) layer were deposited in different combinations using atomic layer deposition (ALD). Fig.1 shows a physical cross-section view of stack of the gate laminate (A/B/A/B type) along with its corresponding band-diagram.

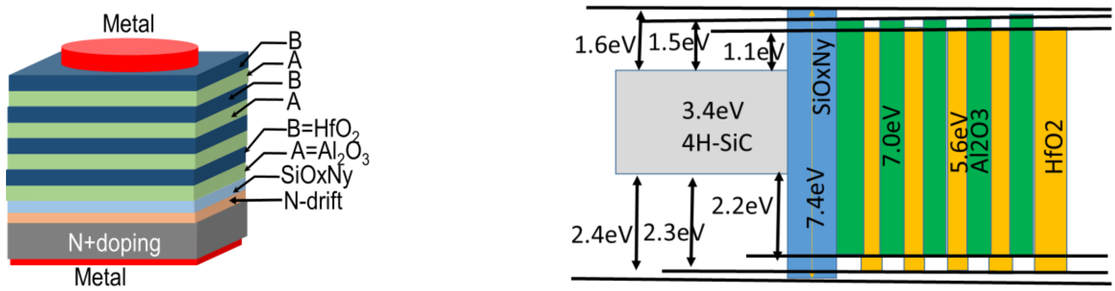

Fig. 1. Schematics of multi-layer high-k stacks with band alignment on 4H-SiC.

The atomic layer deposition (ALD) process involved cycling of precursor and reactant to achieve deposition of controlled and highly conformal layers at the atomic level. Cyclic nature of the deposition with alternate switching between Al_2O_3 and HfO_2 is thought to minimize pinhole defects in the film. MOS capacitors were then fabricated on a (0001) Si-face of 4H-SiC with 10μm thick N-doped homo-epilayer deposited on highly doped n-type substrate. A stack of Ni/Ti/Ni metal was evaporated on front side using a shadow mask to create MOS capacitor top electrodes, with blanket metal deposition on the substrate backside for the back contact. Samples were annealed at different temperatures to study the temperature stability of the gate stack and effect on D_{it}. Temperature stability is absolutely needed as silicide formation on SiC MOSFET is a high-temperature step (900 to 1000°C) and that occurs after gate stack formation.

Results and Discussions

The microstructural analysis to examine the interfaces of laminated multi-layered stacks after fabricaion of MOSCAP devices annealed at 900°C using transmission electron microscopy (TEM). The interfaces of alternating stacks of materials are distinctly maintained as illustrated in cross-sectional TEM images in Fig. 2 (a). The localized lattice fringes due to the crystallization of HfO_2 after RTA is observed in higher magnification TEM image (Fig 2(b)) while Al_2O_3 remained fully amorphous. Some of the grains extended towards Al_2O_3 layer but were not able to crossover the Al_2O_3 layer. The bottom SiO_xN_y layer remains smooth and amorphous.

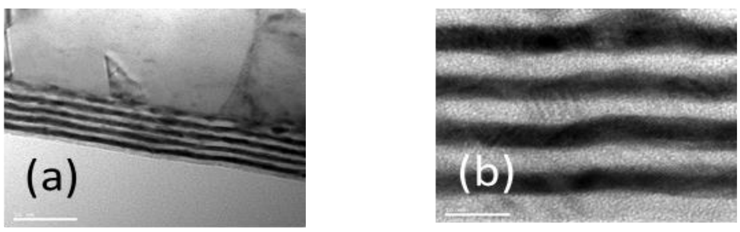

Fig. 2. TEM cross-section images of SiO_xN_y/Al_2O_3/HfO_2 multilayer stacks (a) and its high magnification image (b).

Fig.3 shows the high frequency capacitance-voltage (C-V) charateristics of several dielectric films. The slow rise of capacitance from inversion to accumulation is contributed by sevaral bulk charges and interface traps, and further development work is required to mitigate this issue. The measured accumulation capacitance of 55nm thick gate dielectric gives an effective dielectric constant value of 9.6 and an equivalent oxide thickness of 22nm using high frequency C-V data as shown in Fig. 3.

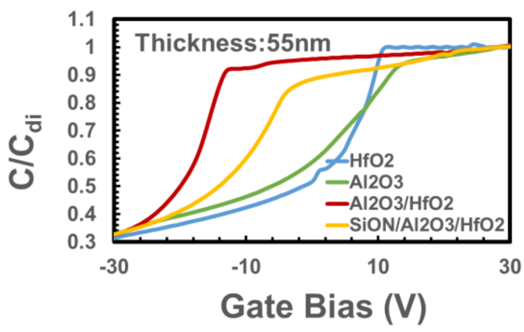

Fig. 3. Normalized C-V char. of different high-K gate stacks on 4H-SiC measured at 100kHz.

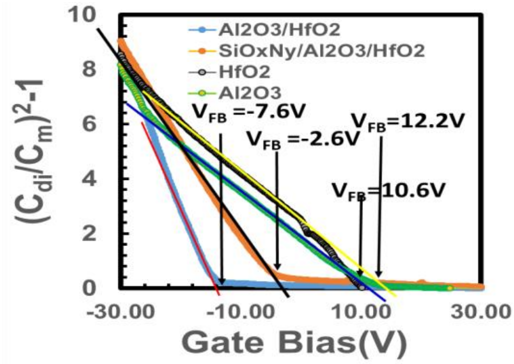

Fig. 4. Plot of $\left(\frac{C_{di}}{C_m}\right)^2 - 1$ vs VG to extract V_{FB}.

V_{FB} is extracted from experimental CV curve using the relationship in equation (1)

$$\left(\frac{C_{di}}{C_m}\right)^2 - 1 = \frac{{C_{di}}^2}{qN_D\varepsilon_S\varepsilon_0}(V_G - V_{FB}) \quad (1)$$

where C_{di} is the dielectric capacitance at accumulation and C_m the measured capacitance of the gate-stacks [5]. The plots of $\left(\frac{C_{di}}{C_m}\right)^2 - 1$ vs V_G for different gate stacks are shown in Fig. 4. The intersection with V_G axis of the linear extrapolation of the graph corresponds to $\left(\frac{C_{di}}{C_m}\right)^2 - 1 = 0$ giving $V_G = V_{FB}$. The single HfO_2 and Al_2O_3 dielectrics show positive V_{FB} which indicates presence of negative charges in the films. Oxygen interstitial defects in dielectric oxide films generated during the ALD process are known to be negatively charged and could possibly be the reason for high fixed negative charges in the film [6]. A high negative V_{FB} is then observed for A/B/A/B type Al_2O_3/HfO_2 stacks. The nano laminate stacks with mild intermixing/doping at the interface of Al_2O_3/HfO_2 generate more positive Al and Hf interstitial causing V_{FB} shifts in the negative direction. It was presumed that the V_{FB} shift is largely controlled by interfacial trap charges. To solve the large V_{FB} shift issue an interfacial SiO_xN_y layer was introduced on the SiC surface before deposition of multilayer stacks. As a result, a significant recovery in V_{FB} was observed, as shown in Fig 4. The V_{FB} tuning process demonstrated here is an important step towards implementation of high-k gate stacks on SiC substrate.

The interface state density is extracted using Hill–Coleman conductance method [7,8]

$$D_{it} = \frac{2}{qA}\frac{G_{m,max}/\omega}{\left(\frac{G_{m,max}}{\omega C_{di}}\right)^2 + \left(1 - \frac{C_m}{C_{di}}\right)^2} \quad (2)$$

where $G_{m,max}$ is the peak conductance value, C_m the corresponding capacitance at the peak gate bias, and C_{di} is dielectric capacitance at accumulation. Fig. 5 shows the G_g-V_g charateristics of different dilectric stacks used to extract interface traps.

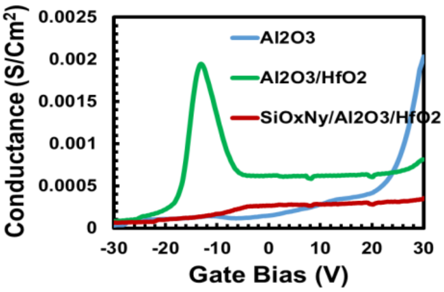

Fig.5. Gate conductance versus voltage characteristics of MOS capacitor measured at 100KHz

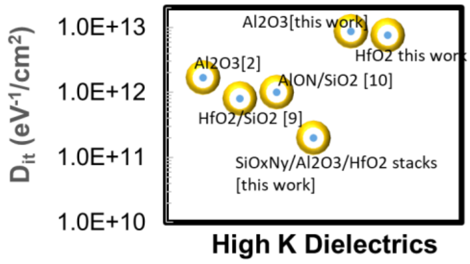

Fig. 6. Comparison of interface state density (D_{it}) with published data. This work reports the lowest D_{it} value among high-k stacks.

The interface state density extracted using equation (2) from the measured values of capacitance and conductance for different high-K stacks are compared with other reported results and illustrated in Fig. 6. The SiO_xN_y interfacial layer with Al_2O_3/HfO_2 laminate is effective to reduce D_{it} to 3×10^{11}/eVcm^2, which is an order of magnitude lower than D_{it} values previously reported on high-K [7-11] and other gate stacks in this work.

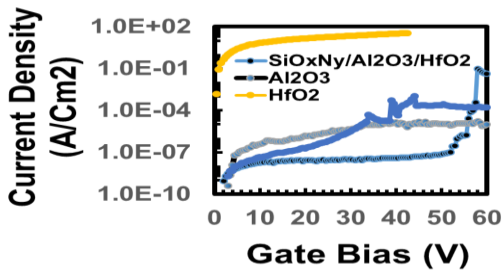

Fig.7. Jg–Vg characteristics of high-K gate stacks on 4H-SiC at 300K

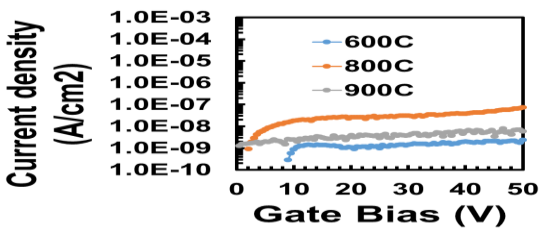

Fig. 8. Jg-Vg characteristics of $SiO_xN_y/Al_2O_3/HfO_2$ gate stacks at 300K after post deposition anneal in N_2 at 600 to 900ºC.

Fig. 7 shows the Jg-Vg characteristics of different gate stacks measured under accumulation. Low gate leakage current density of 0.1µA/cm^2 at V_G = 50V demonstrates high gate dielectric integrity. The breakdown field of stacked gate dielectrics on 4H-SiC is 10.0 MV/cm. The thermal stability of $SiO_xN_y/Al_2O_3/HfO_2$ gate stack was investigated by post deposition rapid thermal anneal in N_2. It was found that the gate stack is fully stable up to 800ºC with slight degradation of flat band voltage (V_{FB}) at 900ºC probably due to the localized crystalization of HfO_2 as seen in TEM. No gate leakage current degradation was observed after post deposition high temperature annealing (Fig. 8), demonstrating robust thermal stability against high-temperature RTA.

Summary

The effect of ultrathin SiO_xN_y interfacial layer with multi stack nanolaminated HfO_2/Al_2O_3 films and standalone Al_2O_3 and HfO_2 gate stacks were systematically investigated. Excellent thermal stability was observed for the multilayer nano laminated film. The interfacial oxynitride film is effective to reduce D_{it} to 3×10^{11}/eVcm^2 and tuning of V_{FB}.. In summary, we developed multi-layered high-K gate stack technology with tuneable V_{FB} and low D_{it} for high-performance SiC power MOSFETs.

*This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research) Singapore, under Grant No. A20H9a0242.

References

[1] N. S. Saks, S. S. Mani, and A. K. Agarwal, Appl. Phys. Lett. 76, 2250(2000).

[2] L. A. Lipkin and J. W. Palmour, IEEE Trans Electron Dev. Vol. 46, No. 3, 525 (1999).

[3] T. Hosoi, S. Azumo, Y. Kashiwagi, S. Hosaka, K. Yamamoto, M. Aketa, H. Asahara, T. Nakamura, T. Kimoto, and T. Shimura, Japanese J. of Applied Physics 59, 021001 (2020).

[4] Hironori Yoshioka, Masashi Yamazaki and Shinsuke Harada, Aip Advances 6, 105206 (2016).

[5] K. Piskorski and H. M. Przewlocki, MIPRO 2010: 33rd International Convention on Information and Communication Technology, Electronics and Microelectronics, p.63

[6] K. Matsunaga, T. Tanaka, T. Yamamoto, Y. Ikuhara, Physical Rev B, vol. 68, 085110, (2003).

[7] W. A. Hill and C. C. Coleman, Solid-State Electron, vol. 23, p. 987 (1980).

[8] V. Kumar, N. Kaminski, A Singh Maan , and J. Akhtar, Physica Status Solidi (A) 1–10 (2015).

[9] Y. Wu, S. Wang, Y. Xuan, T. Shen, Peide D. Ye, J. A. Cooper Jr., ISDRS 2007, December 12-14, 2007, College Park, MD, USA.

[10] K. Y. Cheong, J. H. Moon, T. J. Park, J. H. Kim, C. S. Hwang, H. J. Kim, W. Bahng, and N. K. Kim, IEEE Trans Electron Dev. Vol. 54, No. 12, 3409 (2007).

[11] T. Hosoi, S. Azumo,Y. Kashiwagi, S. Hosaka,R. Nakamura,S. Mitani,Y. Nakano,H. Asahara,T. Nakamura, T. Kimoto, T. Shimura and H. Watanabe, 2012 International Electron Devices Meeting, p. 15