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# Electrothermal Modelling and Measurements of Parallel-Connected VTH Mismatched SiC MOSFETs under Inductive Load Switching

Simon Mendy[1,a], Ruizhu Wu[1,b], Jose Ortiz Gonzalez[1,c], Olayiwola Alatise[1, d]

[1]School of Engineering, University of Warwick, Coventry, United Kingdom

[a]s.mendy@warwick.ac.uk, [b]robert.wu.1@warwick.ac.uk, [c]j.a.ortiz-gonzalez@warwick.ac.uk, [d]o.alatise@warwick.ac.uk

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**Abstract** In high current applications that use several parallel-connected SiC MOSFETs (e.g., automotive traction inverters), optimal current sharing is integral to overall system reliability. Threshold voltage ($V_{TH}$) variation in SiC MOSFETs is a prevalent reliability issue that can cause a current mismatch in parallel-connected devices. Using experimental measurements and compact modelling, a technique has been developed to characterise $V_{TH}$ variation's impact in up to 8 parallel-connected SiC MOSFETs (self-imposed limit). This model can predict the allowable $V_{TH}$ variation for optimal current sharing. It can also be used to evaluate the impact of other parameters, including gate driver synchronisation, on current sharing in parallel devices.

## Introduction

This paper investigates the impact of $V_{TH}$ variation on several parallel (up to 8 – self-imposed limit – the range can be extended to 10s of devices) SiC MOSFETs. The role of parameter variation in the short circuit performance of parallel devices has been investigated in [1,2,3] and unclamped inductive switching [4,5]. Due to the inherent variability of $V_{TH}$ in SiC MOSFETs, it is essential to select devices with minimal $V_{TH}$ variation to avoid unbalanced current sharing and unsynchronised switching between devices [6]. Hence, diagnostic modelling tools that can predict the impact of parameter mismatch on current sharing are required. [7] presents a parallel model, but it does not specify how many parallel devices the model can simulate and does not explore the role of VTH mismatch between devices. They propose adjustment of the gate resistance to solve the inconsistent switching characteristics of parallel devices. [8] investigates the effect of mismatches between device characteristics and circuit components of paralleled SiC MOSFETs. The plots shown bear a close resemblance to the Vth mismatch of up to 8 devices illustrated further in this paper. The DUT with the lower $V_{TH}$ turns ON faster and turns OFF slower. The model, however, is not electrothermal and does not explore the temperature effects of $V_{TH}$ mismatch on current sharing specifically for multiple paralleled DUTs and a long duration of repetitive switching. [9] suggests an active gate driving method to mitigate the current sharing performance caused by mismatched $V_{TH}$. This is a viable solution but adds more complexity to driving paralleled devices.

While design engineers have traditionally used SPICE based models as diagnostic tools, their application depends on model availability and ease of parameter tuning. This study presents a state-space model derived from parallel-connected MOSFET equivalent circuits that include all parasitic capacitances and inductances [10]. Device datasheets are used to parameterise the model extensively. Unavailable parameters are extracted by curve fittings of the output characteristics from the device datasheet to produce the equation for channel current. The model is temperature-dependent since it incorporates the temperature dependency of $V_{TH}$ and device transconductance. The transient thermal impedance extracted from the datasheet is used to create the thermal network that couples with the electrical parameters.

## Model Development and Results

The circuit used to derive the equations for the model is shown in Fig. 1. In the experiments, the PCB tracks are designed to be the same length to mitigate mismatch in parasitics ($R_S$, $R_D$, $L_G$, $L_S$, and $L_D$) and resulting transients. The channel current, $I_{chi}$ of the SiC MOSFETs, is modelled from datasheet output characteristics graphs using fitted equations related to the gate overdrive voltage ($V_{GS}$–$V_{TH}$) and temperature T (see Eq. 1) [11]. The physical constants K and α are extracted using the curve fitting tool in MATLAB and are made overdrive voltage- and temperature-dependent. The material constant, K, contains μ, which is overdrive voltage and temperature-dependent [12]. In addition, α is overdrive voltage-dependent and temperature-dependent since it is a function of $V_{TH}$.

$$I_{chi} = \mathrm{K}_i\left[(V_{GSi} - V_{THi})V_{DSi} - (1+\alpha_i)\frac{V_{DSi}^2}{2}\right](1+\lambda V_{DSi}) \qquad V_{GS} \geq V_{TH} \text{ and } V_{DS} < \frac{(V_{GS}-V_{TH})}{(1+\alpha)} \qquad (1a)$$

$$I_{chi} = \frac{\mathrm{K}_i}{2(1+\alpha)}(V_{GSi} - V_{THi})^2(1+\lambda V_{DSi}) \qquad V_{GS} \geq V_{TH} \text{ and } V_{DS} \geq \frac{(V_{GS}-V_{TH})}{(1+\alpha)} \qquad (1b)$$

From Fig. 1, the following equations (Eq. 2 – Eq. 5) are derived, then converted into state-space form according to Eq. 10 and modelled in MATLAB Simulink using the State-Space block.

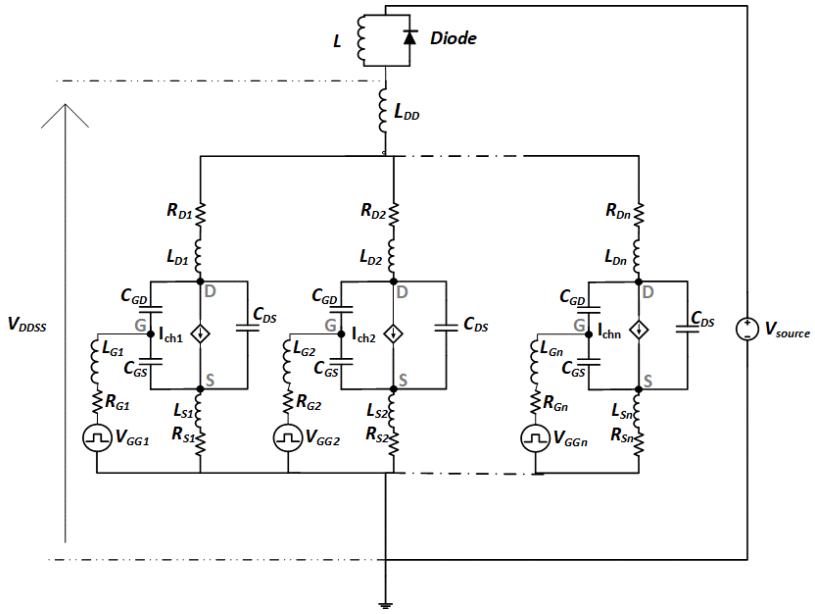


Fig. 1. The circuit diagram of MOSFET 1, MOSFET 2, to MOSFET n, connected in parallel, which is used to produce the model.

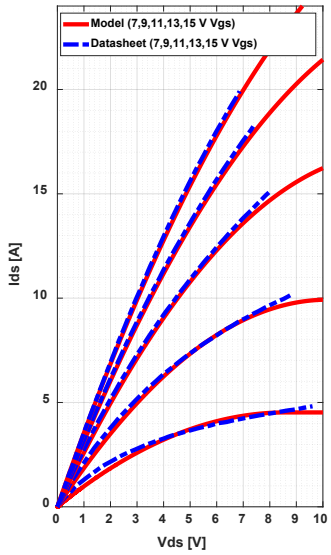


Fig. 2. Output characteristics of the model compared to the datasheet at Tj = 25°C.

$$(L_{Di}+L_{Si})\frac{di_{Si}}{dt} - L_{Di}\frac{di_{Gi}}{dt} + (L_{DDSS})\sum_{i=1}^{n}\frac{di_{Si}}{dt} - (L_{DDSS})\frac{di_{Gi}}{dt} + V_{DSi} + i_{Si}(R_S+R_D) - i_{Gi}R_D = V_{source} \qquad (2)$$

$$R_{Gi}i_{Gi} + R_S i_{Si} + L_{Gi}\frac{di_{Gi}}{dt} + L_{Si}\frac{di_{Si}}{dt} + V_{GSi} = V_{GGi} \qquad (3)$$

$$C_{GS}\frac{dV_{GSi}}{dt} - C_{GD}\frac{dV_{DGi}}{dt} - i_{Gi} = 0 \qquad (4)$$

$$(C_{GS}+C_{DS})\frac{dV_{GSi}}{dt} + C_{DS}\frac{dV_{DGi}}{dt} - i_{Si} = -I_{chi} \qquad (5)$$

$$V_{source} - V_{Diode} = V_{DDSS} \qquad (6)$$

$$\sum_{i=1}^{n} i_{Di} = i_L - i_{Diode} \qquad (7)$$

$$\dot{x} = Ax + Bu \qquad (8)$$

Key: $i$ is the leg number, from left to right according to Fig. 1, and $n$ is the total number of devices connected in parallel. The inputs of the model are $V_{source}$, $V_{GGi}$, and -$I_{chi}$.

The model is verified by reproducing the output characteristics of the datasheet, as shown in Fig. 3. Fig. 3 shows the model switching test results compared to experimental results of the same parameters for a total load current of 8 A. The experimental measurement was obtained using a double-pulse test setup [13], with two devices in parallel ($V_{TH1}$ = 2.541 and $V_{TH2}$ = 3.013). The DC-link voltage was 200 V, and the total load current was 8A. The currents were measured using Rogowski coils current probes.

A $V_{TH}$ difference of 1 V, as shown by the plots in Fig. 4 from the model, does not produce much difference in current sharing between DUTs for four and eight parallel-connected devices when the gate signals are synchronous. In Fig. 4, one can observe that configurations with more parallel devices show longer turn-ON and turn-OFF switching times and more differences in the switching delay during turn-ON and turn-OFF between the DUTs, as expected.

The switching time difference created by a $V_{TH}$ difference of any magnitude can be computed using Eq. 9 [11]. For the C3M0280090D SiC MOSFET, the input capacitance, $C_{iss,}$ is 150 pF, the gate resistance used (internal + external) is 176 Ω, and the gate voltage, $V_{GG,}$ is 17 V.

$$\Delta t_{mismatch} = R_G C_{iss} \ln\left(\frac{V_{GG} - V_{TH1}}{V_{GG} - V_{TH2}}\right) \tag{9}$$

*Note: Eq. 9 is an aid for simplifying explanations for the reader. The $\Delta t_{mismatch}$ can be obtained directly from this presented model, which also accounts for the influence of parasitic inductances in the gate loop.*

Applying Eq. 9 for $V_{TH1}$ = 2.5 V and $V_{TH2}$ = 3.5 V gives a switching time difference of 1.87 ns. From observation and consideration, for ideally in-sync gate drivers, as modelled, the time difference calculated above should hold independent of the number of devices are paralleled.

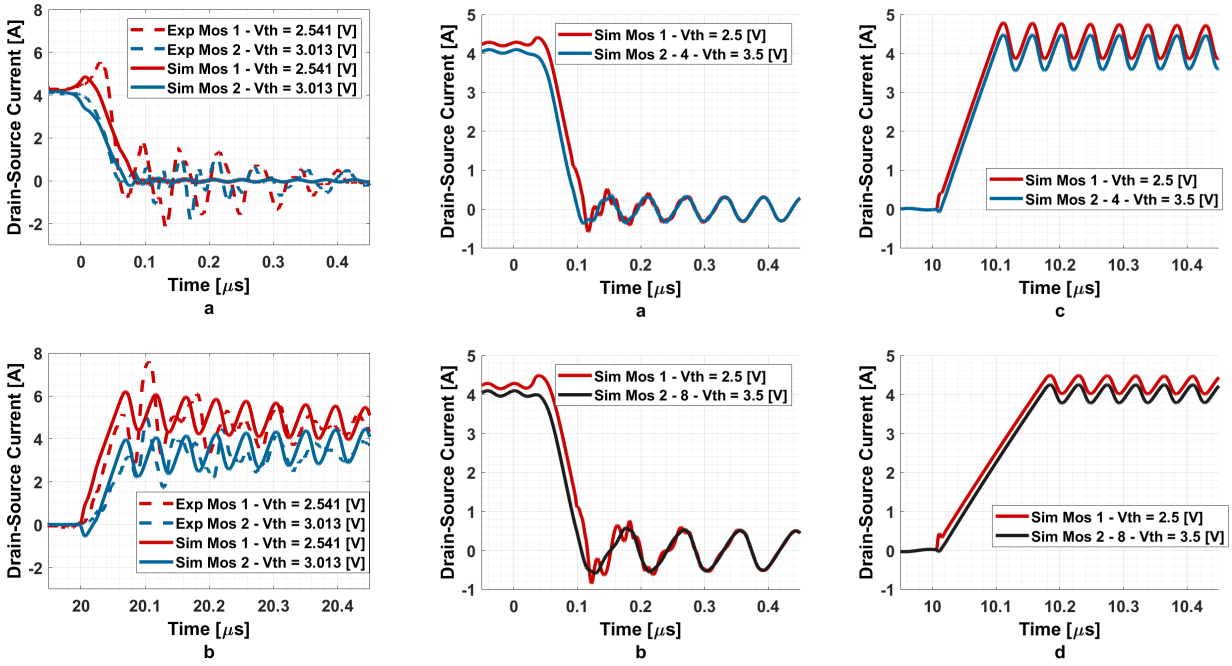


Fig. 3. (a) Turn-OFF and (b) Turn-ON $I_{DS}$ plots from the experiment and model. $V_{GG}$ = 17 V, and the synchronisation mismatch between the gate signals of the DUTs is included in the model.

Fig. 4. (a) and (b) – Turn-OFF for 4 and 8 paralleled DUTs, respectively. (c) and (d) – Turn-ON for 4 and 8 paralleled DUTs, respectively. 1 V mismatch in $V_{TH}$ for four devices in parallel conducting 16 A total load current, and eight devices in parallel conducting 32 A total load current. The $V_{GG}$ signals for these simulation results are synchronised.

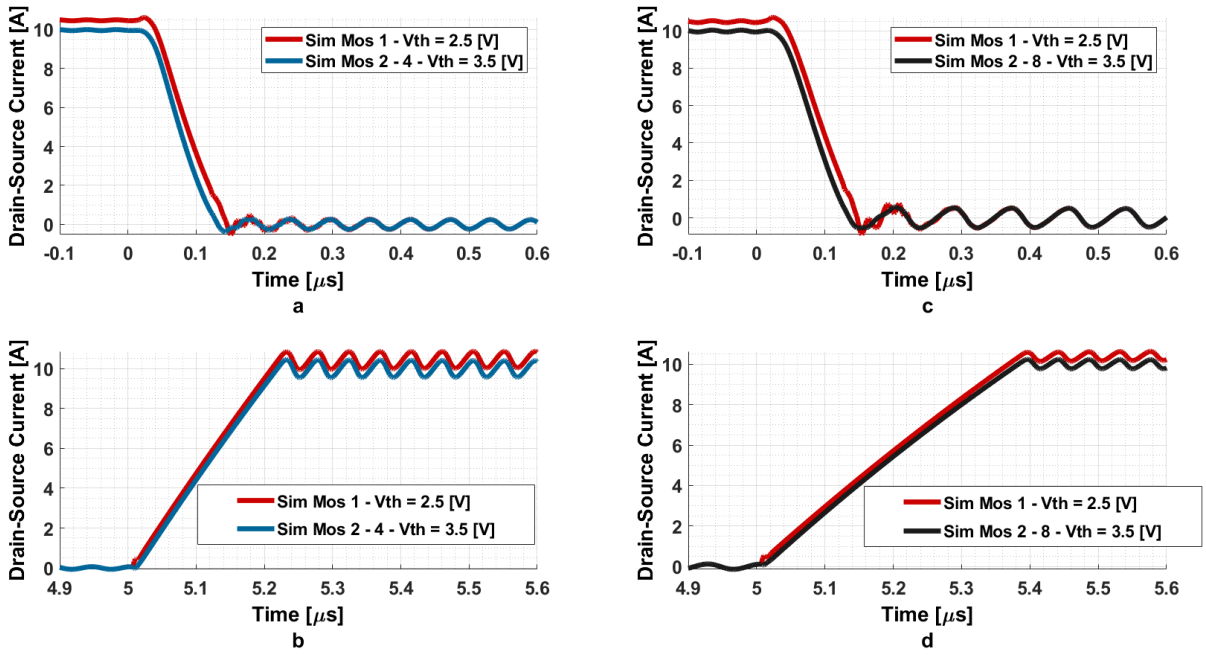


Fig. 5. Turn-OFF ((a) and (c)) and Turn-ON ((b) and (d)) $I_{DS}$ simulation plots showing the current commutation between devices for higher current (~10 A per DUT) – device rating is 11.5 A (C3M0280090D). One of the DUTs is set at 1 V lower $V_{TH}$.

*Note: some of the colours are not visible in the plots because of overlapping lines. To limit the size of the legend, one colour has been used to specify all the lines that overlap due to identical behaviour.*

A delay due to *a* $V_{TH}$ mismatch of 0 to 2 V will correspond to a minimal period- approximately 1-3 ns (calculated as 1.87 ns for the DUTs tested and modelled above). For a short period of 1-3 ns, the current rise or fall of unsynchronised DUTs will be minimal and would therefore not cause much disparity of current sharing.

A serious reliability issue can arise when $V_{TH}$ mismatch is combined with gate driver un-synchronisation. Both these combined could produce a switching difference of more than 10 ns. For switching time difference >10 ns, a device turning on too early or turning off slightly later will temporarily conduct a significant proportion of the total current through the branch of the parallel devices being measured, as demonstrated in Fig. 6. More devices in parallel mean a total load current which is likely to be much higher than the current rating of one FET. Hence, more current would be conducted by the one device that switches, either too early during turn-ON or too late during turn-OFF, if the shift of the unsynchronised gate signal is negative or positive, respectively. For repetitive switching this could lead to the failure of the mismatched DUT. One device of a paralleled branch failing would then trigger a cascading failure effect of the whole branch because more power gets dissipated by the remaining FETs of the branch, leading to higher junction temperatures for each remaining FET. Therefore, gate synchronisation becomes the main concern to ensure the reliability of branches of parallel-connected SiC MOSFETs under inductive load (unless if the devices switch slowly due to high gate resistance or high input capacitance), especially when the branch is configured of many paralleled devices (10s of SiC MOSFETs).

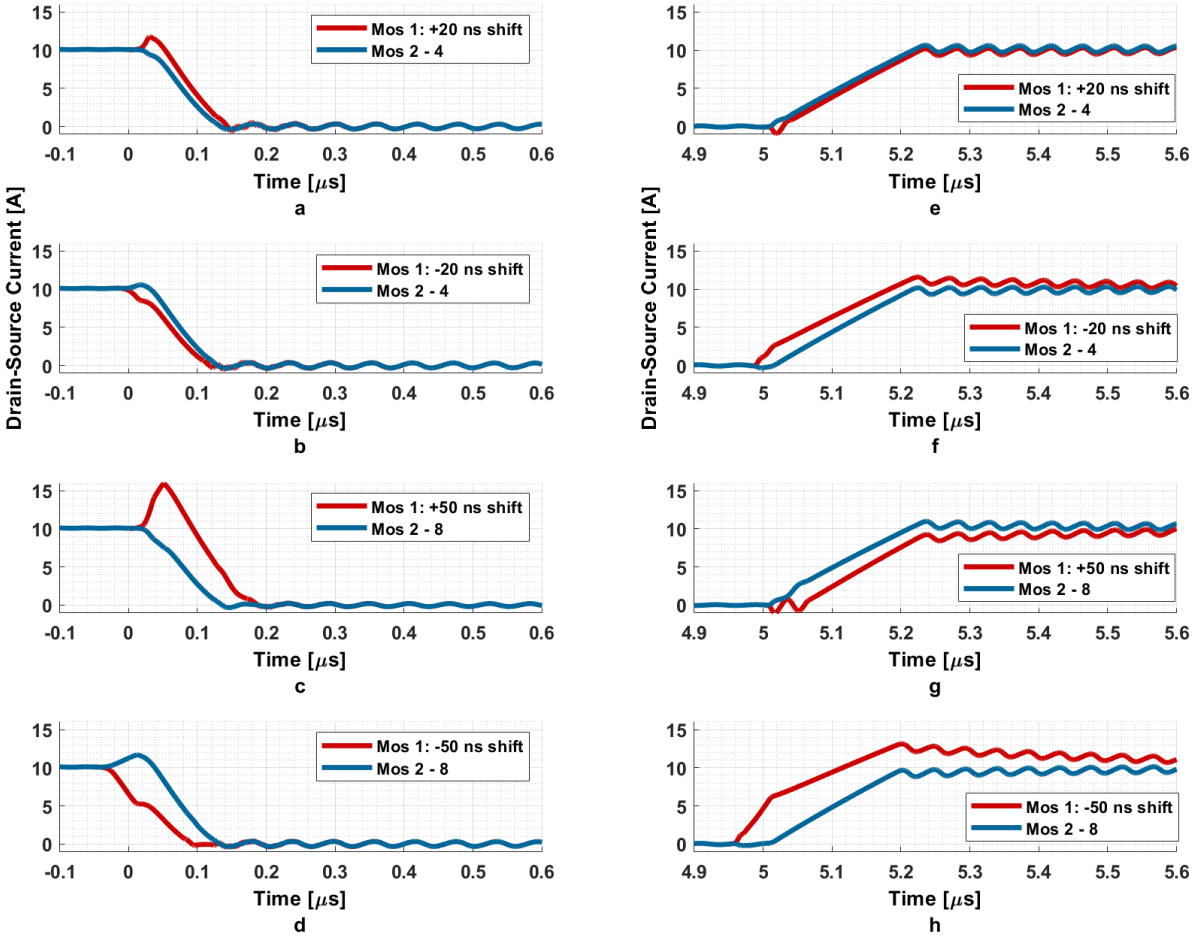


Fig. 6. The turn-OFF (a-d) and turn-ON (e-h) $I_{DS}$ simulation plots of 4 parallel-connected DUTs, where 1 DUT is shifted by either 20 ns or 50 ns to produce unsynchronised gate switching of the branch.

## Conclusion

This paper presents an accurate model for predicting the current sharing of parallel-connected MOSFETs under inductive load. The model can account for $V_{TH}$ and gate drive signal mismatch between parallel devices. A comparison of experimental and simulation results with 1 V $V_{TH}$ difference and unsynchronised gate signals is used to verify the model. Further simulations show that 1 V $V_{TH}$ mismatch with perfect gate synchronisation does not cause much difference in current sharing between groups of four and eight parallel-connected of the MOSFETs tested for this paper. It is not a reliability concern due to the insignificant switching time difference caused by the $V_{TH}$ mismatch. However, $V_{TH}$ mismatch combined with gate un-synchronisation could produce a greater than 10 ns mismatch. As the total current far exceeds the rating of a single MOSFET (more parallel DUTs), 10 ns or more gate driver pulse mismatch can cause one DUT to conduct current beyond its limit, leading to a subsequent device and branch failure.

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