

Advanced 1200V SiC MOSFET Concept Based on Singular Point Source MOS (S-MOS) Technology

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Abstract. This paper presents a Singular Point Source MOS (S-MOS) cell concept suitable for SiC MOSFETs targeting low conduction losses, low switching losses and high robustness. The S-MOS concept differs from standard Planar or Trench MOS cells in the manner by which the total channel width per device area is determined. For the proof of concept and device electrical performance evaluation, the paper will provide 2D and 3D TCAD simulations results for 1200 V SiC MOSFETs including the S-MOS and reference planar and trench structures.

Introduction

MOS cell process and design platforms were developed over the years for enabling advanced power devices such as the power MOSFET and IGBT. These devices employ either planar or trench gate MOS cell concepts arranged in cellular or linear layout designs. The advances made on Silicon based MOS devices have provided a strong base for developing SiC power MOSFETs [1] where higher cell packing densities through cell miniaturisation is essential. Therefore, in recent years advanced 3D design concepts similar to the low voltage lateral FINFET [2] have been proposed for improving the device static and dynamic characteristics [3][4]. 3D solutions rely on multi-dimensional channel arrangements to increase the cell packing densities for lower R_{dson} values.

Following the above trend, a new 3D MOS concept referred to as the “Singular point source” (S-MOS) was presented recently and demonstrated using 3D-TCAD simulations for a 1200 V Silicon IGBT structure [5]. In this paper, the S-MOS concept was adapted and implemented on a 1200 V SiC MOSFET structure by means of 3D-TCAD simulations using Silvaco Victory Process and Device Software. A full set of static and dynamic results are presented for comparing the S-MOS with reference SiC MOSFET 2D structures employing Planar and Trench MOS cell designs.

Device Concept and Structure

For planar or trench MOS cells as shown in Fig. 1a and Fig 1b respectively, the channel width W_{ch} is defined as the total peripheral distance around the N++ source which also depend on the geometrical shape of the MOS cells arrangement (i.e., linear or cellular layout design) [6]. On the other hand, the channel width W_{ch} for the S-MOS concept shown in Fig. 1c is defined by a small-scale dimension of the N++ source and P_{Channel} junction W_{PNJ} length. By positioning this small geometrical feature on a trench side-wall, a predetermined unit channel length W_{chn} is provided. Fig. 1 highlights the critical cell dimensions for all designs along with a 2D top view descriptive cross section. For the S-MOS, a cross section at the trench side-wall along the outline A-A' is also depicted. The S-MOS trenches are positioned orthogonally to the source contact stripe while vertical trench channels are prevented from forming on the inner trench side-walls by extending a highly doped P++ region under the N++ source. Therefore, the S-MOS provides only a singular point source reference for defining W_{chn} as in the top view (i.e., not a line as for reference planar or trench MOS cells). From this singular point, the junction depth W_{PNJ} is defined after implantation and annealing of the N++ source and P_{Channel} regions. Despite the lack of diffusion mechanism in SiC compared to Silicon, we can still obtain a W_{PNJ} in the range of 100-200 nm. By approximating

the shape of the $N^{++}/P_{\text{Channel}}$ junction to a “quarter of a circle”, a W_{chn} around 150-300 nm could be reached for a single trench side-wall. W_{chn} is practically slightly longer if calculated at the P_{Channel} peak doping position which is deeper than W_{PNJ} . The total W_{ch} for a given chip is the sum of all W_{chn} on all trench side-walls. This is adequate when implementing small mesa dimensions and different design variants. Based on this approach, the singular point source will allow more cell packing with miniaturised cell dimensions in future designs to increase the channel density in the third dimension and thus reduce the on-state conduction losses of the device.

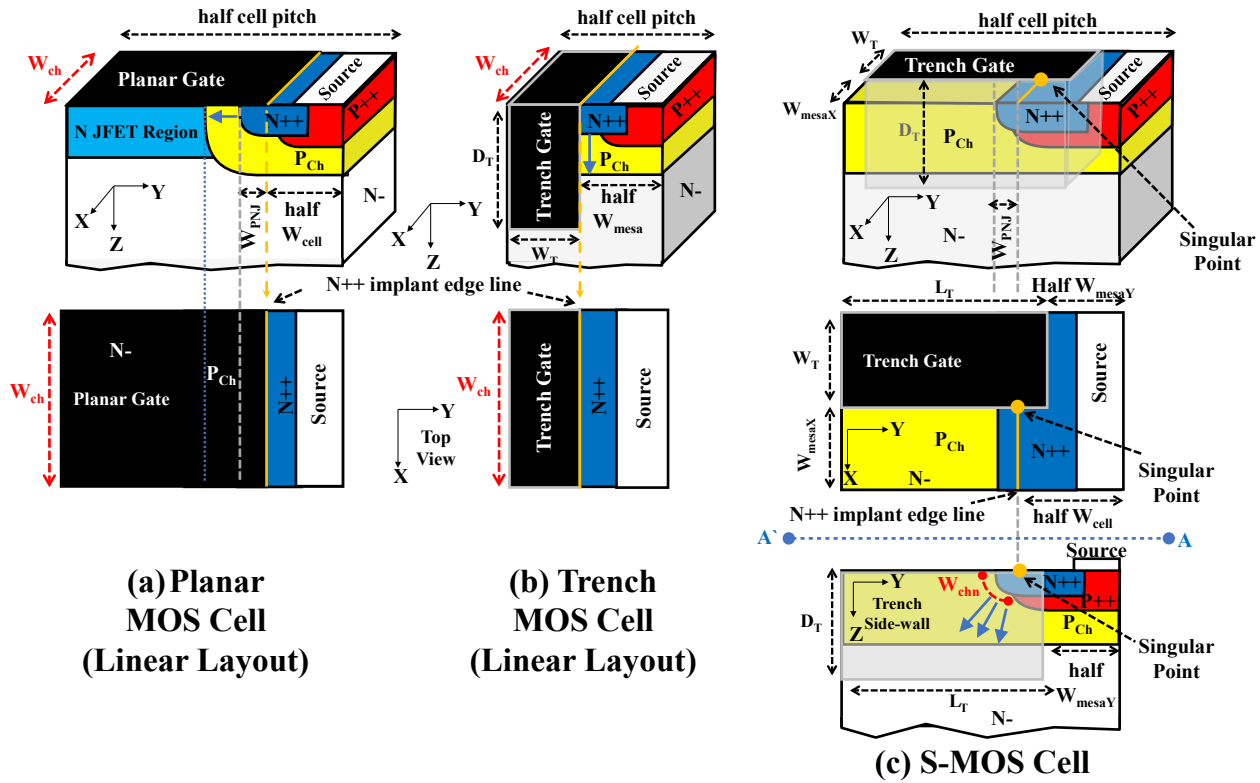


Fig. 1 Source MOS cell concepts including planar MOS (a), Trench MOS (b) and S-MOS (c). Blue arrows at N⁺⁺ source represent the channel path (S-MOS cell does not require a JFET region).

1200V SiC MOSFET Simulation Models

The 1200 V S-MOS SiC MOSFET functionality was demonstrated using 3D-TCAD simulations and compared to reference 2D planar and trench models using linear cell layout designs. For this investigation, 3x S-MOS variants, 2x trench MOS variants and 1x planar MOS variant with a JFET region were modelled with different pitch widths as outlined in Table (1) along with other key dimensions. The new design can be realized using standard manufacturing processes since the W_{mesaY} can be defined with modern processing capabilities while W_{mesaX} contain no central feature (i.e., contact) to limit the design window. No P-regions were employed at trench bottom corners for these simulations. All devices had a total thickness = 10 μm , N- drift doping = $8 \times 10^{15} / \text{cm}^3$, N⁺⁺ drain depth = 1 μm and maximum doping = $1 \times 10^{20} / \text{cm}^3$. All trenches had a width $W_{\text{T}} = 0.8 \mu\text{m}$ and depth $D_{\text{T}} = 0.9 \mu\text{m}$ and the gate oxide thickness = 50 nm. The P_{Channel} doping profile was adjusted to obtain the required saturation current and blocking capability. The doping concentration for the N⁺⁺ source and P⁺⁺ base = $1 \times 10^{20} / \text{cm}^3$ and $5 \times 10^{19} / \text{cm}^3$ respectively.

Different field mobility models were available leading to different static performance with respect to the R_{dson} and threshold voltage V_{th} . The selected model “fldmob” for all devices led to R_{dson} values close to the expected performance albeit with high V_{th} levels. Nevertheless, a qualitative assessment of the S-MOS compared to reference devices was achieved. It is important to note that a planar design can be designed with smaller dimensions using cellular layout designs to achieve even lower conduction losses than what was achieved with the presented simulation results.

Table 1 Critical MOS cell dimension for the different simulation models.

Table (1)		S-MOS(A)	S-MOS(B)	S-MOS(C)	Trench(A)	Trench(B)	Planar
Pitch	μm	1.6	2.4	4	1.6	2	6
W_{cell}	μm	1	1.6	1.6			1.8
W_{mesa}	μm				0.8	1.2	
W_{mesaX}	μm	0.2	0.2	0.2			
W_{mesaY}	μm	0.8	1	1			
L_T	μm	0.4	0.7	1.5			

Results and Discussion

Static and mixed mode inductive load dynamic simulations were carried for all device structures which were scaled for a total active area of 1 cm^2 . All reference and S-MOS structures had avalanche blocking around 1400 V and threshold voltage levels were $> 7 \text{ V}$ at 150°C . The V_{th} values were obviously too high compared to real devices. The output IV characteristics are shown in Fig. 2 up to 600 V and a zoom-in up to 1 V at $V_{\text{gs}}=15 \text{ V}$ and 150°C . All S-MOS versions provide low R_{dson} levels similar to trench cells around $3 \Omega\text{ohm-cm}^2$ at. In addition, the S-MOS provides a flat saturation current compared to reference models. The increasing saturation current is normally linked to short channel effects for the reference planar and trench structures. Therefore, the S-MOS behaviour requires more study to understand the effect of the new cell concept. Fig. 3 show the S-MOS (A) net doping and electron concentration at 100 A/cm^2 highlighting the device conduction mode as described above. The figure also shows that the P++ base region placed under the N++ source ensures no vertical inversion channel forms on the inner trench walls as explained earlier.

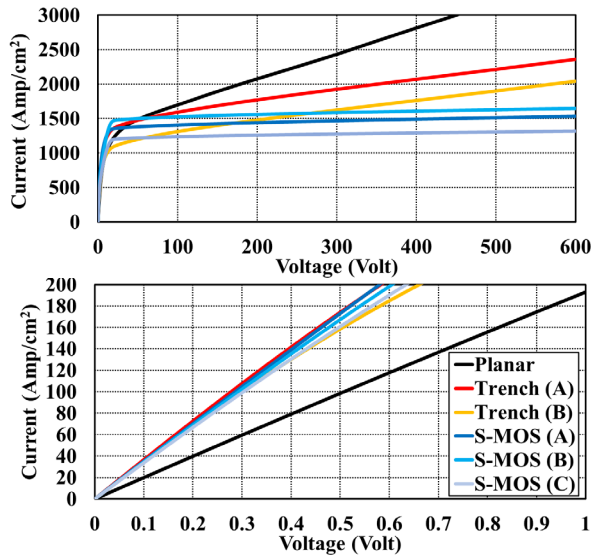


Fig. 2 1200 V SiC MOSFET output curves, $V_{\text{gs}} = 15 \text{ V}$, 150°C .

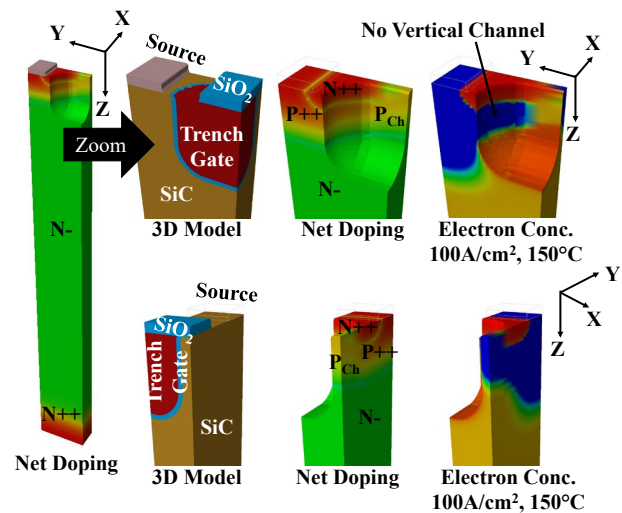


Fig. 3 S-MOS (A) 3D model showing device sections, corresponding net doping and electron concentration.

The inductive switching behaviour is shown in Fig. 4 for nominal conditions (600 V , 100 A/cm^2 , 150°C , stray inductance = 50 nH , $V_{\text{gs}} = 0 \text{ V}$ - 15 V). The turn-on di/dt was set at similar levels with different gate resistors. The faster dv/dt levels for the S-MOS led to lower E_{on} losses at lower di/dt than for reference devices as shown in Fig. 5. All devices show turn-off losses E_{off} around $2\text{-}3 \text{ mJ}$. The S-MOS provides lower overall losses compared to reference devices as shown in Table (2).

Finally, the short circuit current was simulated for all devices at 150°C . Fig. 6 shows the S-MOS(C) short circuit current and voltage waveforms and the corresponding net doping and total current density at maximum short circuit current. The figure illustrates the positioning of the

channel on the trench side-wall and the fact that the only available W_{chn} for the S-MOS concept is located in that space. This approach could be the basis for providing new designs having less short channel effects and improved trade-off between conduction losses and short circuit performance and try to mitigate some of the short circuit related limitations associated with SiC MOSFETs.

Table 2 Static and dynamic losses for all devices at 150 °C under comparable switching conditions.

Table (2)		S-MOS(A)	S-MOS(B)	S-MOS(C)	Trench(A)	Trench(B)	Planar
R_{dson}	$\text{m}\Omega\text{-cm}^2$	2.8	2.9	3	2.7	3	5
E_{sw}	mJ	12.07	15.20	17.22	20.11	18.28	15.93

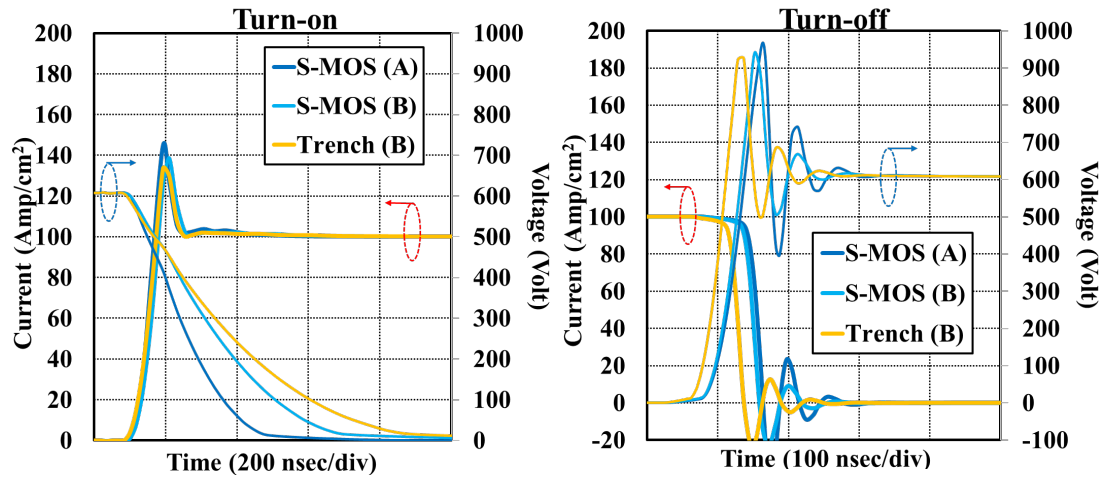


Fig. 4 1200 V SiC MOSFET nominal switching curves (150 °C).

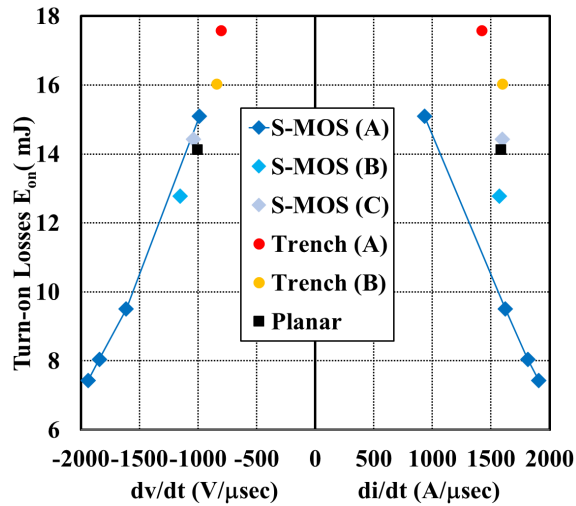


Fig. 5 E_{on} vs. di/dt and dv/dt (150 °C).

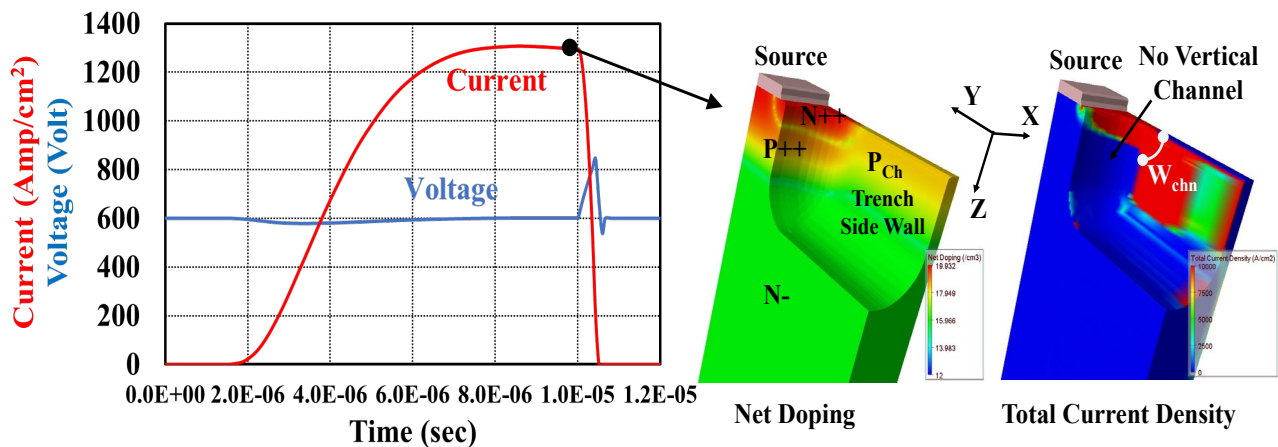


Fig. 6 1200 V S-MOS(C) SiC MOSFET Short Circuit at 150 °C and corresponding net doping for reference and total current density at maximum short circuit current at the indicated point on the current waveform.

Summary

A new SiC MOSFET based on the S-MOS cell concept was presented showing an alternative method to define and control the device channel width. 3D-TCAD simulation results confirm the functionality of the S-MOS concept compared to reference planar and trench SiC MOSFETs rated at 1200 V. Design optimization is now required since the performance shows promising behaviour.

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