

Advances in 200 mm 4H SiC Wafer Development and Production

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Abstract. 200 mm diameter n-type 4H SiC wafers were produced from bulk crystals grown using a physical vapor transport (PVT) method. The configuration of the growth cell was modified to both allow for the growth of larger crystals with respect to the standard 150 mm process, and to induce a thermal environment necessary to increase the mass deposition rate. A 25% increase in deposition rate was achieved relative to the standard process. The resulting wafers exhibited resistivity uniformity comparable to commercial 150 mm product. Optical and x-ray techniques were used to evaluate wafer quality, and revealed surface and bulk crystal defect densities acceptable for epilayer growth.

Introduction

The recent surge in the electric vehicle market, driven in part by ramped exhaust regulations [1], continues to increase demand for power modules capable of high-temperature operation. This in turn has applied pressure on device manufacturers to improve throughput, and to seek ways of reducing production costs. One proven cost reduction method is to expand the surface area of the 4H SiC wafers typically used as device substrates. [2] Building on prior development of 4H SiC bulk crystal growth and processing methods to increase wafer diameter, [3] SK siltron css has committed to developing the next tier of power electronics substrates.

As with the effort to expand wafer diameter from 100 mm to 150 mm, the key challenge to further expanding to 200 mm is to increase the size of the bulk crystals while maintaining both throughput and crystal quality. Changes to process pressure and thermal conditions have been predicted to promote polytype switching, [4] and can lead to the generation of dislocations that are detrimental to device performance. [5] This study investigated modifications to the growth cell to both accommodate larger crystals and increase mass deposition rate, with attention to analyzing defect formation.

Experimental

A PVT method was used to grow 4H n-type SiC crystals, which were processed into wafers using grinding, slicing and polishing techniques common to the industry. The internal volume of the growth cell was modified to accommodate crystal sizes larger than those used to produce 150 mm wafers, while the mass transport rate was controlled by adjusting the thermal environment. Wafer resistivity was measured using a contact eddy current method. Surface and internal defects were imaged using a photoluminescence imaging technique (SICA 88). Macroscopic defects were assessed using full-wafer images obtained from (11 $\bar{2}$ 8) x-ray topograph reflections (Rigaku XRTMicron). Basal plane dislocation densities were qualitatively assessed using high resolution (11 $\bar{2}$ 8) reflections.

Results and Discussion

A comparison between the mean mass deposition rates recorded for the standard 150 mm and 200 mm processes is shown in Fig. 1. To achieve the necessary mass transport, the thermal driving force characteristic of PVT was increased via adjustments to the growth package configuration. A 25% increase in mean mass deposition rate relative to the standard 150 mm process was obtained, enabling further enhancements to bulk crystal size.

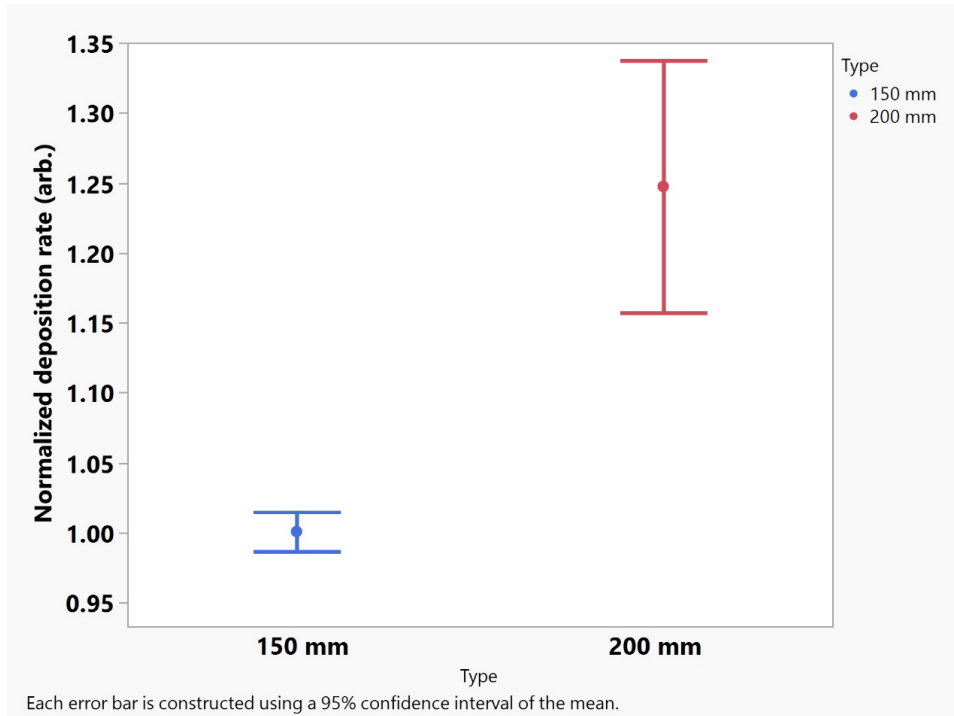


Figure 1. Mean mass deposition rate of the 200 mm process, normalized to the value obtained for the standard 150 mm process (included for reference).

Resistivity maps of typical 200 mm and 150 mm wafers selected from similar locations relative to the bulk crystal surface are shown in Fig. 2. Spatial uniformity of resistivity is important for repeatable electrical performance across device dies fabricated over the wafer surface. As shown, a high degree of uniformity has been demonstrated for 200 mm wafers in comparison with standard 150 mm material, indicating that local nitrogen uptake was not significantly affected by the larger surface area of the growth front or elevated deposition rate.

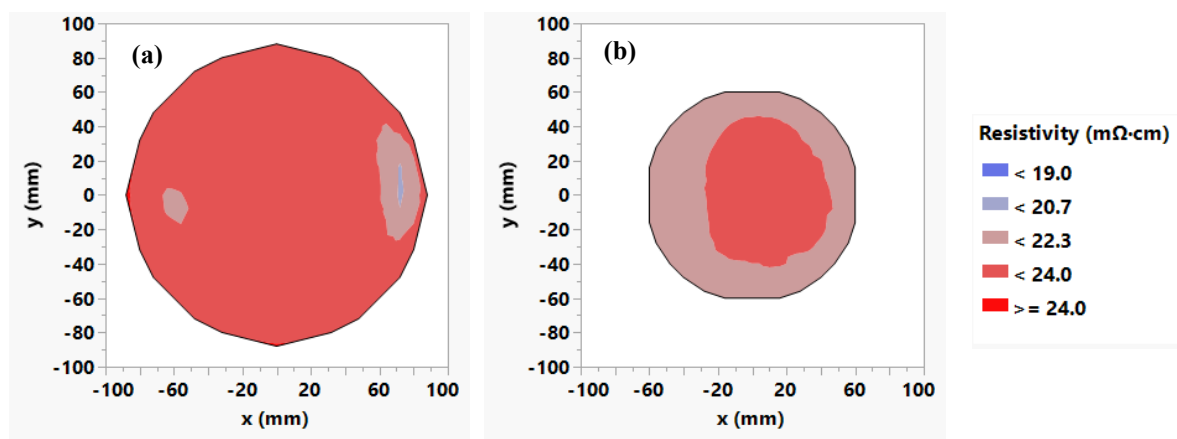


Figure 2. Representative resistivity maps of (a) a 200 mm wafer (12 mm edge exclusion); (b) a 150 mm wafer (15 mm edge exclusion).

A wafer-level defect map obtained from SICA 88 photoluminescence imaging of a representative 200 mm wafer is shown in Fig. 3. Surface and bulk crystal defects, as well as surface damage such as scratches and pits, can reduce device die yield. It was therefore important to verify that the growth process modification required to expand bulk crystal diameters did not lead to significant defect generation. Fig. 3. verifies that killer defects counts remained acceptable for epilayer growth, with the majority classified as “PL black” and “PL white” features. These features are hypothesized to be dislocation lines, decorated with dopant atoms that change the emission wavelength relative to the bulk crystal, and have no expected impact on performance. The micropipe density measured for the wafer shown in Fig. 3 was 0.36 cm^{-2} .

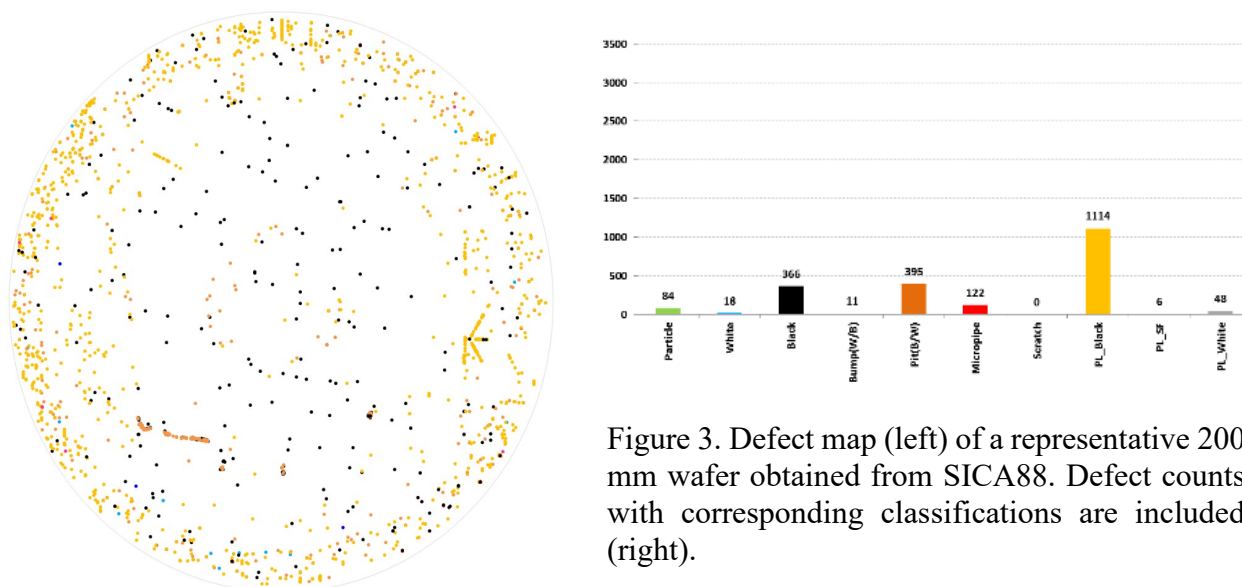


Figure 3. Defect map (left) of a representative 200 mm wafer obtained from SICA88. Defect counts with corresponding classifications are included (right).

Full-wafer $\text{Cu K}\alpha_1$ ($11\bar{2}8$) reflection scans of typical 200 mm and 150 mm wafers are compared in Fig. 4 (a) and (b). As a complement to PL characterization, XRT was performed to detect the presence of grain boundaries, micropipes and stacking faults that may have been introduced by the accelerated bulk crystal growth rate. It was found that the majority of the wafer area remained free of these defects, with grain boundaries observed near the periphery. Low micropipe and stacking fault counts were also noted. High resolution XRT scans were also performed along $16 \text{ mm} \times 72 \text{ mm}$ radial

bands from center to edge in the $[11\bar{2}0]$ direction, and the resulting images were compared with scans of 150 mm wafers selected from crystals of similar length. An example is shown in Fig. 4 (c) (200 mm wafer) and (d) (150 mm wafer) (contrast adjusted to highlight defects). The images indicate that the density of basal plane dislocations (resolved as curved line segments) of the 200 mm wafer is similar to that of the 150 mm wafer. The XRT technique is currently being refined such that dislocation densities can be accurately measured.

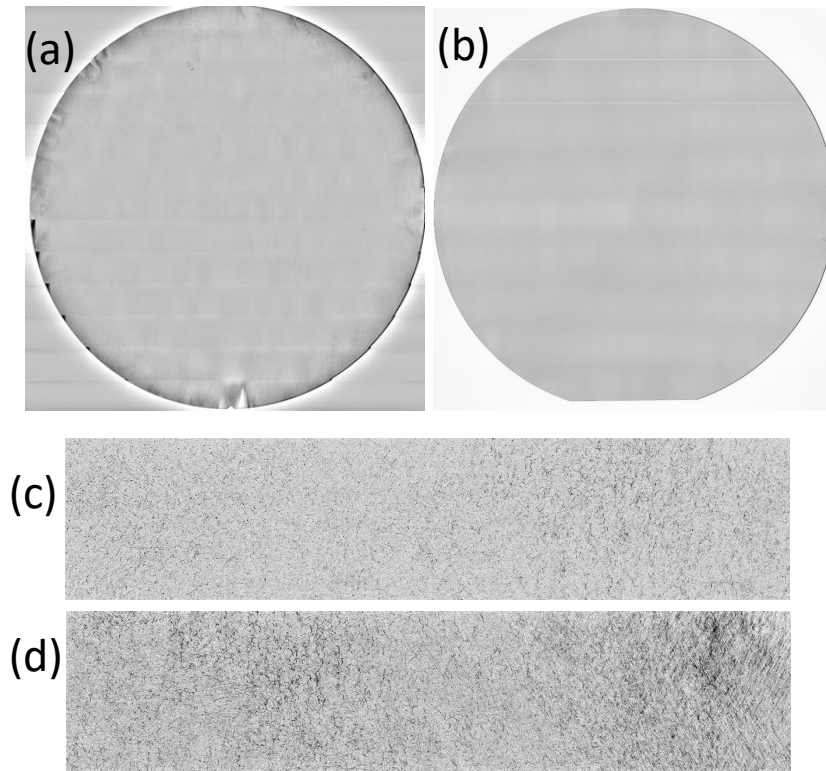


Figure 4. $\text{Cu K}\alpha_1$ ($11\bar{2}8$) reflection x-ray topograph images of (a) a representative 200 mm wafer, and (b) a representative 150 mm wafer. $16 \text{ mm} \times 72 \text{ mm}$ high-resolution images taken along the radius are shown for a (c) 200 mm and (d) 150 mm wafer.

Summary

A PVT bulk crystal growth method capable of producing epi-ready 200 mm wafers was developed. The mass deposition rate of the process was increased by 25% over the standard 150 mm process to ensure that the cycle time remained unaffected by the increase in crystal size. The resulting wafers showed low doping variation, resulting in excellent resistivity uniformity. Photoluminescence imaging and XRT revealed low densities of microscopic and macroscopic defects. Dislocation densities were qualitatively compared using high resolution XRT scans. Additional studies are required to improve edge quality.

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