

Failure Analysis of Atmospheric Neutron-Induced Single Event Burnout of a Commercial SiC MOSFET

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Abstract. Dealing with electronic devices for high reliability applications in terrestrial environments, neutron-induced Single Event Effects must be investigated. In this paper, the experimental observation of an atmospheric-like neutron-induced Single Event Burnout (SEB) on a packaged commercial SiC power MOSFET is presented after irradiation at ISIS-ChipIr. The effects of the SEB in the electrical properties of the MOSFET are established, and the SiC damaged zone is observed by scanning electron microscopy. Based on this failure analysis at the die level, the distinct stages during the SEB mechanism can be defined. The sensitive volume where the secondary particle deposited enough energy to trigger the SEB mechanism is identified and located inside the SiC n-drift epitaxial layer near the epitaxial layer/substrate junction.

Introduction

Dealing with high reliability applications in terrestrial and space environments, such as automotive, train transportation, aeronautics or space applications, the consideration of any failure source is a critical necessity. All environmental constraints must be considered, and in particular atmospheric radiations representing an intense continuous flux, which have been shown to affect the overall reliability of electronic systems. In atmospheric environment, neutron-induced single event effects are known indeed to be a crucial concern for high power device reliability [1]. Under the effect of a primary neutron, nuclear interactions occur within the device with any of the constitutive atoms, producing recoil ions and eventually even the generation of localized currents. These unsuited currents possibly induce a thermal breakdown of power devices and a loss of functionality of the entire system, due to the high internal drain to source electric field. This Single Event Burnout (SEB) destructive mechanism has been investigated for SiC power diodes [2] and SiC power MOSFETs [3,4]. For MOSFETs, investigations focused on the effect of applied drain voltage on SEB sensitivity [5] and device technology [6–8]. Impacts of electrical stress [9] and reverse gate voltage [10] were also evaluated. Some studies estimated the location of the sensitive volume for initiating SEB in SiC-MOSFET through numerical simulations [11,12]. Moreover, in this reference [12], the authors study the difference between heavy ion and neutron-induced SEB, showing that in the special case of neutron irradiation the sensitive volume is near the epitaxial-substrate junction. By comparing SiC-MOSFET and SiC-PIN diodes, no significant failure rates difference was found against neutron single event effect [4], therefore this study concludes that the SEB mechanisms in SiC-MOSFET is due to the current-induced avalanche in the drift region.

In this work, packaged commercial SiC MOSFETs have been tested under an accelerated atmospheric neutron spectrum to determine their reliability for critical applications. At the die level, failure analysis has been performed in order to provide new insights regarding the physical mechanisms at stake during neutron-induced SEB.

Devices and Test Set-Up

Device Under Test (DUT)

The devices under test (DUT's) are commercial vertical planar-gate SiC power MOSFETs in a TO-247 molded packages. For this device, nominal maximum ratings are $V_{DS} = 900$ V, V_{GS} from -4 V to +15 V, $I_{DS} = 23$ A and on-resistance (R_{on}) is 120 m Ω . Electrical characterizations, including I_{DS} - V_{GS} and I_{GS} - V_{GS} measurements, have been performed before and after irradiation for each device.

To evaluate the irradiation effect, a dedicated test board following the MIL-STD-750E test standard has been designed and fabricated. The test board containing DUTs is placed under the radiation beam while drain and gate voltages are controlled. Source measurement units (SMUs) are used to supply voltages and to measure currents in the control room. The SMUs were controlled and data were collected via Ethernet and USB interfaces. The schematic diagram of the developed irradiation test setup is presented in Fig.1.a). The SiC devices were connected in parallel configuration. For each DUT, a series resistor at the drain was placed in order to limit the total current of the power supply to ensure bias voltage stability across the rest of the non-failed devices. On top of that, a capacitance was placed at the drain of each DUT providing sufficient energy for SEB. Fig.1.b) shows the test board in the irradiation room. During neutron irradiation, $V_{DS} = 675$ V (75% of the V_{DSmax}) and $V_{GS} = 0$ V were applied.

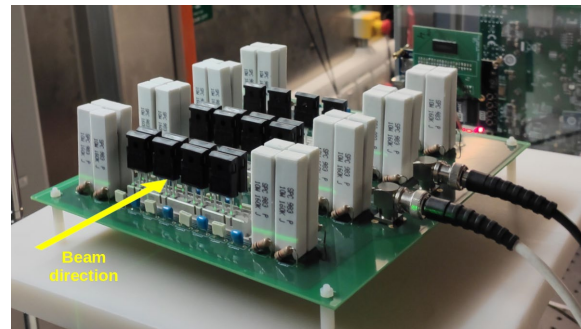
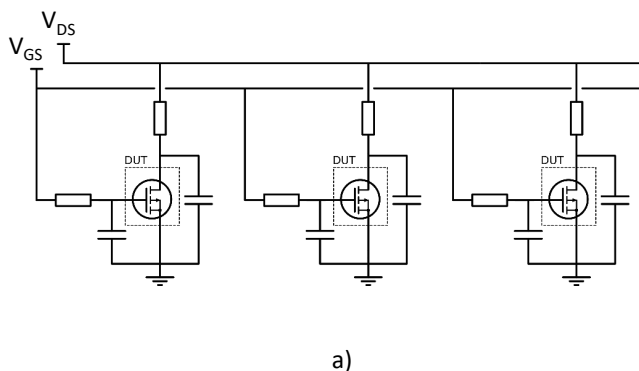


Figure 1: a) Schematic of the dedicated test board for irradiation (for 3 devices) and b) picture of the board with SiC MOSFETs.

Neutron irradiations facility

Neutron irradiations were carried out at ChipIr (Chip Irradiation) beamline [13] of the ISIS spallation source at the Rutherford Appleton Laboratory, UK. This beamline is dedicated to accelerated testing of microelectronics under atmospheric-like ultra-fast neutron spectrum. For neutron energies above 10 MeV, the average flux is 5×10^6 cm $^{-2}$ s $^{-1}$. The acceleration factor compared to the ground level neutron flux is 10^9 . For this experiment, devices were irradiated up to a neutron fluence of about 2×10^{10} n/cm 2 .

Results and Discussion

Experimental results are reported in Fig.2. Fifteen devices, with the same lot number, were irradiated by neutrons. A SEB event was detected by the increase of I_{DS} of the device. The cumulative SEB events is plotted versus the neutron fluence (Fig.2.a). Since the neutron-matter interaction is considered as a stochastic process, as expected, a constant rate increase with time is observed. Moreover, Weibull shape parameter of the neutron induced failure distribution is 0.93, close to 1,

which indicates random failures i.e. constant failure rate over time. After the total fluence of 2×10^{10} n/cm², 53 % of the irradiated devices were destroyed, thus eight devices of the initial lot. For a device having suffered a SEB, subthreshold $I_{DS}-V_{GS}$ and $I_{GS}-V_{GS}$ before and after irradiation are represented in Fig.2.b). Electrical characterizations after neutron irradiation show the occurrence of the short circuit between the drain and the source due to the SEB. After neutron irradiation, the I_{DS} exhibits an increase and reaches the compliance limit, implying the loss of voltage blocking capability of the SiC MOSFET structure. On top of that, from $I_{GS}-V_{GS}$ response, a low resistance current path from gate to source is measured.

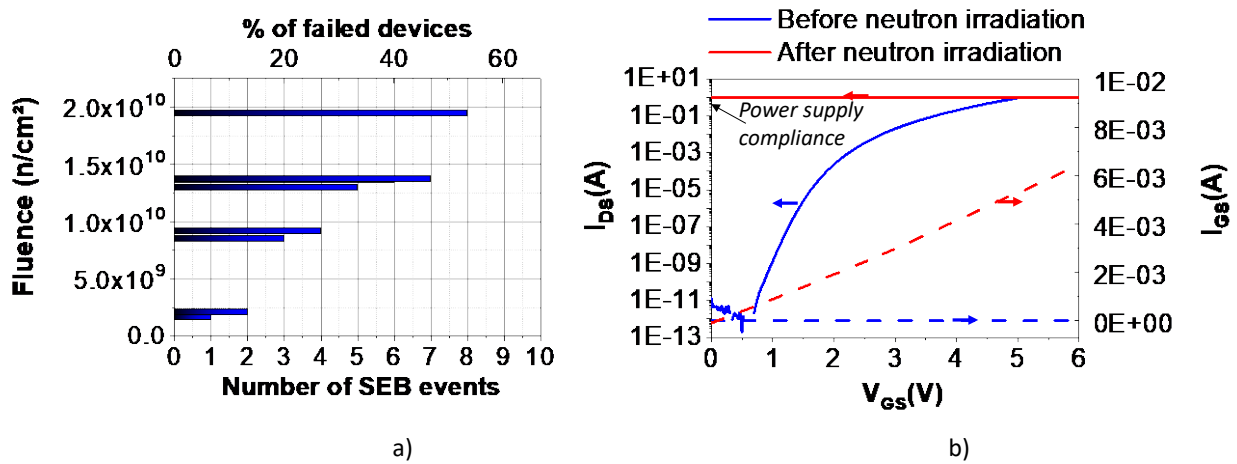


Figure 2: a) Fluences of SEB occurrence during neutrons irradiations, b) $I_{DS}-V_{GS}$ and $I_{GS}-V_{GS}$ before and after neutron irradiation for a device having suffered a SEB.

In order to analyze the SiC MOSFET at the die level and provide electrical local analysis, a cross-sectional sample preparation was developed. Since the device is a packaged commercial component (not a device from a bare die without packaging), and to conserve the back-end structure, the sample preparation has been based on a backside opening, followed by the mechanical grinding of the copper heat spread. The SiC die has been thinned (less than 50 μ m thickness) in order to become fully optically transparent. The sample cutting axis was located at the center of the damage observed, through the thin SiC material. Our localization method for this SEB damage is different from the analysis presented in reference [12], where the crack was located from the degradation of top polyimide passivation. In our case no degradation was observable on the front side of the device.

Cross sectional Scanning Electron Microscopy (SEM) views indicate the residual trace induced by the SEB inside the SiC die from the top of the gate (in the metal contact source) to the SiC substrate (Fig.3.a)). Indeed, looking at the failure analysis results, residual deformations, cracks, appearance and shape of the materials allow to propose the following scenario for describing the different steps of the failure mechanism. If the root cause is known to be a nuclear neutron-atom interaction, the SEB can only be initiated by ionizing particles such as recoil ions or secondary atoms created through the primary neutron interaction. A bifurcation shape of the damage inside the SiC material suggests that the secondary particle has deposited enough energy in this sensitive volume (area located in Fig.3.a). Due to the high local electrical field, the impact ionization current is created, and generated electrons and holes respectively flow towards the drain (from the SiC epilayer to the substrate) and the source contacts, surrounding the gate contact. This bifurcation trace is clearly located at the point of maximum impact ionization inside the SiC, which corresponds to the hot spot during the SEB (the point of the highest temperature). Therefore, the starting point of the SEB is thus located in the n-drift epitaxial region below the channel. This experimental observation agrees with the location of the SEB sensitive volume determined by simulations in reference [12]. A zoom of the damage in the gate region is compared with a gate without impact (Fig.3.b)). In the SEM view, after the SEB the gate and interlayer dielectric (ILD) are completely blown up. Due to the SEB, the ILD is cut in two parts and one part is displaced, thrown up into the source metal. This is an evidence of a self-sustained

strongly localized overheating through the impact ionization process and/or the Kirk effect. Once the SEB has resulted in the high drain current state due to the short-circuit between drain and source and an electrical connection of the metal source contact to the drain is created. Like a fire blast, a collateral effect likely related to the thermal expansion of SiC material has been observed, leading to the total contact melting and metal inclusion. As a more global thermal consequence, we also observe the delamination of the epoxy resin of the metal layer.

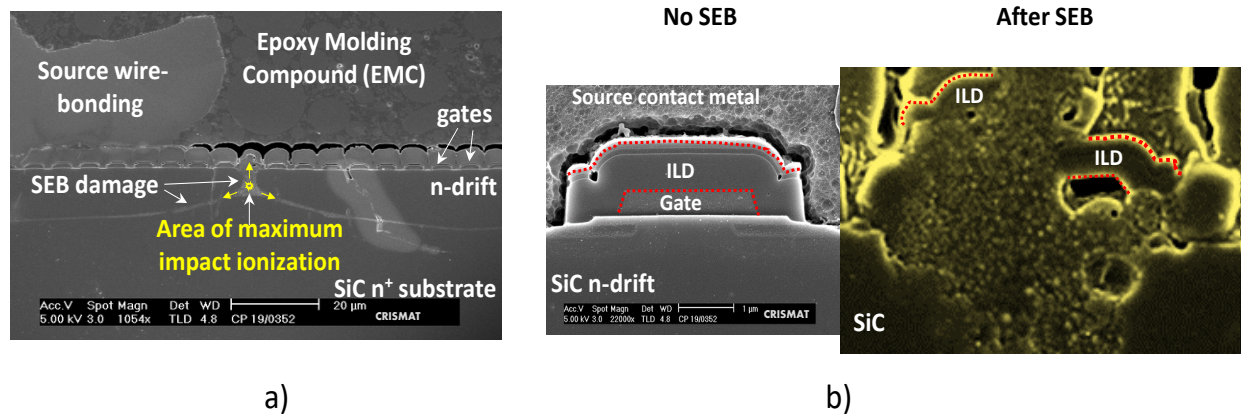


Figure 3: SEM views of the SiC MOSFET structure after SEB, a) large view where the location of the impact is determined and b) comparison of two gates regions without and after SEB.

Conclusion

In this paper, the total thermal runaway of a SEB mechanism in a packaged commercial SiC power MOSFET was analyzed by SEM. Damage zone is located by a special backside opening to conserve back-end layer structure. Based on failure analysis, the different steps of the SEB scenario have been elucidated and experimentally proves that the neutron-induced SEB sensitive volume is inside the drift region, near the epitaxial-substrate junction. The analysis of the SEM view clearly reveals the starting point of the SEB located in the epitaxial SiC layer and just under the channel region.

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