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SiC Diode with Vertical Superjunction Realized Using Channeled Implant and Multi-Step Epitaxial Growth

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Abstract. This work details two approaches with multi-epitaxial growth to create a vertical superjunction structure made of alternating pillars. One approach is a chain of very high energy implants, the other uses a preferred implantation direction to achieve a channeled profile. The manufactured devices show a breakdown voltage of 1000 V for channeled, two-step epi with a total thickness of 4.9 µm. 800 V for regular high energy implants using three epi steps of a total thickness of 3.7 µm. The measured R_{sp} was 0.7 mOhm*cm^2 for dies with size 0.018 cm^{-2}. UIS and temperature measurement show reliable performance. The channeled implant looks favorable to reduce the number of process steps needed to create an efficient superjunction structure.

Introduction

The challenge in power semiconductor manufacturing is always to balance the tradeoffs of cost, blocking voltage and forward resistance. In unipolar vertical devices, switching to Silicon Carbide (SiC) from Silicon (Si) already reduces the needed epitaxial thickness of the device, greatly reducing the on-state resistance. The superjunction concept [1] can push this even further by decreasing the thickness and resistance for the same voltage rating. The superjunction is a charge balance structure, made of narrow, highly doped alternating p-n regions in the epitaxial layer, as shown in Fig. 1 a. The superjunction region becomes completely depleted at a high blocking voltage and provides a trapezoidal electric field distribution, leading to higher breakdown voltage (see Fig. 1). The high n-doping enabled by the superjunction concept reduces the on-state resistance. There are multiple ways to create a superjunction structure, with various levels of complexity and equipment needed [2]. In this study, a process is demonstrated relying on vertical pillars made by multi-step epitaxial growth and two implantation methods – very high energy implant chain (VHE) and channeled implant. Devices made by both methods are electrically characterized and compared.

Fabrication Process

The superjunction diodes are made on heavily Nitrogen (N) doped SiC wafers. In the first step, a buffer layer (2 µm, 1e17 cm^{-3}, nitrogen) is grown on the substrate, along with a first layer for the pillars. In the case of VHE implant, the layer is lightly n-doped and implanted by a chain of energy and doses with N ions to create a desired concentration. Then the layer is masked with 3 µm of photoresist, and a similar chain of aluminum (Al) is implanted, with double the total dose of the nitrogen implant to create the p-pillar. The epi and implantation steps are repeated until the desired pillar thickness of 3.7 µm is achieved. In the channeled implant scenario, the epi layer was grown with the targeted nitrogen concentration of 6.3e16 cm^{-3} and Al was implanted along the [0001] crystal

direction to create a deep and flat doping profile [3]. The default pillar pitch is 4 µm. A process flow of the process is shown in Figure 2 and simulated profiles are shown in Figure 3. For the VHE experiment, the epi and implant process are repeated three times for a total thickness of 3.7 µm of charge balance area. The channeled experiment requires only two epi-implant steps with a total thickness of 4.9 µm.

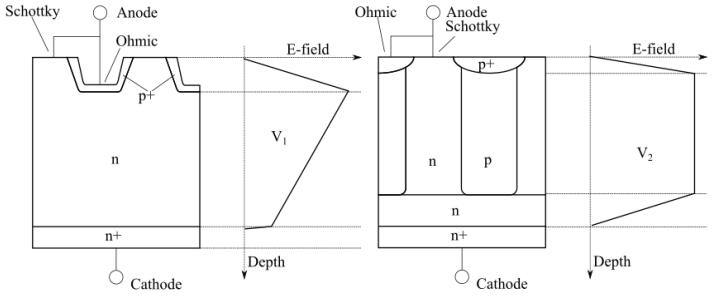

Figure 1. Schematic illustration of the Superjunction concept. Left: Classic design of junction barrier Schottky diode. Right: Superjunction with vertical pillars. The charge balance allows the electric field in reverse to spread in trapezoidal fashion, increasing the breakdown voltage.

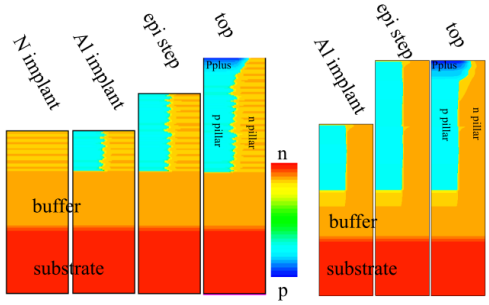

Figure 2. Schematic flow of the multi-epitaxial process. Left: Process with high energy implants. Right: Process with channelled Al implant.

Epitaxial growth techniques were developed to fabricate both highly doped and lightly doped layers. The pre-growth and initial growth conditions were optimized to have minimal pre-etch and an abrupt transition layer. In the case of doped epitaxial layers, a continuous doping profile was verified by SIMS.

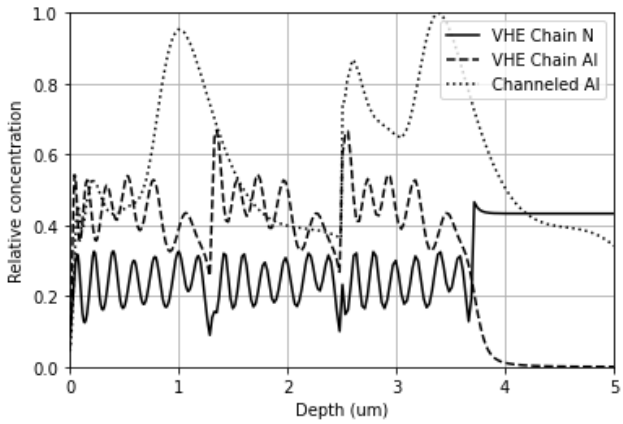

Figure 3. Simulation of the implanted profiles after all epi steps, model is based on internal SIMS data. Values are normalized to the maximum in channelled experiment.

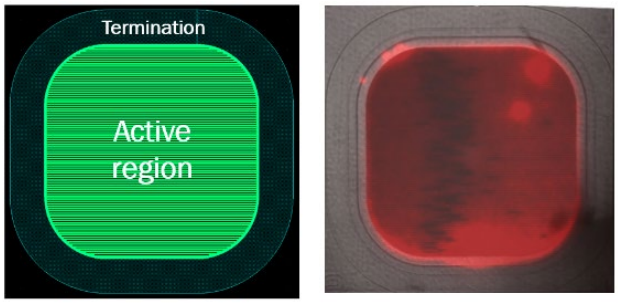

Figure 4. Left: Schematic of the device layout. Green stripes show the p-type implanted regions defined by the pillar mask. Right: Photoluminescence photo of the device in breakdown condition. The current is concentrated in the active area, showing robust design of the junction termination.

The p-pillar was finalized with a high dose Al implant. A Ti/TiN barrier and aluminum layer was deposited over the active structure and annealed at 450°C. The high doped region on the p-pillar forms a Schottky contact while the n-pillar forms a Schottky one. The implants were activated by annealing at high temperature prior to formation of the metal contacts. The wafer was thinned to 200 um and the backside Ni contact was laser annealed.

Device Design. The superjunction diode was designed with stripes along the [11$\bar{2}$1] direction to avoid the shadowing of the implant with photoresist during the 4° angled implantation needed for channeling. The charge balance was controlled by varying the p-pillar mask width. The JTE termination was designed to distribute the avalanche current homogenously in the active region to achieve a robust device in unclamped inductive switching. The design was verified by photoluminescence measurements and shows uniform emission in the active area at the breakdown voltage. The schematic and the measurement are shown in Figure 4. Both small (0.0012 cm^{-2}) and big (0.018 cm^{-2}) dies were manufactured.

Electrical Results. The devices were subject to several tests, both on wafer as well as in package.

Breakdown voltage and Rsp. Wafer level tests were performed on devices near the wafer top, center and bottom, as the epi thickness and concentration vary across the wafer and both parameters affect the resistance and breakdown voltage. The measurements are shown in Figure 5 (a-c). Both approaches worked as intended, with similar values of BV per micrometer of charge balance structure. The VHE approach showed a higher tolerance to the thickness and concentration variation of the epitaxial layers, at the expense of needing more layers to get the desired BV. The variation of the p-pillar width and the implanted dose illustrate the charge balance and its sensitivity. It is apparent by the BV that the channeled experiment was shown to have slightly higher Al concentration in the 100% dose and pillar ratio 1, while the VHE had Al underdosed. The rise of Rsp values for wider p-pillars and higher Al doses was caused by the pinching of the n-pillar, which is also the width of the Schottky contact. The specific on-resistance Rsp (extracted in the linear regime) was measured for smaller dies and is thus affected by current spreading. The actual values of Rsp for the 0.018cm^{-2} device is shown in the temperature dependent analysis.

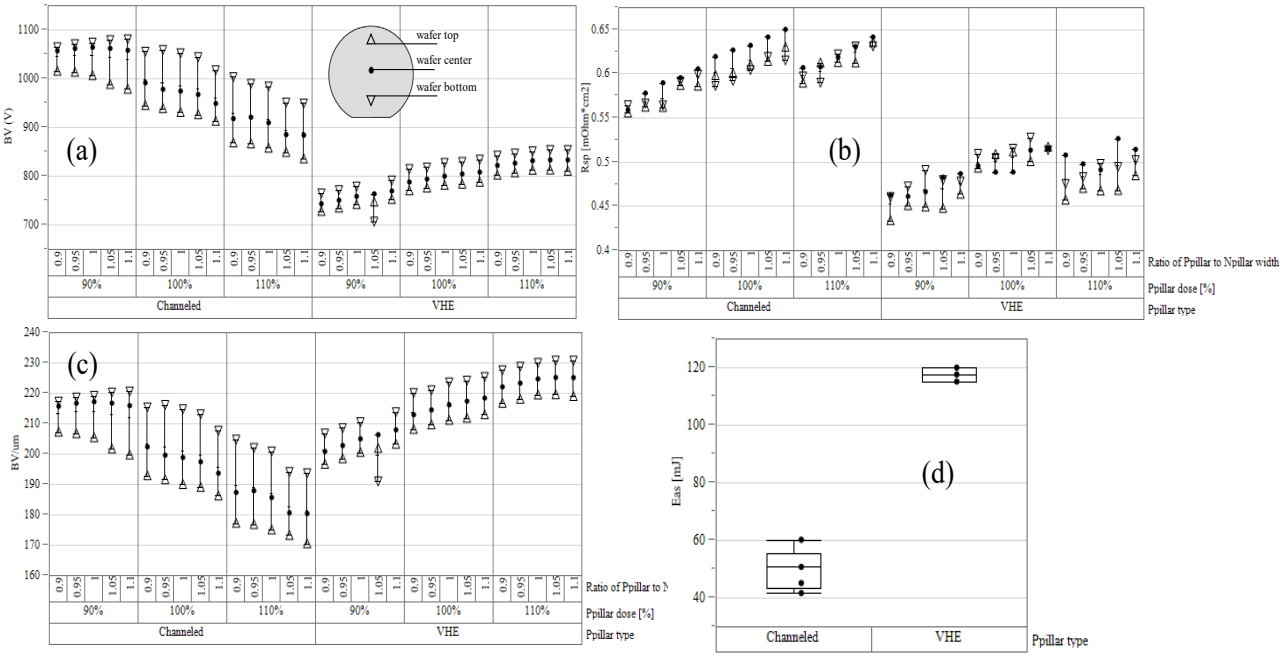

Figure 5. (a) Results of Breakdown voltage with dependence on type of p-pillar, respective dose and pillar-to-pillar ratio. Inset shows the location of measured devices across the wafer. (b) Rsp values on small devices. (c) BV normalized to the pillar depth. This shows that both approaches have similar characteristics and the BV in mainly determined by the pillar depth. (d) Results of Eas (avalanche energy in unclamped inductive switching, single pulse) on packaged devices.

Unclamped Inductive Switching (UIS). Samples from both concepts underwent UIS to verify device ruggedness. At least 3 samples were measured for each design with an inductance of 1 mH. The maximum sustained energy Eas for the devices with VHE implant was 121 mJ whereas the

channeled implant only sustained 41 mJ (mean values), shown in Figure 5 (d). Based on photoluminescence measurement, the device with VHE implant has avalanche concentrated at the top of the edge of the active region, shown in Figure 6. The good UIS result can be explained by the fact that the avalanche distributes in whole active region at a higher current level. On the other hand, the device with channeled implant has avalanche distributed in the active region but significantly lower UIS capability was achieved. Spots with localized avalanche were observed for all samples and these may be related to local barrier reduction due to material defects. As suggested in [4], the VHE data for the 0.018 cm^{-2} die are close to expectation.

On-state resistance and Breakdown voltage over temperature. Eight devices with the same pillar width and implant conditions were packaged. The data in Figure 7, show that the Rsp values rise with a quadratic dependence on temperature. At lower temperatures, the concentration of ionized dopants decreases, hence Rsp rises. The increase in breakdown voltage with elevated temperature is attributed to increased phonon scattering and therefore a higher electric field is needed to induce impact ionization. [4].

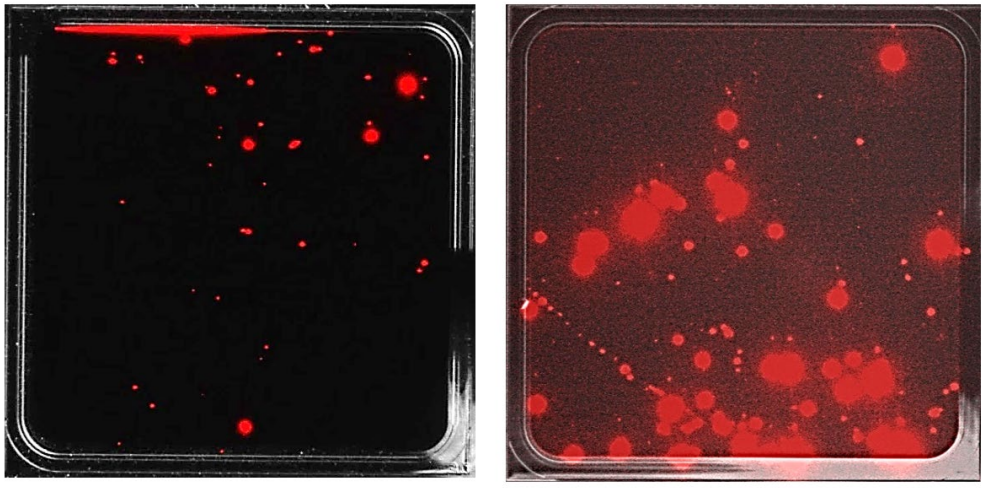

Figure 6. Photoluminescence measurement in UIS. Left: VHE, Right: Channeled

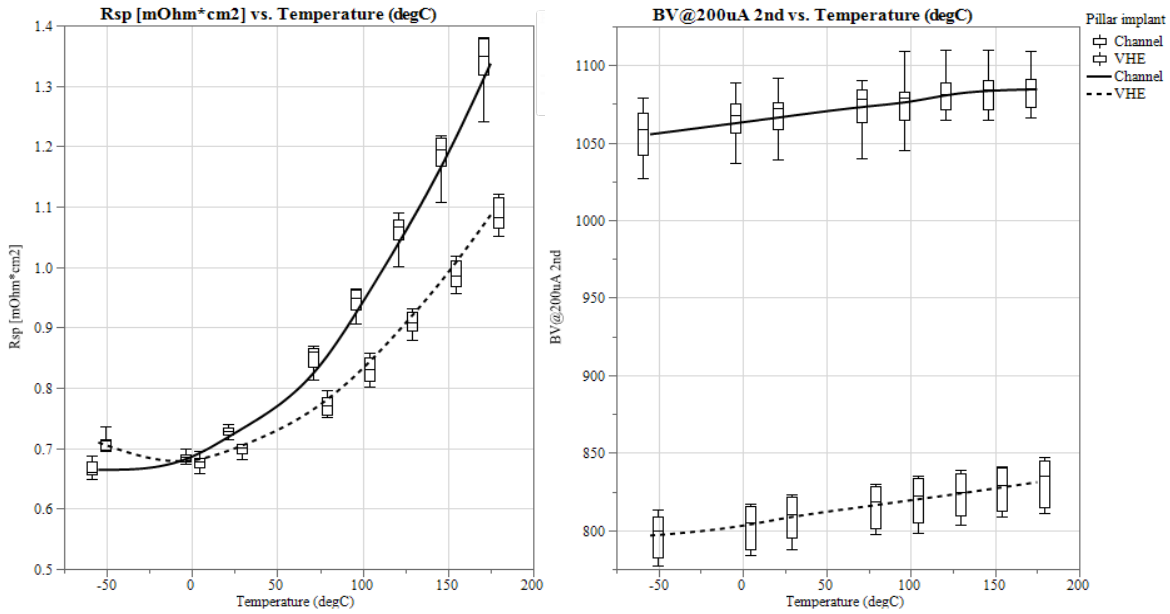

Figure 7. Results of BV and Rsp on large devices at various temperatures

Process Complexity. The multi-epitaxial growth with channeled implant mitigates the risk of introducing additional crystal defects during epi growth. The implantation energies require no special masking process, as the energies are low (<1MeV), yet the channeling provides deep concentration profiles and this reduces the number of epi steps needed.

Conclusion

A SiC Superjunction diode concept is presented using alternating p-n pillars made by multi-epitaxial growth of layers and ion implantation. The implantation is either a chain of high energy implants or medium energy channeled implants. The electrical wafer level measurements show BV of about 210 V per µm of pillar depth and Rsp of 0.7 mOhm*cm^2. UIS measurement shows good avalanche robustness of the VHE approach, while the channeled approach has room for improvement. The device follows a predictable temperature behavior, with increase of both Rsp and BV at elevated temperature. Overall, the use of channeled implant offers a reduction of the number of process steps needed to fabricate the structure and makes for a viable alternative to a traditional device architecture.

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