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Comparative Performance Evaluation of Conventional and Superjunction Vertical 4H-SiC High-Voltage Power MOSFETs

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Abstract. We evaluate and compare the static and dynamic performances of four different 4H-SiC power MOSFETs (Conventional DMOS and UMOS, Superjunction (SJ) DMOS and UMOS FETs) from 0.6 to 10kV with the same approach of [1]. The static on-state performance is determined by analytically calculating the specific on-resistance ($R_{ON,sp}$), while the dynamic switching performance is determined by extracting the specific gate charge ($Q_{G,sp}$) and switching energy loss per cycle ($E_{sw,cycle}$) using 2D device simulations. It has been found that the SJ UMOS FET exhibits at least a 31% (up to 53% at 0.6kV) reduction in the $R_{ON,sp} \cdot Q_{G,sp}$ Figure-of-Merit (FoM) compared to the SJ DMOS FET within the breakdown voltage rating range studied.

Introduction

4H-SiC has a 10× higher critical electric field than Si, making it possible to achieve high voltage power devices with a much smaller (1000x) specific on-resistance ($R_{ON,sp}$) than Si-based devices at the same breakdown voltage (BV). Besides, superjunction (SJ) devices have better conduction performance over conventional devices due to a lower specific on-resistance in the drift layer, resulting in a better trade-off between $R_{ON,sp}$, and BV and hence lower conduction power loss [2]. In this paper, the conventional vertical planar DMOS and trench UMOS FETs, and their SJ counterparts, in 4H-SiC, in the blocking voltage range between 0.6 to 10kV, are examined and compared in terms of their static and dynamic performances, determining quantitatively which transistor to have the best performance.

Device Design

The schematic cross-sections of the four power MOSFETs considered are shown in Figs. 1 to 4, with the unit cell pitch of 6 and 3μm for DMOS and UMOS structures, respectively. The conventional 4H-SiC devices are designed using t, and N_D dependence on BV [3], while the SJ devices are designed according to [4] for the desired BV ratings. In Table 1, the drift layer thickness and the doping of the conventional UMOS and DMOS FETs, while the structural parameters for SJ FETs is at constant aspect ratio (t/W=10). The electron inversion and accumulation mobilities are assumed to be 15 and 200 $cm^2/V.s$ respectively for DMOS. However, the inversion mobility for UMOS FETs is $66cm^2/V.s$ because of the different crystal orientations.

Table 1. Design parameters of conventional and SJ 4H-SiC MOSFETs at different BV ratings.

BV Rating [V]	Conventional 4H-SiC U/DMOSFETs		Superjunction 4H-SiC U/DMOSFETs	
	Drift Layer Thickness (t)[μm]	Drift Layer Doping (N_D)[cm^{-3}]	Pillar Thickness (t)[μm]	Pillar Doping (N_P) (t/W=10)[cm^{-3}]
0.6k	5.5	2.4×10^{16}	3.0	3.3×10^{17}
1.2k	11	1.2×10^{16}	6.0	1.7×10^{17}
3.3k	35	3.4×10^{15}	24	4.2×10^{16}
4.5k	50	2.2×10^{15}	32	3.1×10^{16}
10k	130	7.3×10^{14}	64	1.6×10^{16}

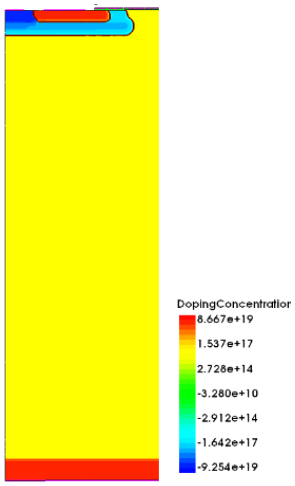

Fig. 1. Schematic cross-section of the conventional DMOS half-cell.

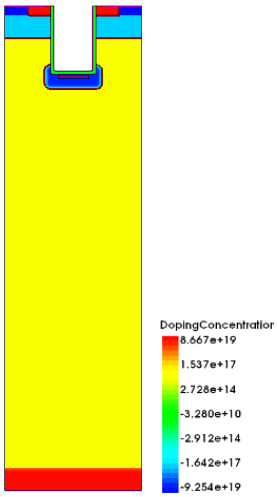

Fig. 2. Schematic cross-section of the conventional UMOS full-cell.

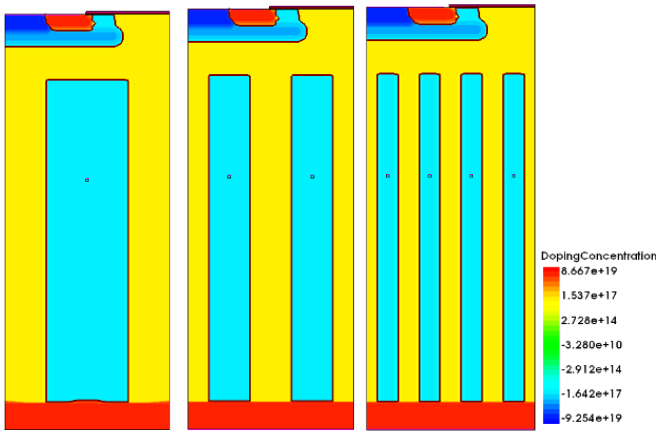

Fig. 3. Schematic cross-section of the SJ DMOS at different pillar widths.

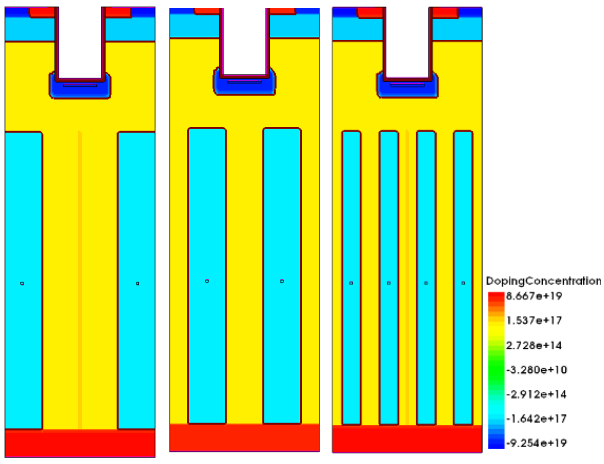

Fig. 4. Schematic cross-section of the SJ UMOS at different pillar widths.

The specific on-resistance components are depicted in Fig 5 and 6. All of them are calculated using the structural dimensions, doping, and mobility of the corresponding regions. The three main components are the channel region ($R_{ch,sp}$), the JFET region(s) (R_{JFET} (1,2)), and the drift region ($R_{drift,sp}$) for the conventional devices. However, for SJ devices, the drift region has a lower resistance because of a higher pillar doping compared to conventional devices. At lower BVs, the resistance of the channel region dominates, while the drift region dominates at relatively BVs. Consequently, at lower BVs, we expect that the conventional and SJ devices will have almost the same specific on-resistance ($R_{ON,sp}$) due to the channel region, however, at higher BVs, SJ devices will deviate from the conventional devices and exhibit a significantly lower specific on-resistance ($R_{ON,sp}$).

For the dynamic characteristics, the specific gate capacitance is extracted from a 2D device TCAD simulator (Sentaurus) for each device at each BV rating. From the switching simulations, the gate current i_G is integrated over the time to obtain $Q_{G,sp}$. Furthermore, switching energy loss per cycle ($E_{sw/cycle}$) are extracted. The switching circuit is shown in Fig. 7, where the device is scaled with the appropriate resistive load to achieve the same drain current (I_D = 10A) and (V_{on} = 1V) through and across each device.

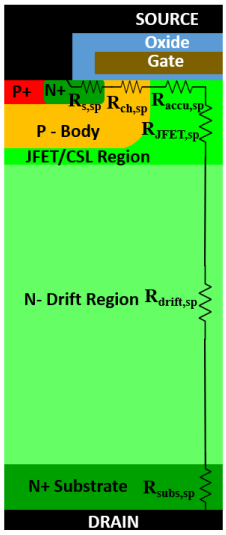

Fig. 5. Schematic DMOS cross-section showing various specific on-resistance components.

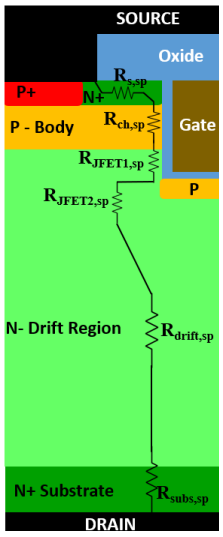

Fig. 6. Schematic UMOS cross-section showing various specific on-resistance components.

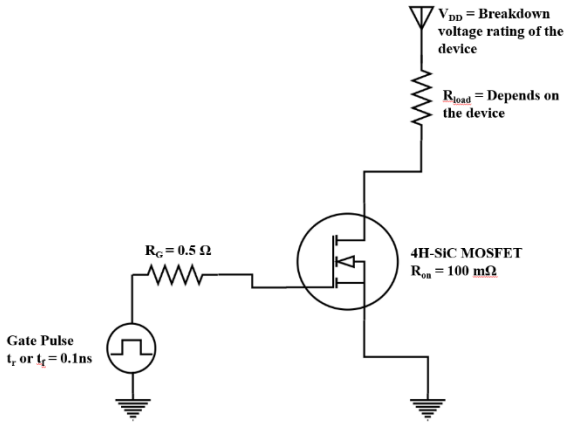

Fig. 7. The switching circuit schematic with a resistive load.

Results and Discussion

In Fig. 8, the $R_{ON,sp}$ and BV trade-off for SJ FETs is better. For SJ FETs, the trade-off is $R_{ON,sp} \propto BV^2$ and $R_{ON,sp} \propto BV$ for constant asepct ratio and constant pillar width respectively, while it is $R_{ON,sp} \propto BV^{2.3}$ for conventional FETs. In Fig. 9, $R_{ON,sp}$ is reduced by 89 and 78% for SJ UMOS and DMOS FETs respectively, compared to their conventional counterparts at 3300V, due to a lower $R_{drift,sp}$, achieving 99% reduction at 10kV, while $Q_{G,sp}$ reduction is 8 and 20% at all BV ratings. The lower $R_{ON,sp}$ of UMOS devices is due to a higher channel density, hence lower $R_{ch,sp}$. In Fig. 10, SJ UMOS exhibits longer turn-off time, hence, higher switching energy losses per cycle due to higher $Q_{G,sp}$. As illustrated in Fig. 11, the SJ UMOS FET with the narrowest pillar width [5] exhibits the best performance as it has a Figure-of-Merit (FoM) ($R_{ON,sp} \cdot Q_{G,sp}$) reduction of 24, 47, 90, 95, and 99% compared to conventional UMOS at 0.6 to 10kV ratings respectively, while it is 53, 51, 49, 40, and 31% in SJ DMOS at the same BV ratings respectively. The FoM reduction is decreasing at higher BV because the pillar resistance dominates at higher BVs. Unlike Si, 4H-SiC has a significant specific drain charge $Q_{D,sp}$ because of its heavier doping and shorter thickness at the same breakdown voltage. On the other hand, SJ devices exhibit sharp CV characteristics, enabling them to have very small $Q_{D,sp}$, and lower switching losses compared to conventional devices. SJ UMOS has higher switching losses due to an average of 60% higher $Q_{G,sp}$ compared to SJ DMOS, however, it has a significant on average reduction of 50% in $R_{ON,sp}$, achieving the lowest FoM.

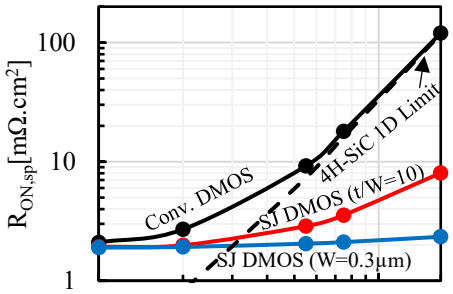

Fig. 8. $R_{ON,sp}$ and BV trade-off for conv. DMOS and SJ DMOS with constant aspect ratio (t/W=10) and constant pillar width (W=0.3µm).

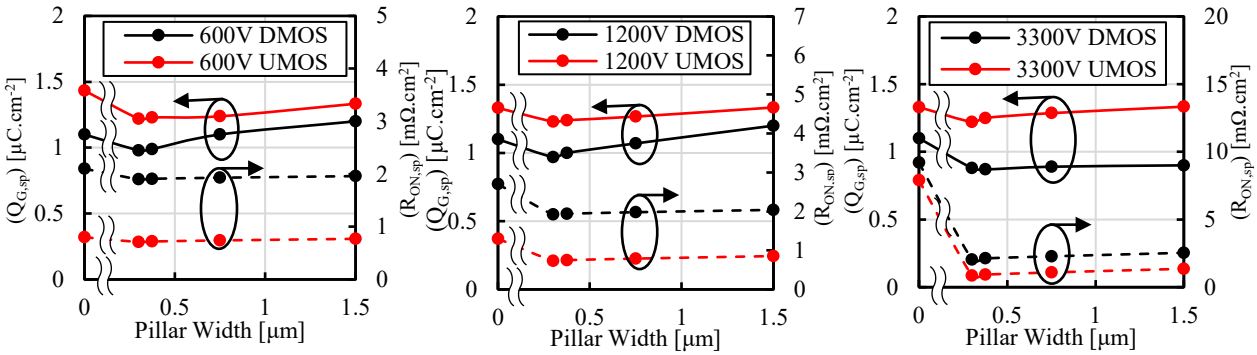

Fig. 9. $R_{ON,sp}$ and $Q_{G,sp}$ for SJ DMOS and UMOS FETs at 600, 1200, and 3300V. Conventional device results are plotted for a pillar width of 0µm.

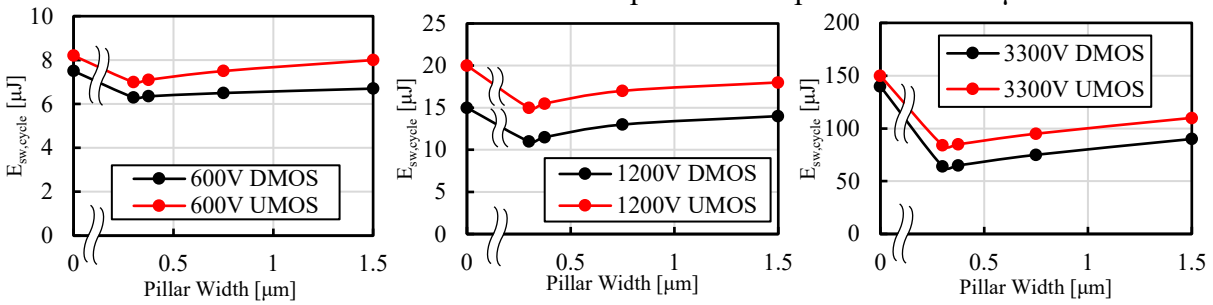

Fig. 10. Switching energy loss per cycle ($E_{sw,cycle}$) for SJ DMOS and UMOS FETs at 600, 1200, and 3300V. Conventional device results are plotted for a pillar width of 0µm.

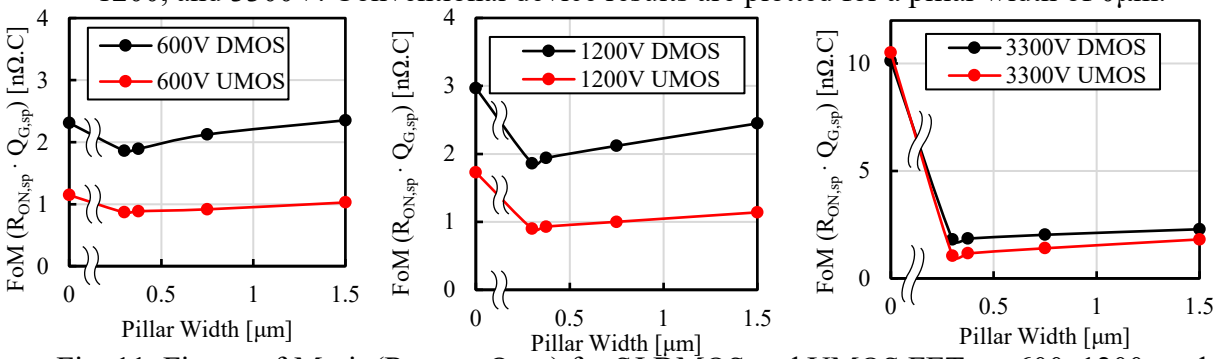

Fig. 11. Figure-of-Merit ($R_{ON,sp} \cdot Q_{G,sp}$) for SJ DMOS and UMOS FETs at 600, 1200, and 3300V. Conventional device results are plotted for a pillar width of 0µm.

Summary

In summary, the SJ UMOS FET has the best performance in terms of the lowest $R_{ON,sp} \cdot Q_{G,sp}$ FoM with at least 31% reduction compared to SJ DMOS at all BV ratings, which infers to have the lowest total energy loss (conduction and switching losses).

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