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Edge Terminations for 4H-SiC Power Devices: A Critical Issue

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Abstract. Edge termination is a critical part of a power devices. Numerous edge termination types have been developed for silicon devices. Implementation of these termination architectures are not straightforward in SiC due to physical and processing specificities: lower junction depths, higher electric field, trench depth and shaping limitations, etc. Two main families of terminations are currently used in commercial devices, pure Field Guard Rings, and JTE + Rings combination. The increasing number of trench commercial devices requires new approaches based on etched rings filled with dielectrics or polysilicon. For epitaxied bipolar devices, MESA with bevel angle termination combined with JTE based architecture are also suitable. In any case, and especially regarding avalanche capability requirements, not only the termination architecture is relevant, but also the passivation type, the channel stopper design, the 3D design. As modelling using conventional tools is not fully reliable, specific characterization methods are needed. For instance, micro-OBIC can be very effective to determine the electric field distribution in the periphery of the power devices.

Introduction

Most of planar and trench power devices are based of one or several n-type/p-type junctions. When the active part of the junction ends on the lateral side of the device, a very high electric field appear under reverse voltage biasing, due to junction curvature or trench corners. Then, a periphery protection, called edge termination is necessary. Reliable and robust high voltage devices need effective edge termination structures to protect the device periphery, so that blocking values close to the ideal 1D avalanche voltage value can be achieved. Many types of terminations have been developed in Silicon technology, the main ones being MESA termination for rectifiers and thyristors, field plates for low voltage range, field guard rings (FGR) and junction termination extension (JTE) for planar rectifiers and transistors. Silicon Carbide is not as friendly as Silicon in terms of processing technology for power device fabrication. Several physical limitations make SiC edge terminations more complex to design in a same way to Silicon. The main limitation is the low diffusion coefficients of dopant atoms inside the semiconductor. Deep junction (> 1μm) are difficult to implement and lateral dopants diffusion is very limited. On the other hand, one of the theoretical advantages of SiC versus Si, its high critical electric field, is also a drawback when looking for compatible dielectric layers capable of operating under such high fields in a reliable way. It clearly limits the use of field plates for instance. Finally, the higher interface traps level observed in the SiC/SiO_2 interface compared to Si is also affecting the efficiency of the standard Si terminations architectures in the SiC power devices. Charges accumulate at the interface, generating breakdown voltage instabilities, especially with temperature. Finally, the termination design is also relevant to reach high avalanche ruggedness in order to comply with applications prone to unclamped inductive switching. In this case, the edge termination must reach breakdown at higher voltage than the main active junction [1].

Edge Termination Structures

Termination optimization is relevant in power device design since it may affect the reliability of the component, but also because it may consume a large area of the die, especially in the case of very high voltage devices (Fig. 1). This is particularly relevant for SiC semiconductor, considering the cost of the starting material and the defects density, which usually limit the die area of the components. In addition, in some cases, edge termination integration increases the fabrication process complexity (increasing the number of photolithography mask levels), like in trench JFETs, pure Schottky diodes, BJTs or thyristors. These aspects have a direct impact on cost and reliability.

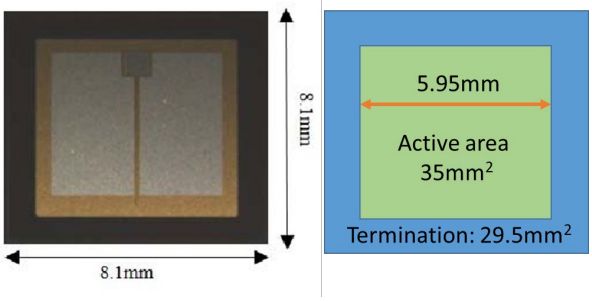


Fig. 1: 6.5kV commercial device picture and evaluation of its respective active and termination area

Usual terminations architectures. The more common periphery protection used in SiC commercial devices is the field guard ring (FGR) termination (Fig. 2a). It is formed with P^+-type implantation wells, having a width of few microns. The key design parameters are the rings distances, which usually increase with the ring position, and the first ring distance with the device main junction. This termination usually consumes a large area and require very precise photolithography and mask etching resolution. The optimal first ring distance depends on the epilayer doping and must be lower than 1µm for devices voltage ranges below 1.7kV. Rings termination also depends on the surface charges at the SiC/dielectric interface. In this sense, buried rings configuration have been proposed in order to shift the high electric field peaks from the surface to the SiC bulk [2], limiting interface parasitic effects. This is efficient but more complex to implement, since epilayer regrowth or very high energy implantation are required.

The second common type of edge protection is the Junction Termination Extension (JTE), which enable smaller area, but which typically requires an extra Al ion implantation step, with an accurate control of the implanted dose. JTE is also sensible to surface charges [3]. Then, single implantation JTE is not used anymore, as multiple JTE combination, having decreasing implantation dose, have shown to be more efficient in terms of process control. SiC etching process can be also use to mitigate the JTE dose (see Fig. 2b) and create a double or triple JTE structure without the need for 3 Al implantation steps [4]. Even if the number of photolithographic masks is not reduced, the global technological process results simpler and cheaper. However, a combination of JTE + FGR, or JTE + FGR + JTE outer rings (see Fig. 3) is the most stable, reproducible and efficient combination for most of the SiC devices structures, especially for blocking voltages higher than 1.7kV. For instance, this architecture has been used in [5] for 27 kV diodes demonstration. Other combination of JTE and rings have been proposed in order to reduce termination length [6].

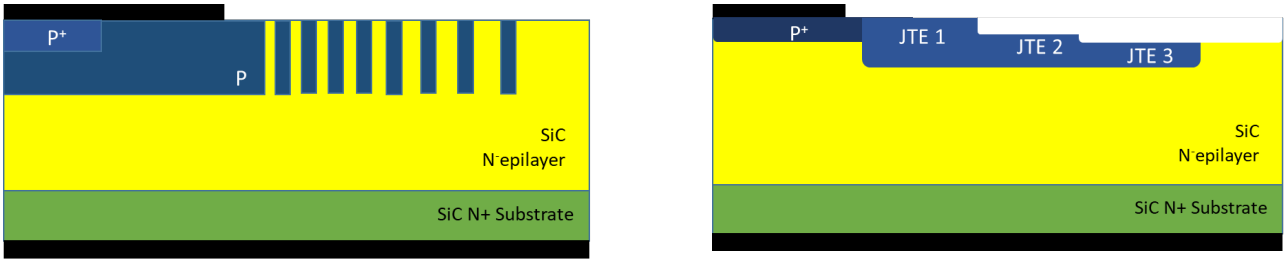


Fig. 2: Schematic of typical termination types including (a) guard rings termination using VDMOS pwell (b) triple JTE created by SiC dry etching

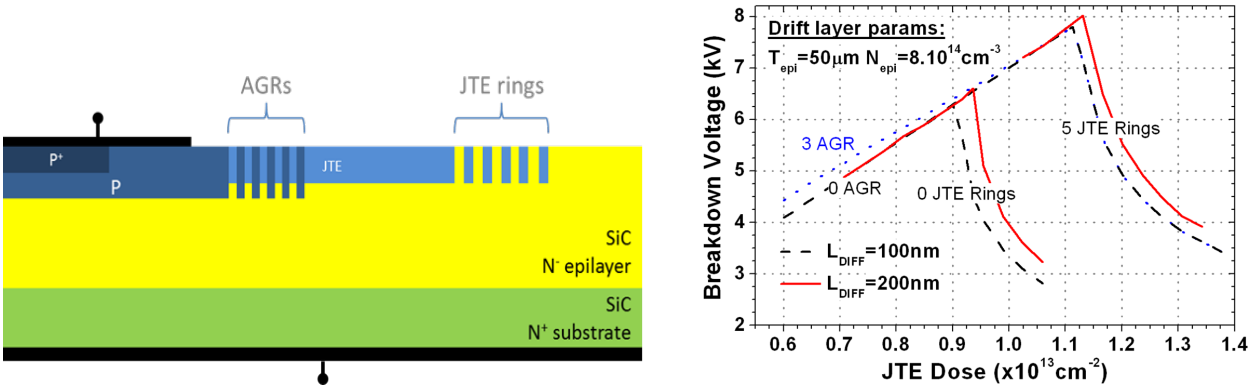


Fig. 3: Schematic of JBS diode termination including (a) JTE with JTE outer rings and P-well FGR (b) comparison of simulated breakdown voltage of a 6.5kV wafer for different JTE + rings designs

In a previous paper [7], we analyzed different field guard rings, JTE and JTE + rings combinations for 1.7kV and 4.5kV planar MOSFETs fabrication. Main results are summarized in Table 1. We intended to use the MOSFET P-well doping to form deep FGR termination (Fig. 1). The efficiency (calculated using simulated ideal 1D breakdown) of these FGR terminations (designs D3 to D8) is lower than the JTE + Rings one (designs D9 to D11). We believe this difference is due to the surface charges type present in our devices. We also tried to use the P-well doping profile as the 1st JTE in a double JTEs configuration (design D2), without clear success. The lateral extension of the P-well in the periphery has basically no impact on the termination efficiency.

Table 1: Measured breakdown voltage and termination efficiency of 1.7kV & 4.5kV MOSFET [7]

Design	Schematic cross section	Wafer#1 Average V_{BR} (V)	Wafer#1 Efficiency (%)	Wafer#2 Average V_{BR} (V)	Wafer#2 Efficiency (%)
D1 (130 µm)		1930	85	4500	77
D2 (100 + 30µm)		1870	82	4000	68
D3 (12 rings)		2000	88	4870	83
D4		1360	60	4550	78
D5		960	42	2880	49
D6 (20 rings)		2080	91	4550	78
D7		1300	57	4230	72
D8		890	39	2700	46
D9		2260	99	5050	86
D10		2260	99	5130	88
D11		2270	99	5230	89

Other 2D and 3D parameters must be defined when designing a JTE (+ rings) termination. JTE length or corner radius must be optimized to minimize the consumed area. In table 2 are reported breakdown voltages of 1.7kV JBS diodes with the termination architecture shown in Fig. 3a. When comparing design D5 to the reference, we can see that a reduction of the corner radius decreases the breakdown capability. The corner radius will also have a strong impact on the device avalanche ruggedness.

Table 2: Impact of the JTE length and corner radius in 1.7kV JBS diode avalanche voltage

	Reference design	D2	D3	D4	D5
JTE length	150µm	*100µm*	*50µm*	*35µm*	150µm
Corner radius	150µm	150µm	150µm	150µm	*100µm*
Avalanche voltage	> 2000V	> 2000V	1450V	1320V	1910V

On the other hand, the recent availability of SiC trench devices also required adaptation of edge termination. In this sense, 3D edge termination like trench guard rings terminations have been recently proposed for SiC devices [8]. This termination configuration has shown to be efficient in Silicon technologies. It allows to reduce the consumed area, and is compatible with the trench fabrication process. Additionally, the bottom of the trench can be implanted with self-aligned buried P^+ ring (see Fig 4a), allowing a reduction of the electric field at the SiC surface. In Fig. 4b, we can see another alternative using a wide trench filled with Benzocyclobutene (BCB) in an as JTE configuration [9-10]. The critical part of this termination is the trench side wall charges displacement and the possible parasitic channel that can be created with the electric field peaks. The field plate geometry on top of the termination structure is also a key parameter. For high voltage components, especially for bipolar SiC device, positive and negative beveled MESA terminations can also be used. These terminations, formerly used in thyristor and early power diodes components presents the advantage of lower dimensions than planar terminations [11]. The main issue, especially for the negative bevel, is the SiC etching process necessary to reach low aspect ratio angles. However, solution playing with the etching mask topology (photoresist) or using multiple etching steps are possible, even if not fully compatible with mass production requirements.

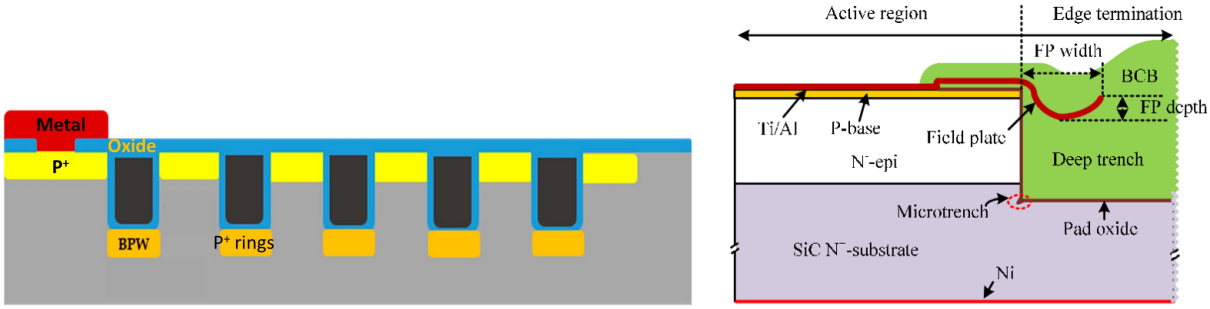


Fig. 4: Schematic of a) a trench rings termination [8] (b) a trench termination filled with Benzocyclobutene BCB [10]

Other termination elements. One element of the termination never mentioned in the literature is the channel stopper (see Fig. 5a). Nevertheless, it is part of the termination design, as the distance between the end of the JTE or the rings and this channel stopper may affect the breakdown capability, the dynamic behavior and directly contribute to the total area required for the periphery protection of the power devices. To determine the optimal position of the channel stopper by modelling is tricky as it depends on a wide range of parameters such as the interface traps and fixed charge of the different passivation layers, the type of packaging technique used, the position of the top metal electrode, etc. We studied the optimal position of the channel stopper in 1.7 kV JBS diodes passivated with 5µm of polyamide. Diodes with a distance of 100µm between the end of the JTE and the channel stopper were able to withstand more than 2 kV while the diodes with a JTE-CS distance of 60µm exhibit a premature breakdown around 1.6 kV after arcing between the anode and channel stopper metals. A picture of a failing diode at 1.6 kV is shown in Fig. 5b, where the damaged area is clearly seen.

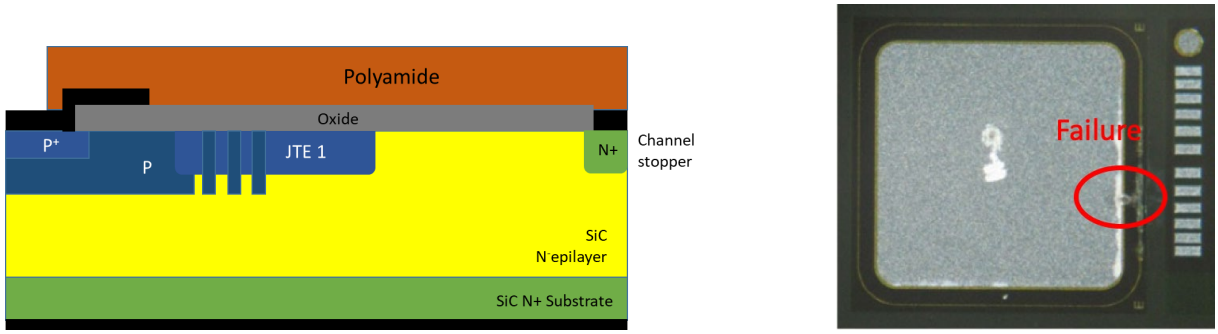


Fig. 5: (a) schematic of the termination with channel stopper (b) A picture of a failed 1.7 kV diode after premature breakdown at 1.6 kV due to short distance between anode and channel stopper

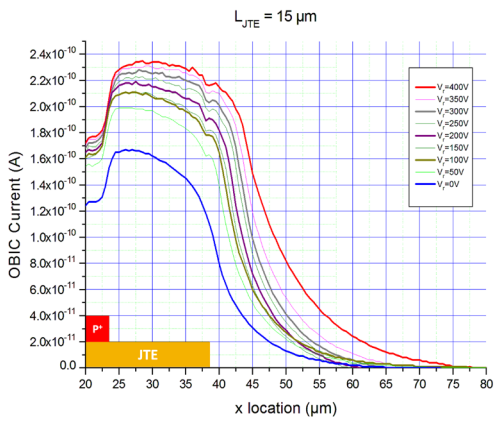
Last but not least, the passivation of the surface in the termination area is a critical aspect for the wide band gap semiconductor high voltage devices. When no passivation is used, premature breakdown due to arcing in air can occur. However, the addition of a passivation layer (for instance polyamide) may change the surface charges state, and impact the breakdown voltage. This is particularly visible in JTE terminations, as the surface charges directly impact the optimal value of JTE implantation dose. Again, a combination of JTE and rings is the most suitable solution to mitigate these charges issues. For high voltage devices (> 2.5 kV), additional effects due to ambient factors like humidity are enhanced and may seriously affect the reliability of power modules if not properly passivated [12]. In this case, solutions pass through a proper packaging technology, for instance using organic passivant like GlobTop. Stability and reliability evaluation of the termination can be done using High Temperature Reverse Bias test (HTRB) [12], including Humidity (H3TRB) [13-14], if a proper evaluation of the passivation is to be done. It is also relevant to test the termination under Unclamped Inductive Switching (UIS) to check the avalanche capability of the device [1].

Termination optimization through advanced characterization:

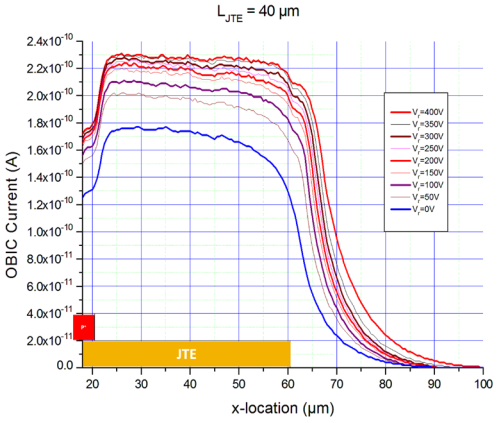
A good understanding of termination behavior also requires advanced characterization tools such as lock-in thermography, photoluminescence, Electron Beam Induced Current (EBIC). Optical Beam Induced Current technique (OBIC) applied to WBG semiconductor devices have shown to be useful to study the efficiency of different edge protection techniques [15]. In order to illustrate some OBIC experiments on different terminations, PiN diodes with several JTE protections (1.7 kV-class) has been measured with increasing reverse voltage up to 400V. Since OBIC setup is under air, as described in [16], it limits the maximum voltage bias for unpassivated devices. Scans were performed from the center of the diode towards the outer periphery. For each results of Fig 6, one can find the drawing of the edge termination at the bottom. Diodes (#1-#3) exhibit increasing length of JTE. Diode #4 has a JTE length of 35 µm + 3 JTE rings. As it can be seen, the OBIC signal appears at least on the JTE length even with 0V. As the reverse voltage increases, the OBIC signal increases and extends laterally towards the outside. For diode #4, none of the JTE rings are depleted at 0V. However, these rings are quickly depleted with a reverse voltage as low as 50V.

Conclusion

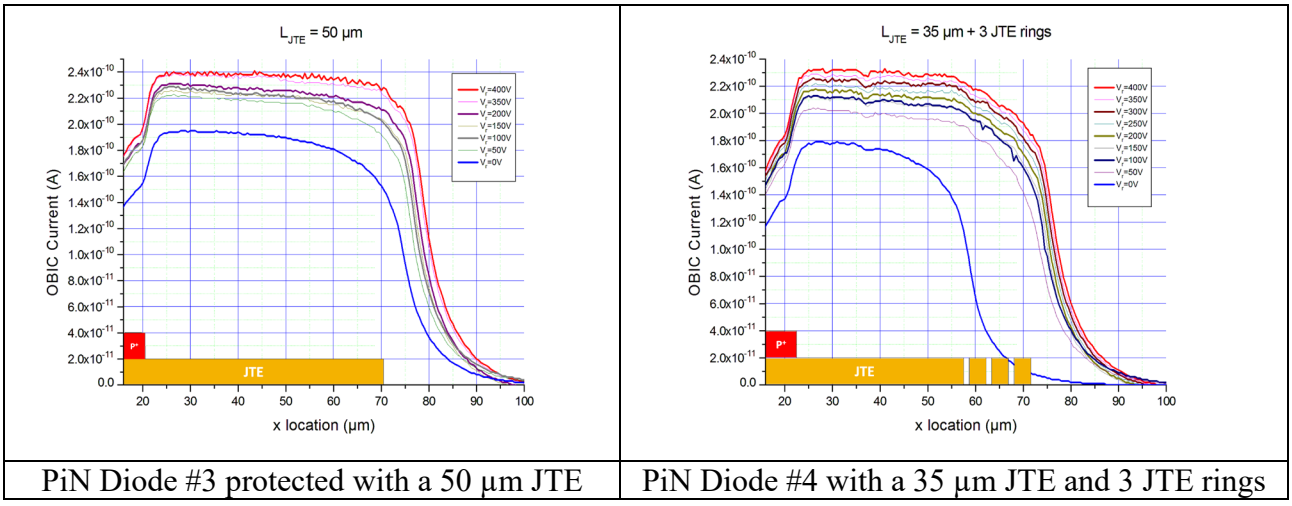
Current edge termination in SiC can reach 100% efficiency, which is relevant for the avalanche ruggedness capability. Termination design is still improving to adapt to the new Trench and Super-Junction technologies or to reduce the consumed area, especially in high and very high voltage devices. However, physical limits as the minimum distance between main top electrode and channel stopper will fix the maximum size reduction achievable. Passivation and packaging are also two of the main concerns for the next generation of high voltage devices.



PiN Diode #1 protected with a 15 µm JTE



PiN Diode #2 protected with a 40 µm JTE



PiN Diode #3 protected with a 50 µm JTE	PiN Diode #4 with a 35 µm JTE and 3 JTE rings

Fig. 6: OBIC measured current versus distance in experiments on 1.7 kV Class PiN diodes with several JTE protections geometries. Basic drawing of each termination is shown as inset

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