

Impact of Device Design Parameters on 15 kV SiC MOSFETs

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Abstract. Experimental results from 15 kV-rated SiC DMOSFETs developed by GeneSiC Semiconductor are presented. A breakdown voltage of 16.7 kV is recorded, with < 200 nA leakage current at 15 kV. $R_{DS,ON}$ in the range of 4-5 Ω , 12-15 Ω or 50-75 Ω were measured on MOSFETs with chip sizes of 25 mm², 16 mm² and 9 mm², respectively, with a lowest specific $R_{DS,ON}$ of 238 m Ω -cm². The impact of MOSFET channel length and JFET width on the device performance is elucidated. Single-pulse avalanche energy = 22.1 J/cm² and t_{AV} =18.2 μ s is achieved. V_G +20 V gate stress applied at 175°C showed good V_{TH} stability with only a small 200-300 mV increase during the initial stages of the stress time.

Introduction and Experimental Details

Ultra-high voltage (> 10 kV) SiC transistors will be a key enabling technology for smart-grid solid-state transformers [1], traction device and renewable energy systems, power supplies for electron guns, and DoD applications [2]. In this paper, we present experimental results obtained on SiC planar MOSFETs developed by GeneSiC Semiconductor on 150 μ m/4.5E14 cm⁻³ thick N- drift layers. Different die sizes with total chip areas of 9 mm², 16 mm² and 25 mm² were fabricated. A planar DMOSFET device structure was employed, with different JFET and MOSFET channel lengths. A 50 nm thick gate oxide was used. The device fabrication was conducted using GeneSiC's established process used for fabricating lower voltage rated SiC DMOSFETs. Selected die were packaged in custom packages for high-temperature and UHV characterization.

Static Electrical Characteristics

Breakdown Voltage: A breakdown voltage of 16.7 kV was measured on 16 mm² MOSFETs fabricated on 5E14 cm⁻³ drift layer (Fig. 1a). The simulated unit cell breakdown voltage is shown in Fig 1b. A worst case breakdown voltage, assuming 20% higher drift doping and 10% higher drift thickness is also shown in Fig. 1b.

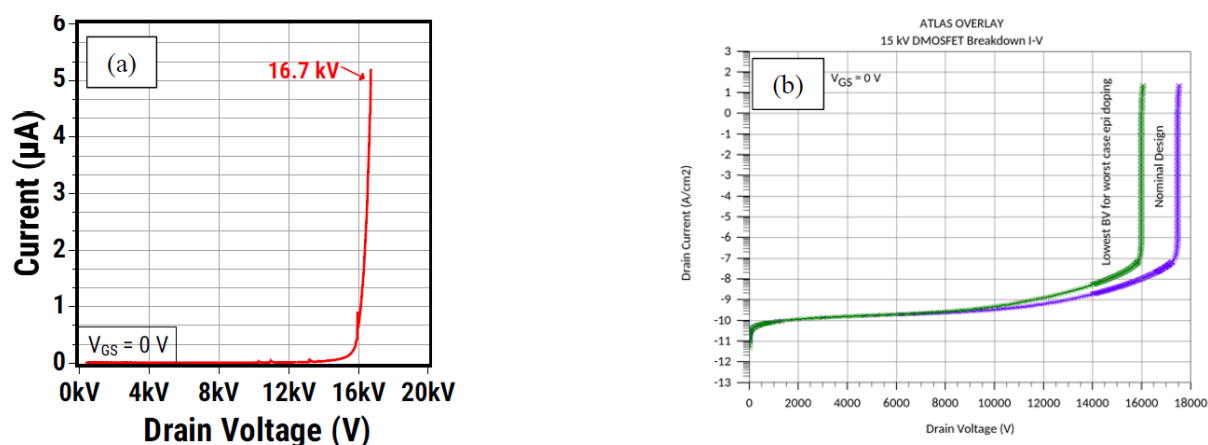


Figure 1 (a): Breakdown voltage measured on SiC MOSFET fabricated on a 150 μ m/5E14 cm⁻³ N-drift layer (b): TCAD Simulated breakdown voltage for the SiC MOSFET unit cell with nominal and worst-case (highest doping/lowest thickness) N-epilayer specs.

The measured breakdown voltage is close to the 1-D avalanche breakdown voltage for the $150\text{ }\mu\text{m}/5\text{E}14\text{ cm}^{-3}$ N-epilayer, which is an indication of a robust device design. A sub-200 nA drain leakage current is observed at the rated 15 kV blocking voltage.

Output Characteristics: A comparison of output characteristics measured in the 1st and 3rd quadrants on 25 mm^2 SiC MOSFETs (active area = 7.4 mm^2) with different JFET widths is shown in Fig 2a. The MOSFET with JFET width of $2.5\text{ }\mu\text{m}$ shows the presence of a “knee voltage” due to a potential barrier in the JFET region, which is clearly absent for the MOSFET with JFET width of $3.0\text{ }\mu\text{m}$. $R_{\text{DS,ON}}$ values of $4.4\text{ }\Omega$ and $5.2\text{ }\Omega$ are extracted at $V_{\text{GS}}=20\text{ V}$ and $I_{\text{D}}=2\text{ A}$, in the 1st quadrant for the different JFET width die, which corresponds to $R_{\text{DS,ON-SP}}$ of $324\text{ m}\Omega\text{-cm}^2$ and $383\text{ m}\Omega\text{-cm}^2$, respectively – the 1-D calculated N-drift layer resistance is $\sim 220\text{ m}\Omega\text{-cm}^2$, for comparison. The $R_{\text{DS,ON}}$ for the two devices in the 3rd quadrant (Fig. 2b) are $252\text{ m}\Omega\text{-cm}^2$ and $259\text{ m}\Omega\text{-cm}^2$, respectively. The 3rd quadrant $R_{\text{DS,ON}}$ is closer to the calculated resistance for the N- drift layer, with almost no difference between the two devices with different JFET widths. Since the body-drift p-n junction is forward biased in the 3rd quadrant, these observations indicate that a significant portion of the total 1st quadrant $R_{\text{DS,ON}}$ can be attributed to the resistance in the JFET region, for these devices. The output characteristics measured at 175°C is shown in Fig. 2b. The $R_{\text{DS,ON}}$ at 175°C increases by a factor of three, when compared to the room-temperature value.

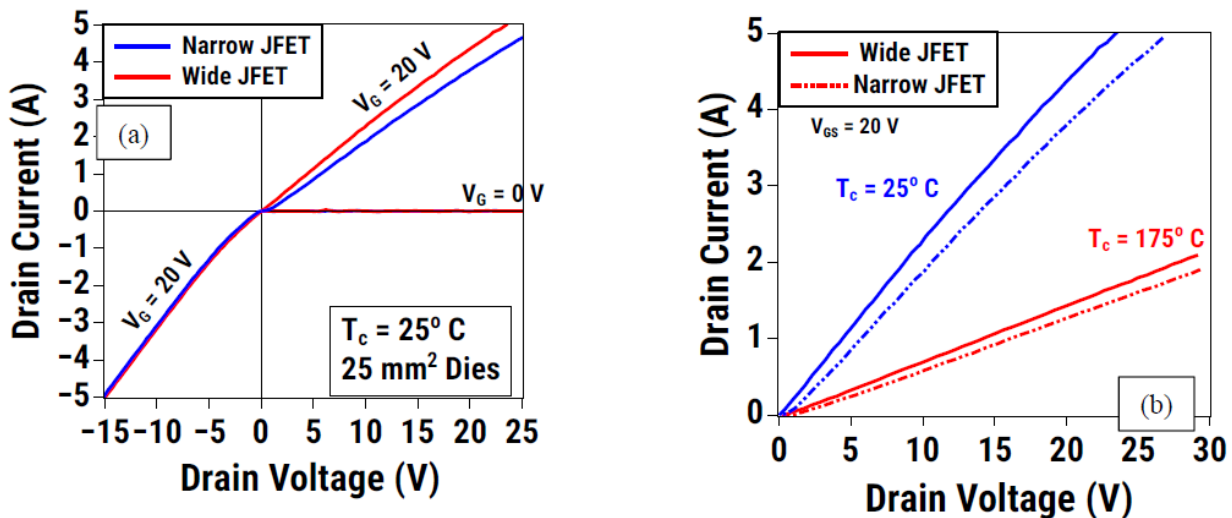


Figure 2: (a) 1st quadrant and 3rd quadrant output characteristics at room-temperature and (b) 175°C measurements of output characteristics.

Impact of JFET Width on $R_{\text{DS,ON}}$: A plot of $R_{\text{DS,ON}}$ versus JFET width is shown in Fig. 3. A clear reduction of $R_{\text{DS,ON}}$ with increasing JFET width is observed – the minima in the $R_{\text{DS,ON}}$ lies beyond the range of JFET widths explored in this study. A lowest $R_{\text{DS,ON}}$ of $238\text{ m}\Omega\text{-cm}^2$ is extracted for the widest JFET width explored in this study – this is close to the theoretical limit. There was minimal impact of MOSFET channel length on the output characteristics (not shown). The peak gate oxide field was kept below 4 MV/cm for all device designs explored in this study.

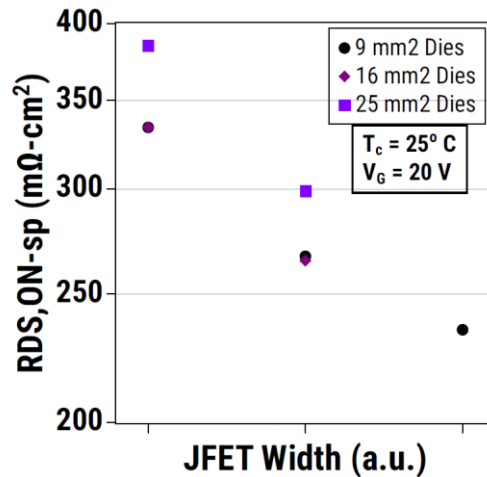


Figure 3: RDS,ON versus JFET Width for 15 kV SiC MOSFETs fabricated in this study.

Third Quadrant Characteristics: The output characteristics in the 3rd quadrant are compared at room-temperature for 16 mm² MOSFETs (active area = 2.1 mm²) at different gate biases in Fig. 4a, and with different channel lengths, in Fig. 4b. A cross-over current is clearly visible in Fig. 4a, above which zero gate bias results in higher I_{SD} than the case when $V_{GS}=20$ V. When the MOSFET channel is kept off (zero gate bias), the I_{SD} is primarily conducted through the p-n junction in bipolar mode, with conductivity modulation of the N-drift layer. When the MOSFET channel is fully turned on ($V_{GS} = 20$ V), a significant portion of the I_{SD} is conducted by the majority carrier electrons through the MOSFET channel, and less current is conducted by the body diode in bipolar mode, which results in a higher differential on-resistance (or lower I_{SD}) at a given drain bias. The MOSFET with the longer channel (Fig. 4b) shows a more pronounced bipolar action when compared to its shorter channel counterpart, since the higher channel resistance pushes more current through the p-n junction. There is no impact of the MOSFET channel length in the 1st quadrant output characteristics (not shown) which are largely dominated by the high resistance of the 150 μ m thick drift layer. At 175°C (Fig. 4c), the Aluminum acceptors in the P-Well are almost fully ionized [3], and this results in a more stark contrast between the zero gate bias and 20 V gate bias output curves for either device. Fig. 4c shows that operating the 15 kV MOSFET at 20 V gate bias can result in a positive temperature co-efficient of I_{SD} , whereas operating the same device at zero gate bias can result in a negative temperature co-efficient of I_{SD} due to the aforementioned competing mechanisms.

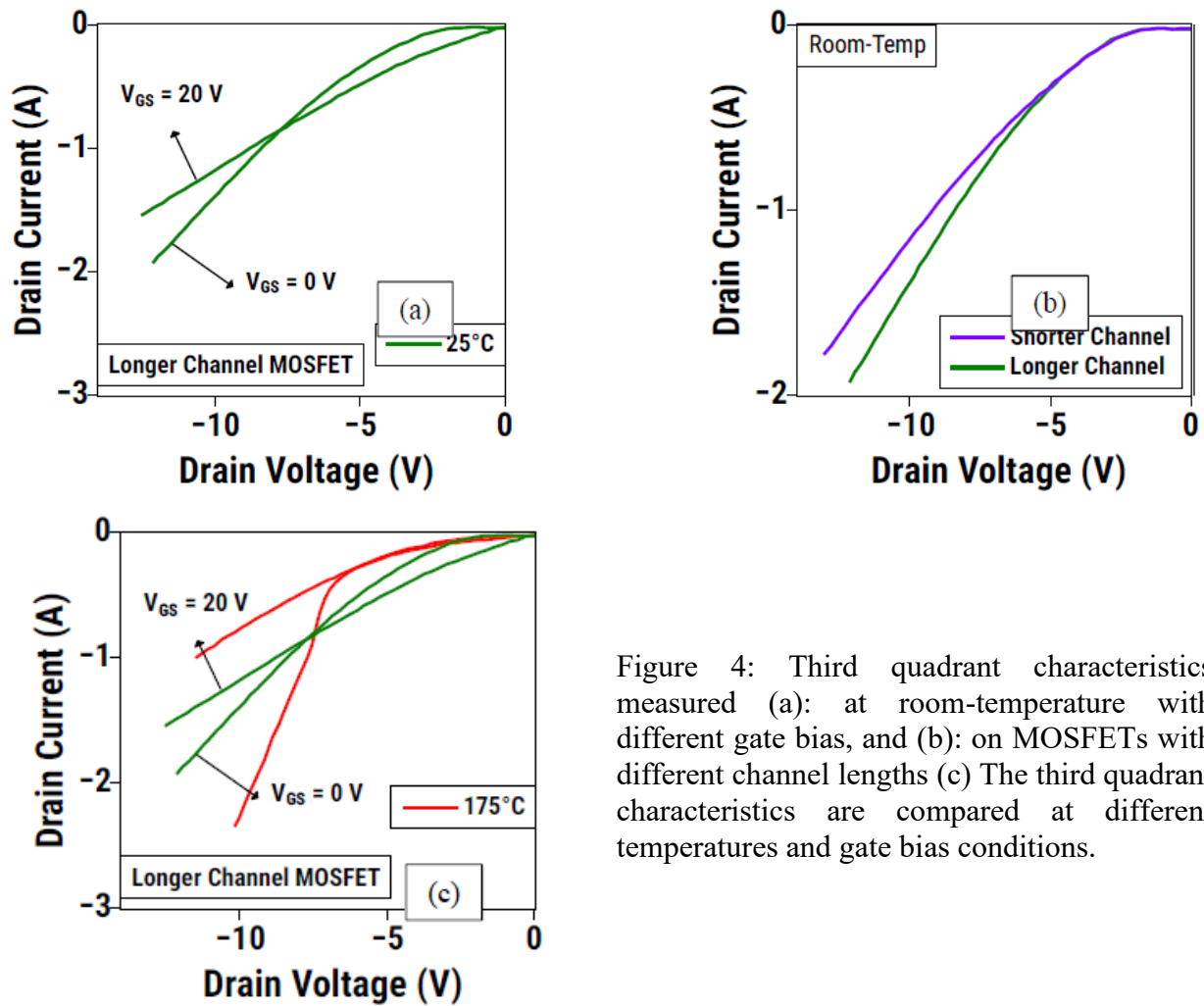


Figure 4: Third quadrant characteristics measured (a): at room-temperature with different gate bias, and (b): on MOSFETs with different channel lengths (c) The third quadrant characteristics are compared at different temperatures and gate bias conditions.

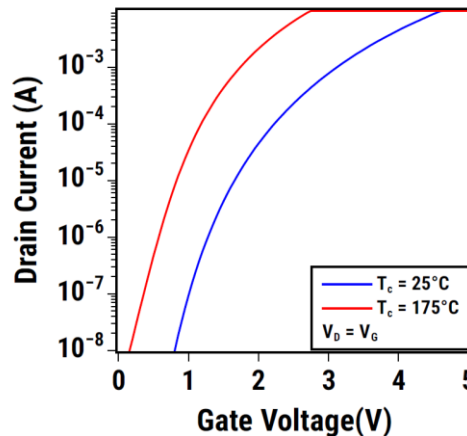


Figure 5: Transfer I-V characteristics measured on 25 mm² 15 kV SiC MOSFET die at room-temperature and 175°C.

Transfer Characteristics: The transfer I-V characteristics of a 25 mm² MOSFET at 25°C and 175°C are shown in Fig. 5. A gate threshold voltage (V_{TH}) of 3.2 V is measured at $I_D = 1$ mA at room-temperature, which drops to 1.8 V at 175°C. In the 10 nA – 1 μ A I_D range, an average sub-threshold slope (SS) of 240 mV/decade is extracted at 25°C, which drops to 206 mV/decade at 175°C – a lower SS at higher temperatures (and at lower drain bias) results from an exponentially decreasing acceptor trap density when moving away from the conduction band edge of SiC, towards the mid-gap. The density of interface traps is extracted from the room-temperature SS as 1×10^{13} cm⁻²eV⁻¹ in weak inversion, using the equation provided in [4].

Saturation Current Characteristics: The saturation current ($I_{D,SAT}$) characteristics measured on two 15 kV MOSFETs with different channel lengths (Fig. 6). A 20% lower $I_{D,SAT}$ was measured at $V_{DS}=600$ V, with near-identical $R_{DS,ON}$ under operating conditions. A lower $I_{D,SAT}$ is beneficial for increasing short-circuit withstand time, since it reduces the power dissipation during the short-circuit event. The short-circuit robustness of these devices will be reported elsewhere.

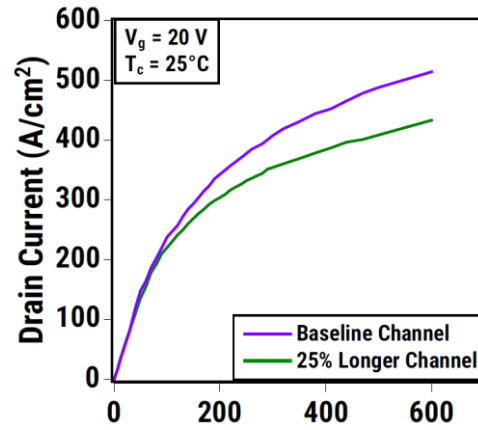


Figure 6: Saturation Current characteristics.

High-Temperature Gate Bias Stress: Several 15 kV SiC MOSFETs fabricated in this work were stressed for 60 hours at $V_{GS} = +20$ V in a 175°C oven. The evolution of the V_{TH} over time is shown in Fig. 7. After an initial increase, the V_{TH} saturates for the remainder of the stress time, similar to the 1200 V SiC MOSFETs reported in [5].

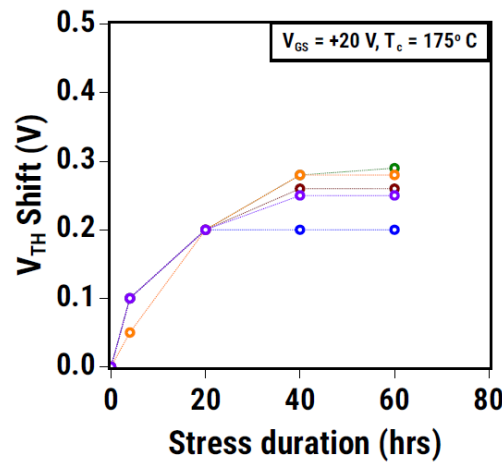


Figure 7: High-Temperature Gate Bias Stress Test.

Unclamped inductive switching (UIS): Unclamped inductive switching (UIS) was performed on a packaged 15 kV MOSFET at a peak drain current of 2.95 A (141 A/cm^2) with a 115 mH inductor at room-temperature, with $V_{GS} = 20$ V and $V_{DD} = 250$ V. We could not measure the drain voltage during the UIS waveform, due to equipment limitations for measuring such a high voltage. A single-pulse avalanche energy (E_{AS}) $\approx 22.1 \text{ J/cm}^2$ was achieved before the device failed catastrophically. A peak drain voltage of 18.9 kV can be inferred from the inductor discharging waveform (Fig.8), which is in line with the static breakdown voltage reported in Fig. 1.

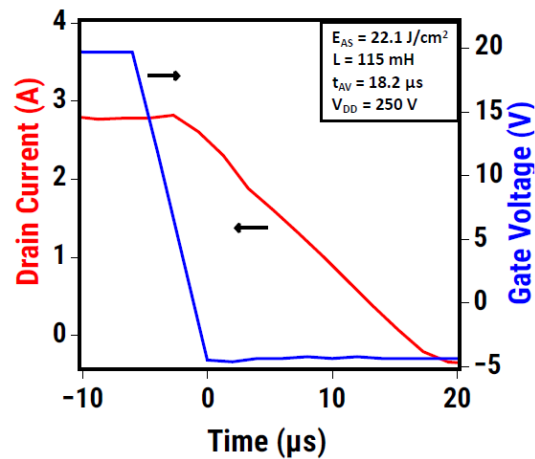


Figure 8: Unclamped inductive switching waveforms.

Acknowledgement

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References

- [1] A. Q. Huang et al, in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 118-130, 2017
- [2] A. N. Lemmon et al in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 309-322, March 2017
- [3] M.A. Capano et al. *J. Appl. Phys.* 87, 8773 (2000)
- [4] K. Tachiki et al. *Appl. Phys. Express* 14 031001 (2021)
- [5] S. Sundaresan et al. 2020 IEEE IRPS Proceedings pp1-4 (2021), doi: 10.1109/IRPS45951.2020.9128225