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Introducing Foundry-Compatible SiC and GaN Trench Processing Technologies for Reliable Automotive Application

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Abstract. In this paper we report the progress of our SiC trench etch development using enhanced ICP-based etch technology. Computer modelling of the electric field strength in the gate oxide as a function of corner geometry was used to illustrate trench corner rounding as an effective method to avoid to high gate oxide field strengths. This is an effort to examine a major ongoing issue in device reliability, and to govern future device design.

Introduction

High efficiency electric vehicles of the future will utilise wide bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) transistors (replacing silicon) in power electronic converters (PEC). With respect to SiC MOSFETs, device manufacturers are developing trench MOSFET (metal oxide field effect transistor) technology to increase the die per wafer and improve performance and reliability. The reliability of SiC and GaN based power devices is inherently related to the trench etch processes. Overcoming challenges relating to device fabrication and design of high voltage SiC and GaN trench devices is a prerequisite for widespread uptake in the automotive sector. Current SiC device structures are primarily MOSFET designs, while GaN device structures are typically based on high electron mobility transistors (HEMT) [1-2]. Trench based architectures offer competitive cellular pitches and greater current carrying capabilities, SiC trench MOSFETs being a prime example of state-of-the-art WBG technology.

This paper reports the development of an in-line SiC trench etch process technology suitable for high-volume GaN and SiC power device manufacture in a semiconductor foundry. Specifically, the trench etching capability demonstrated in this paper is applicable to classic SiC trench MOSFET architectures and GaN device structures based on vertical GaN-on-SiC MOSFETs (as opposed to HEMT) device structures. **Fig. 1.1** illustrates Gauss' Law of the electric field enhancement within the gate oxide of a SiC trench power MOSFET. Naturally the failure of the oxide due to increased electric field strength will be exacerbated when considering GaN, since the critical electric field strength in GaN is higher in magnitude compared to 4H-SiC.

From the device design perspective, one of the leading technologies specifically aimed at suppressing this enhanced gate oxide electric field is based on a double trench device design approach [3]. This design utilizes secondary trench structures in the sources area as a means of reducing the electric field concentration at the base of the gate trench, providing 50% reduced ON-resistances and 35% reduced input capacitance, compared with contemporary DMOS structure SiC-MOSFETs [4]. The challenges for realising foundry-ready trench etching processes for WBG materials are; (1) Micro-trenches or sharp corners, that induce the crowding of electric field in the corner of the trench, thereby reducing the breakdown field; and (2) Sidewall striations - having the effect of increasing the

leakage current through the gate oxide. Additionally, rounded corners on both the top and bottom of the trench must be processed for electric field suppression.

This paper reports developments in two distinct areas; SiC trench device simulation and SiC trench process etching.

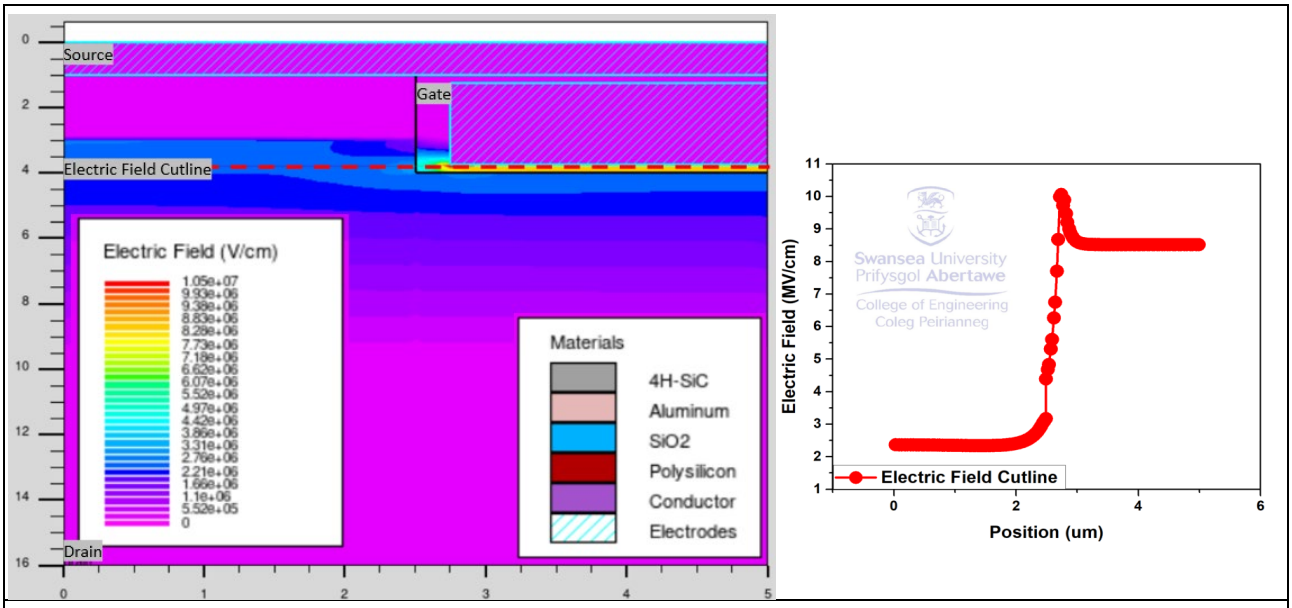

Fig. 1.1: Illustration of Gauss' law showing e-field enhancement in the gate oxide of a SiC trench MOSFET modelled using Silvaco TCAD. 2D trench MOSFET power device model including cutline (left) and the resultant plot of the Electric field magnitude against horizontal position (right).

Experimental Details

Etched SiC samples were fabricated as follows; a 2µm SiO_2 layer was deposited onto a 100mm SiC substrate using an SPTS PECVD tool. The substrate was prepared for photolithography by solvent cleaning and dehydration at 150˚C. Ti Prime adhesion promoter was deposited on the SiC wafer as a thin film, via spin coating. The wafer substrate was subsequently patterned using AZ® ECI 3012 positive photoresist. The method of patterning involved photoresist deposition by spin coating, exposure using a SUSS MA8 Gen5 Mask Aligner and development with AZ® 726 MIF developer. An oxide etch was performed using an SPTS APS tool. Following this, 2µm wide SiC trenches were etched to a depth of 1µm, also using the same etch system. Key SiC etch process parameters were 126s processing time, 900W ICP power, 500W electrode power, 10mT pressure, and gas flows of SF_6 39sccm, O_2 9sccm, and He 25sccm.

Results and Discussion

SiC ICP Etch

The SEM cross-sections presented in **Fig. 2.1** shows **(a)** the PR used to define the underlying oxide hard mask and **(b)** the remaining oxide hard mask after the SiC etch. An initial SiC etch rate of 526nm/min was achieved; which could be increased with further optimisation. The trench itself has a width of 2µm and a depth of 1µm. The sidewall angle is ~88˚ and there are no instances of micro-trenching observed. SiO_2/SiC selectivity however is quite low, at around 2:1.

Typical preliminary SiC etch rates reported elsewhere have been known to be as low as 200nm/min [5], so by comparison 526nm/min is a good starting point for further optimisation. Improving the SiC etch rate is key to processing trench MOSFET device architecture. Increasing the ICP power is known to increase the etch rate of materials such as Si, however for SiC increasing the bias power has been found to be more effective.

Currently SiO_2/SiC selectivity is roughly 2:1, with the SiO_2 hardmask noticeably etching and degrading **Fig. 2.1 (a) – Fig. 2.1 (b)**. For the 1um deep trench this is not a major issue, as **Fig. 2.1 (b)** shows that the SiC etch profile is near vertical, with no instances of micro-trenching and a sidewall angle close to 90˚. Nevertheless, it is clear from the etched SiO_2 profile, that further SiO_2 mask deformation will result in a compromised SiC etch. Therefore, improving the etch selectivity is crucial for further process development. Increasing process pressure should improve the etch selectivity, as SiC etch rate is known to improve as pressure increases to ~20mTorr, while SiO_2 exhibits an inhibited etch rate at this higher-pressure range [5].

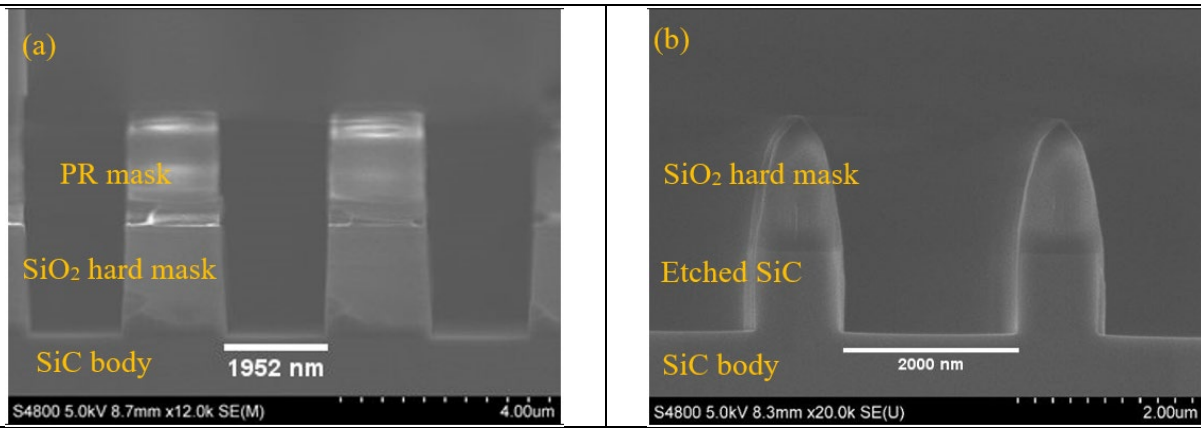

Fig. 2.1: SEM imaging of etched SiO_2 (a) and etched SiC using the SPTS APS tool (b). 2um trench width, 1um depth. Remnants of the SiO_2 hard mask are still visible, while the PR has been stripped post-etch.

SiC/SiO_2 Trench Device Simulation

When compared to silicon, one of the key benefits is the ability of SiC devices to operate at far larger electric fields. However, due to Gauss's law this material benefit turns into a major design challenge when the gate oxide of a MOSFET is concerned; the field in the oxide can reach up to 2.6 times the field in the SiC – which could result in a field as high as 10MV/cm in the gate oxide [6]. Additionally, in a trench MOSFET electric field crowds at the corners of the trench, causing the field values in the oxide to reach unacceptably high levels and thus fail at relatively low V_{ds} (compared to the theoretical maximum) under reverse bias conditions.

Simulations of SiC trench MOSFET structures, investigating the effect of the curvature of the trench etch on the electric field profile, were completed using Sentaurus TCAD. An example trench MOSFET structure, **Fig. 2.2 (a)**, was designed with a drift region doping of $1x10^{16}$ cm^{-3} shown in **Fig. 2.2(b)**. The radius of curvature of the trench bottom was varied, whilst keeping the depth & position of the trench constant (**Fig. 2.3**). This device was then simulated under reverse bias conditions of V_{ds}= 500V, 750V & 1000V, and the maximum electric field in the SiC region recorded at each voltage. For comparison, an identical reverse bias simulation was completed at each of the three bias points for a similar design with a sharp right-angle corner. There is a significant change in the field profile within the gate oxide as the trench radius of curvature increases; we observe a change in the electrostatic potential distribution, shown in **Fig 2.4**, alongside less electric field crowding at the corners of the gate oxide, as shown in **Fig 2.5**. The maximum field observed in the surrounding SiC layer is also reduces with increased trench curvature.

Device simulations show a decrease of ~0.1MV/cm SiC maximum electric field strength per 30nm of increased radius of curvature, as shown in **Fig. 2.6**. This rate of decrease in field strength is consistent across all three bias points. By increasing the radius of curvature of trench etch by 100nm, a decrease of 0.32MV/cm, 0.4MV/cm and 0.43MV/cm in field strength is observed at V_{ds}= 500V, 750V and 1000V, respectively. This equates to a ~17% decrease in field strength at all bias points simulated. When comparing the trench with the largest radius of curvature simulated (185nm) with a trench possessing a right-angle corner, a field decrease of 36% was observed at all three V_{ds} values.

These results carry even more significance when the magnitude of the electric field is considered. At V_{ds} = 500V, a drop of 0.78MV/cm field strength in the SiC would result in a drop of 2MV/cm in the gate oxide.

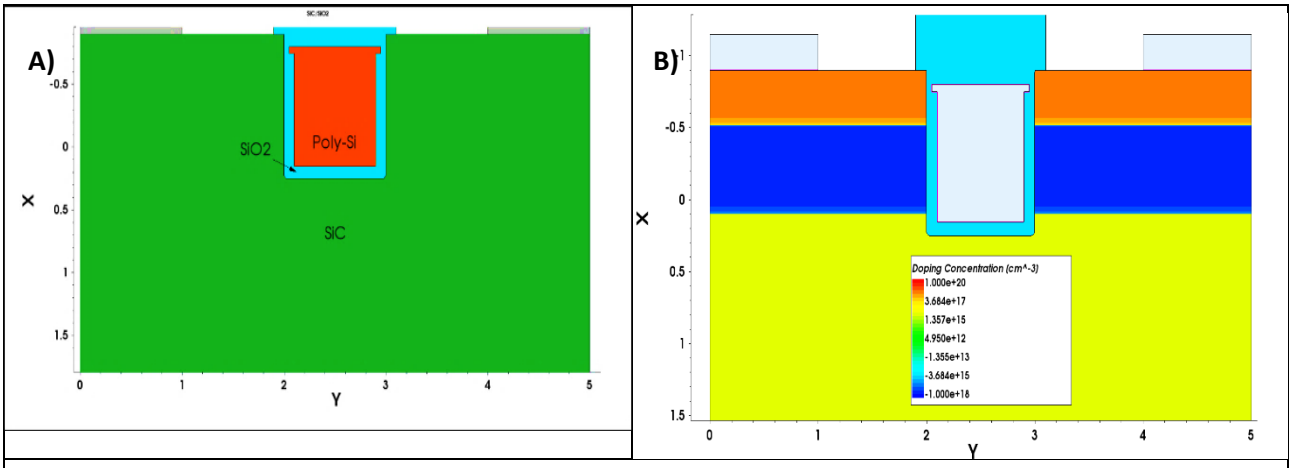

Fig. 2.2: a) Model SiC/SiO_2 trench cross section. b) Close up image of doping profile around the gate trench of the MOSFET.

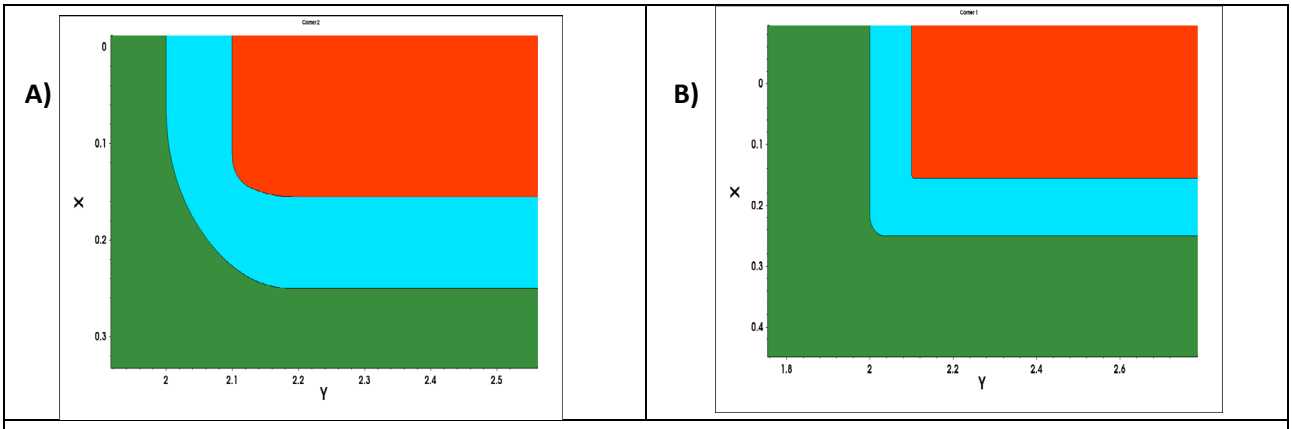

Fig. 2.3: Further model SiC/SiO_2 cross sections illustrating the variation of radius of curvature at the of the trench bottom. a) Extensive corner rounding – radius of curvature =185nm b) Minimal corner rounding – radius of curvature = 35nm.

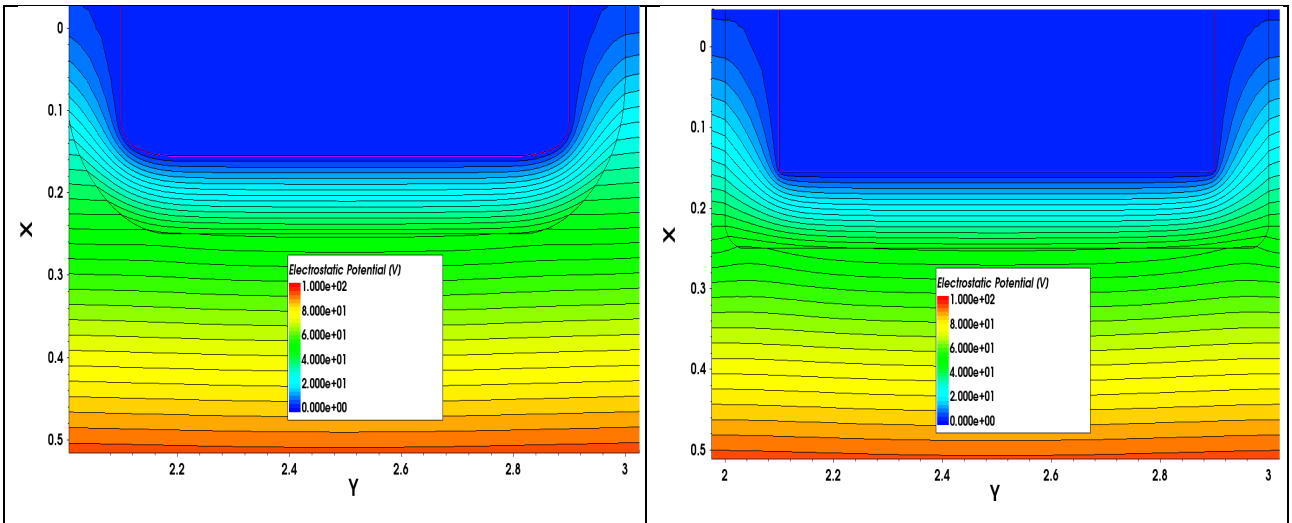

Fig. 2.4: Potential Distribution plot with contours at V_{ds} = 1000V a) Extensive corner rounding - radius of curvature = 185 nm b) Minimal corner rounding - radius of curvature = 35nm.

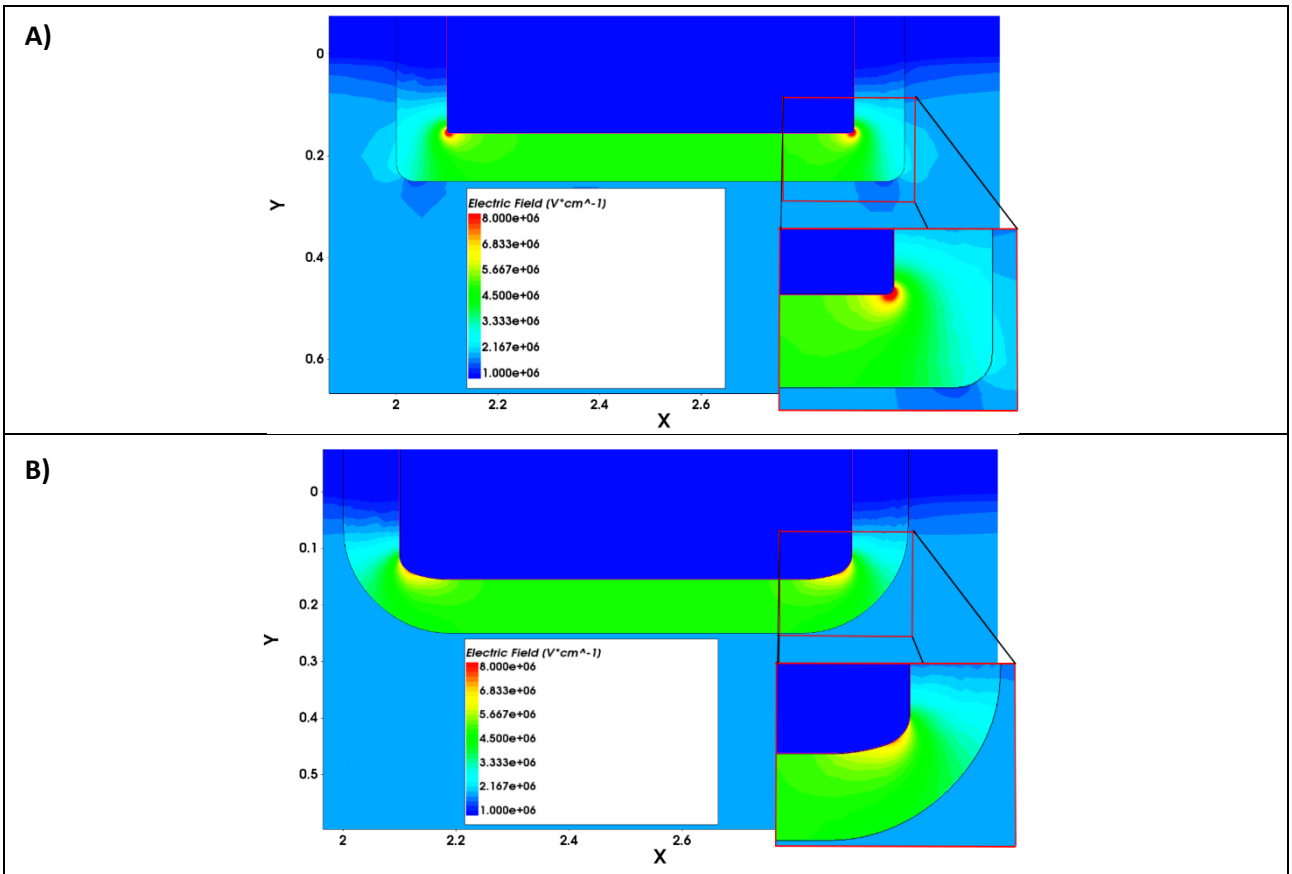

Fig. 2.5: Electric field profile of the gate trench at V_{ds} = 1000V b) Radius of curvature = 35nm b) Radius of curvature = 180nm.

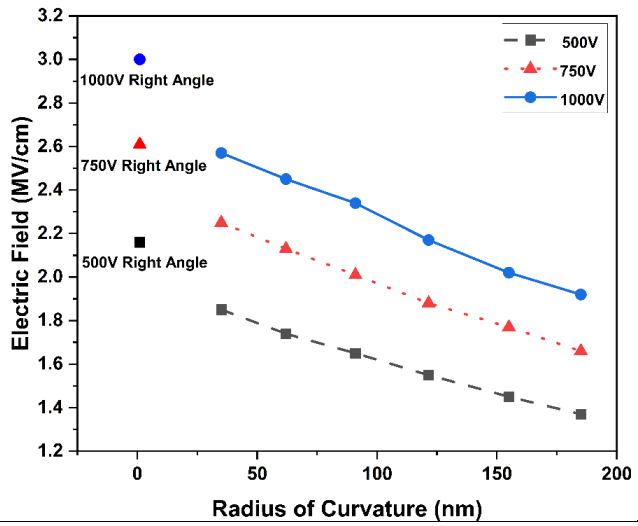

Fig. 2.6: Plot of trench bottom corner radius of curvature versus electric field strength at three different voltage ratings. Increasing radius of curvature reduces the maximum field observed at the SiC corner. The trend is observed irrespective of applied voltage.

Conclusion

In summary we have demonstrated development work on our SiC etch capability using an enhanced ICP-based etch tool from SPTS. The influence of several etch process parameters have been considered with a goal of optimising the SiC etch process. Future work on the SiC etch will aim to improve the etch selectivity as trench depth increases. Ultimately, high aspect ratio trenches with rounded corners should be achieved to facilitate fabricating a double trench device design. Additionally, the implied impacts of trench corner rounding on the gate oxide have been investigated using Sentaurus TCAD modelling. A decrease of ~0.1MV/cm SiC maximum electric field strength per 30nm of increased radius of curvature was simulated. This is promising, and work is ongoing to attain electrical characterisation results to confirm the model.

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