Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 598-602
doi:10.4028/p-64ey6u

Submitted: 2021-10-26
Revised: 2022-03-17
Accepted: 2022-03-17
Online: 2022-05-31

Compact Trench Floating Field Rings Termination for 10kV+ Rated SiC n-IGBTs

Neophytos Lophitis[1,a*], Peter M. Gammon[2,b], A. Benjamin Renz[2,c], Tianxiang Dai[2,d], Amit Tiwari[3,e], Tatjana Trajkovic[3,f], Philip A. Mawby[2,g], Florin Udrea[3,h], Marina Antoniou[2,i]

[1]Faculty of Engineering, University of Nottingham, Nottingham, UK

[2]School of Engineering, Warwick University, Coventry, UK

Department of Engineering, University of Cambridge, Cambridge, UK

[a*]neo.lophitis@nottingham.ac.uk, [b]p.m.gammon@warwick.ac.uk, [c]a.renz@warwick.ac.uk, [d]t.dai@warwick.ac.uk, [e]akt40@cam.ac.uk, [f]tt208@cam.ac.uk, [g]p.a.mawby@warwick.ac.uk, [h]fu@eng.cam.ac.uk, [i]marina.antoniou@warwick.ac.uk

*corresponding author: Neophytos Lophitis

Keywords: Silicon Carbide, Edge Termination, Trench, Floating Field Rings, IGBT.

Abstract. This work presents the design methodology and performance of a compact edge termination structure aiming 10kV+ rated Silicon Carbide (SiC) devices. Standard Floating Field Rings (FFRs) for such high voltage rating SiC devices are not favored because they are inefficient in terms of the achievable breakdown voltage as a percentage of the 1D maximum, consume large chip area, require high implantation energies and small gaps between rings which can violate fabrication limits. We show that the implantation of Aluminium at the bottom of carefully positioned trenches can be analogous to deep Aluminium implantation in terms of performance, thus annulling the need for small gaps between rings and MeV ion implantation. We optimize the distribution of trenches by placing them in multiple zones of different expansion coefficient. The proposed multi expansion ratio Trench FFR termination was utilized to terminate the active area of a 10kV rated Punch Through n-IGBT having 0.8 μm p-body and 100 μm, 3×10^{14} cm^{-3} drift region. We found the 0.6 – 0.8 μm to be the most optimum trench depth, achieving over 10 kV within less than 500 μm of termination length.

Introduction

Edge termination for 10 kV+ devices is an area of intense research. Floating Field Ring (FFR) termination is simple to process, repeatable and the effectiveness does not depend on dose variations. However, the chip area consumed at any voltage rating above 3.3 kV becomes very large, and the efficiency (achievable breakdown voltage as a percentage of the 1D maximum) reduces significantly. For example, FFRs designed for 5 kV achieved 76% efficiency and the termination length was 4.5× the drift region width [1]; FFRs for 27 kV IGBTs were only 48% efficient and the termination length was 6.5× the drift length [2]. This drop in efficiency and increase in termination length is attributable to the very shallow FFRs in SiC. The lack of impurity diffusion makes the formation of deep junctions impossible without resorting to MeV implants. Alternatively, Junction Termination Extensions (JTEs) are compact; however, compared to FFRs, JTEs have higher sensitivity to dose variations and to the presence of fixed charge. Adding multiple zones JTE rings and/or p+ rings requires extra calibration and implantation profiles but can increase the efficiency and stability [3]–[6].

We present a compact, scalable, and efficient Trench FFR termination design for 10 kV+ rated SiC devices. The Trench FFR design proposed in this work (shown in Fig.1) is implemented for SiC n-IGBTs featuring 100 μm wide drift region of doping concentration 3×10^{14} cm^{-3} [7]–[11]. The FFRs are implanted through the trench openings. An optimized electrostatic potential distribution which avoids weak points was achieved by splitting the termination in 4 zones, each having different expansion coefficient. The optimisation carried out includes the profile of the rings and the peak

concentration, the number of rings, the expansion ratio in each zone, the width and the depth of the trenches. Accurate and appropriate physics models and parameters have been used [12] to optimize the design with TCAD simulations. The results are discussed in the following section.

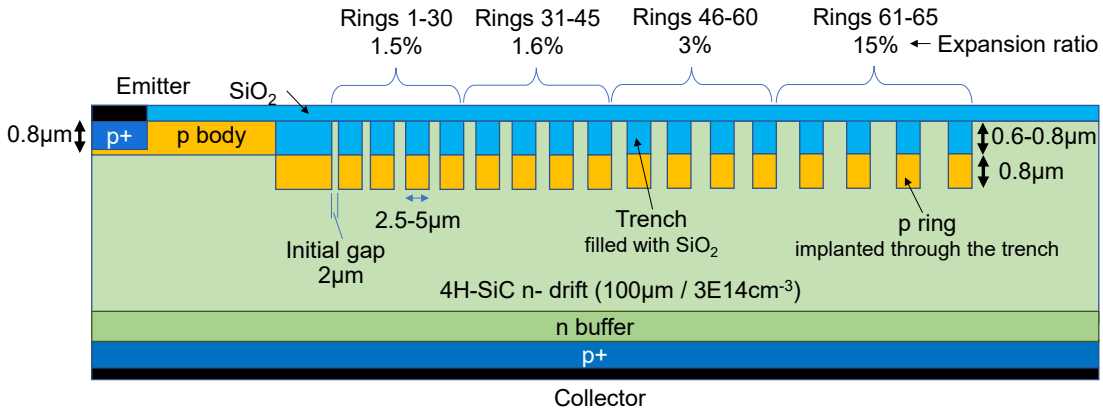

Fig. 1: Trench Rings edge termination design.

Results

The doping profile of the implanted p rings resulted from calibrated process simulations using Synopsys Advanced TCAD Sentaurus Process (SProcess). Fig. 2 depicts the final. The peak doping is at the bottom of the trench; it is near constant for 0.4 µm and then reduces with depth to achieve an effective p body/drift junction of depth ~0.8 µm. The selected profile helps avoid punch through and keeps the space charge at least 0.4 µm from the SiO_2. Any micro-trenches or small variations in the sidewall etching angle will be hidden/buried by the highly doped portion of the p ring, hence having very small or no impact. Device simulations were then conducted with Synopsys Advanced TCAD Sentaurus Device (SDevice) to optimise the distribution of rings and to assess the impact of trench depth and width in the achievable blocking voltage (BV). This multi-parameter, single objective optimisation procedure revealed that 65 rings implanted through trenches 0.6 – 0.8 µm deep and 2.5 – 5 µm wide can achieve 10.3 – 10.9 kV (~84 – ~89 % efficiency; 1D PNP breakdown voltage ~12.3 kV) when distributed in 4 expansion zones (Fig. 1), with a wide initial gap of 2 µm. A smaller initial gap, and the addition of rings and Al implantations can increase the blocking ability. The dependency of BV on the trench depth for trench widths of 2.5 µm and 5 µm can be seen in Fig. 3.

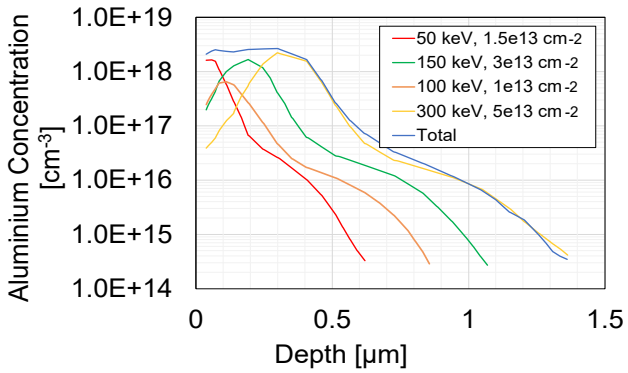

Fig. 2: Aluminium distribution of implanted Trench FFRs with calibrated SProcess simulations.

The impact of trench depth on the electric field profile is shown in Fig. 4. Shallow trenches and thus shallow FFR junctions result in a spike in the electric field close to the active area as the electric field pressure cannot be alleviated by the superficial p-ring junction for the same p-rings spacing; this can be solved only by reducing the initial distance and adding more rings. Deeper trenches result in an electric field spike at the edge of the termination because lower potential drop takes place in-between the p-rings; again, this can be addressed by adding more rings hence increasing the termination area.

While adding more rings is not a challenge, reducing the initial gap is limited by the processing capabilities of the foundry. Fig. 5 depicts the electric field distribution and electrostatic potential of an optimised arrangement (trench depth 0.8µm and width 2.5 µm) at 10 kV, whereby the electrostatic potential is fully dissipated within 450 µm (4.5× the drift region width). The peak electric field remains less than 2 MV/cm throughout, and less than 1.7 MV/cm at the surface (the SiO_2 interface).

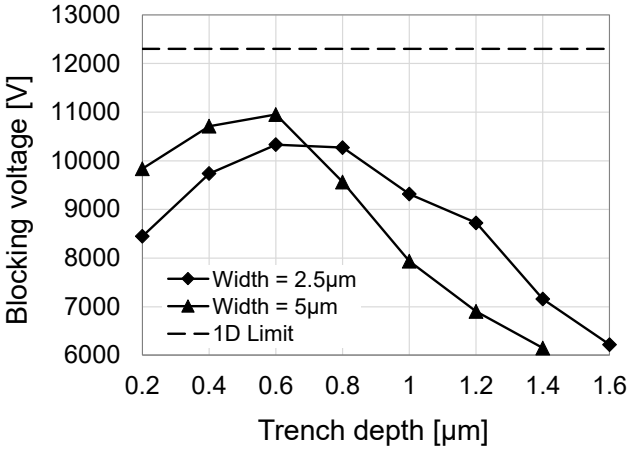

Fig. 3: Dependency of blocking voltage on the trench depth and width compared with the 1D PNP limit.

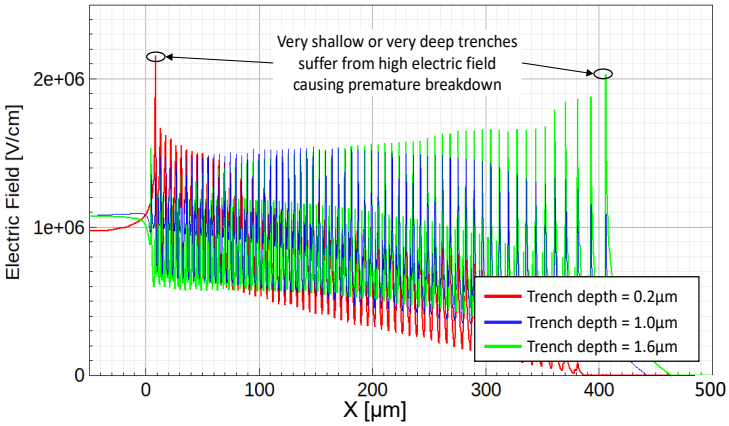

Fig. 4: Electric field (peak) distribution along the termination at 6 kV for trench depths 0.2 – 1.6 µm and trench width 2.5 µm.

Although the measurements from the optimized multi expansion zone Trench FFR termination are not available yet, initial experimental results compared to simulations of non-optimised Trench FFR designs featuring identical trench widths and implantation profile but having a fixed expansion ratio are shown in Fig. 6. They validate our simulation results for the specific design and our conclusion that ~ 0.8 µm Trench FFRs give the highest performance. They also validate their manufacturability.

Summary

FFRs are widely used in power devices due to their reliability and effectiveness. However, for 10kV+ rated SiC devices, they require deep junctions, or can consume large area and pose a challenge towards the fabrication of small ring spacing. By implanting aluminium at the bottom of trenches we show that the effective junction of FFRs in the edge termination region increases without the need to consult in MeV ion implantation. Trench FFRs placed in multiple zones of different expansion ratio, can be optimised to achieve over 10 kV, 84 % – 89 % efficiency and as little as 4.5× termination length to drift width ratio; while the required implantation energy is be kept low (< 300keV), the gaps between rings and trench dimensions are kept large (> 2µm and 2.5µm respectively) to enhance manufacturability. To achieve the same result with conventional FFRs, the implantation energy required is over 1 MeV which results in excessive damage and the requires thick masks.

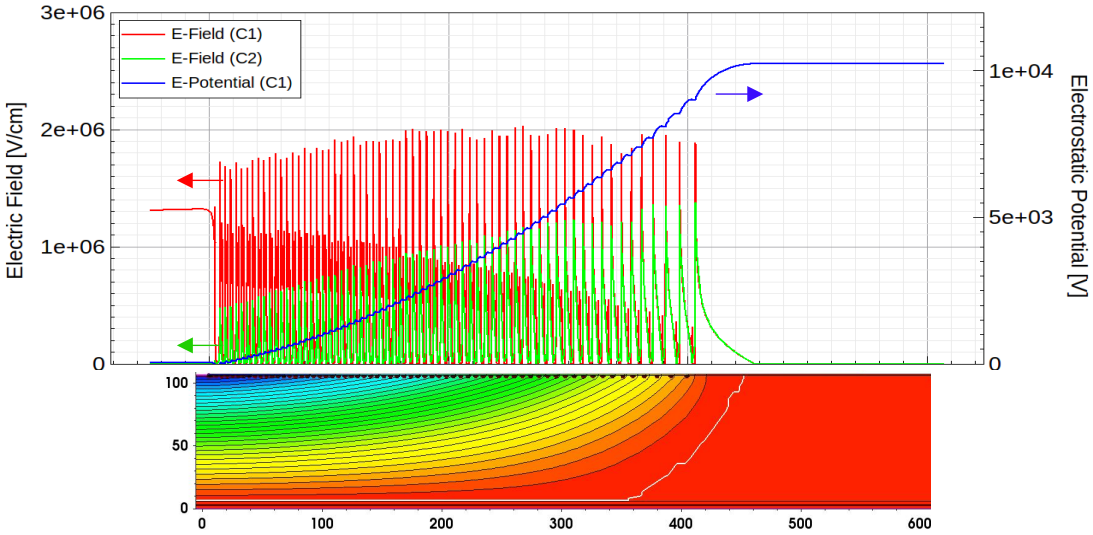

Fig. 5: Top image – Plot of electric field and electrostatic potential along a Y-cut passing through the peak E-field value (C1) and a Y-cut at the surface of the semiconductor (C2). Bottom image – Electrostatic potential contours depicting the smooth 2D distribution of the electrostatic potential in the termination area. Trench depth is 0.8µm, width is 2.5µm. All dimensions are in µm.

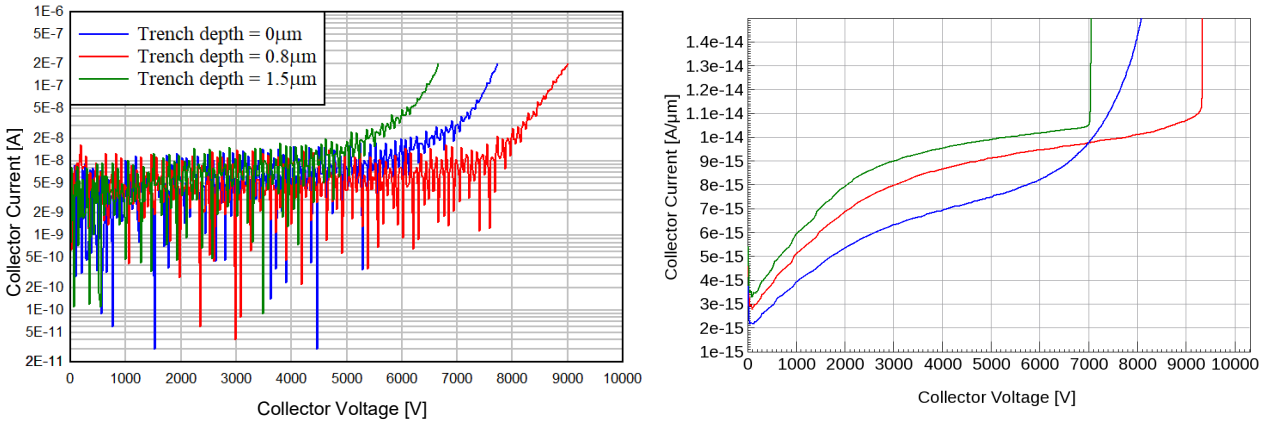

Fig. 6: Initial experimental results (left) compared to simulations (right) on Trench FFRs devices with (non-optimal) fixed expansion ratio.

Therefore, the proposed trench rings compare well with equivalently rated JTE structures [3, 4]. Furthermore, as with standard FFRs, the rings are expected to be of highly reliable due to the low electric field in the trenches oxide and to be largely independent of dose variations.

References

[1] W. Sung and B. J. Baliga, "A Comparative Study 4500-V Edge Termination Techniques for SiC Devices," *IEEE Trans. Electron Devices*, vol. 64, no. 4, Apr. 2017, doi: 10.1109/TED.2017.2664051.

[2] E. Van Brunt, L. Cheng, M. J. O'Loughlin, J. Richmond, V. Pala, J. Palmour, C. W. Tipton, C. Scozzie, E. Van Brunt, L. Cheng, M. J. O'Loughlin, J. Richmond, V. Pala, J. Palmour, C. W. Tipton, C. Scozzie, E. Van Brunt, L. Cheng, M. J. O'Loughlin, *et al.*, "27 kV, 20 A 4H-SiC n-IGBTs," in *Materials Science Forum*, 2015, vol. 821, pp. 847–850. doi: 10.4028/www.scientific.net/MSF.821-823.847.

[3] W. Sung, E. Van Brunt, B. J. Baliga, and A. Q. Huang, "A New Edge Termination Technique for High-Voltage Devices in 4H-SiC–Multiple-Floating-Zone Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 32, no. 7, Jul. 2011, doi: 10.1109/LED.2011.2144561.

[4] G. Feng, J. Suda, and T. Kimoto, "Space-Modulated Junction Termination Extension for Ultrahigh-Voltage p-i-n Diodes in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 59, no. 2, Feb. 2012, doi: 10.1109/TED.2011.2175486.

[5] S. Perkins, M. Antoniou, A. K. A. K. Tiwari, A. Arvanitopoulos, K. N. N. Gyftakis, T. Trajkovic, F. Udrea, and N. Lophitis, "Optimal edge termination for high oxide reliability aiming 10kV SiC n-IGBTs," in *2019 IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)*, Aug. 2019, pp. 358–363. doi: 10.1109/DEMPED.2019.8864919.

[6] X. Deng, L. Li, J. Wu, C. Li, W. Chen, J. Li, Z. Li, and B. Zhang, "A Multiple-Ring-Modulated JTE Technique for 4H-SiC Power Device with Improved JTE-Dose Window," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5042–5047, 2017, doi: 10.1109/TED.2017.2761995.

[7] A. K. Tiwari, F. Udrea, N. Lophitis, and M. Antoniou, "Operation of ultra-high voltage (>10kV) SiC IGBTs at elevated temperatures: benefits & constraints," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2019, pp. 175–178. doi: 10.1109/ISPSD.2019.8757586.

[8] A. K. Tiwari, M. Antoniou, N. Lophitis, S. Perkin, T. Trajkovic, and F. Udrea, "Retrograde p-Well for 10-kV Class SiC IGBTs," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 3066–3072, Jul. 2019, doi: 10.1109/TED.2019.2918008.

[9] A. K. Tiwari, M. Antoniou, N. Lophitis, S. Perkins, T. Trajkovic, and F. Udrea, "Performance Improvement of >10kV SiC IGBTs with Retrograde p-Well," *Mater. Sci. Forum*, vol. 963, pp. 639–642, Jul. 2019, doi: 10.4028/www.scientific.net/MSF.963.639.

[10] A. K. Tiwari, S. Perkin, N. Lophitis, M. Antoniou, T. Trajkovic, and F. Udrea, "On the robustness of ultra-high voltage 4H-SiC IGBTs with an optimized retrograde p-well," in *2019 IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)*, Aug. 2019, pp. 351–357. doi: 10.1109/DEMPED.2019.8864804.

[11] S. Perkins, M. Antoniou, A. K. Tiwari, A. Arvanitopoulos, T. Trajkovic, F. Udrea, and N. Lophitis, ">10kV 4H-SiC n-IGBTs for Elevated Temperature Environments," *14th Int. Semin. Power Semicond. (ISPS 2018)*, 2018.

[12] N. Lophitis, A. Arvanitopoulos, S. Perkins, and M. Antoniou, "TCAD Device Modelling and Simulation of Wide Bandgap Power Semiconductors," in *Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications*, Y. K. Sharma, Ed. Rijeka: InTech, 2018. doi: 10.5772/intechopen.76062.