Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 603-607
doi:10.4028/p-4vc4yb

Submitted: 2022-01-06
Revised: 2022-03-21
Accepted: 2022-03-22
Online: 2022-05-31

Fabrication and Characterization of Epitaxial Graphene Field Effect Transistor Devices Based on a Monolithic Bottom Gate

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Keywords: epitaxial graphene, silicon carbide, bottom gate, field-effect transistor (FET), electronic devices

Abstract. Current electronics technology increasingly demands higher integration, flexibility, higher efficiency, and performance aspects such as compatibility with higher temperature operation of the semiconductor devices, which may find limitations when silicon is used. The superior intrinsic properties of SiC, eventually combined with the ability of growing monolithically epitaxial, high quality graphene on a SiC wafer (1), makes it a reliable alternative for some electronic applications, such as field effect transistors (FET), radio frequency (RF) power amplifiers, integrated circuits (IC), or sensors. In this work, we describe the fabrication and preliminary electrical characterizations of epitaxial graphene (EG) on a SiC substrate FET devices based on an alternative back gate architecture. We propose a new approach in which the FET device is built on a 4◦ off-axis cut, N+ doped 4H-SiC substrate (the back gate) with, on top of, it a 1μm semi-insulating homoepitaxial layer of SiC compensated with vanadium (the dielectric layer). EG will be used as FET conduction channel. Using this V-compensated dielectric layer is aimed to minimize effects on the FET characteristics such as from defects in the SiC crystal, especially below the FET active areas, which would have occurred when using ion implantation to create a buried gate. The EG film was grown by the high temperature Si sublimation method under an Ar ambient. Raman spectroscopy, Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM) were applied in the structural characterization of epigraphene. The lack of D-peak in Raman spectra, together with SEM and AFM images, indicate that high quality monolayer to few layer epitaxial graphene fully covering the SiC surface is deposited. The electrical characteristics of the EG channel-devices and the functionality of the bottom gate were examined with 2-probe and 4-probe method. The electrical properties of the FET devices were also investigated with 3 terminal configuration.

Introduction

For more than 5 decades, Moore´s law has dictated the advancements in silicon technology. (2) However, the progressive demand for electronic devices with different performance capabilities, integration issues or higher efficiency, generated the need of new semiconductor materials to substitute or complement silicon-based electronics. Silicon carbide, SiC, is a foremost alternative as it combines unique physical and chemical properties, furthermore with the possibility of an monolithic, epitaxial growth of, high quality graphene on the SiC surface. Field effect transistors (FET), radio frequency (RF) power amplifiers and sensors are some of the promising electronic applications of epigraphene (EG) on SiC substrates. (1)

In this work, we describe the fabrication and preliminary electrical characterizations of EG FET devices on SiC substrate based on an alternative back gate architecture. The novelty of our approach is the use of a new material, the SiC doped substrate with the semi-insulating homoepitaxial layer, for the realization of back gated EG FET devices, towards high performance and low losses due to

leakage. Actually, in a previous work (3), the EG FET gate bias was based on using high-energy nitrogen implantation to form a buried N+ layer below the FET graphene channel. However, those devices exhibited high leakage current due to the damage generated in the SiC crystal by the implantation process, thus, here we want to eliminate this element by an alternative structure which exploits an advanced film recently enabled in the SiC electronic materials manufacturers (4).

Materials and Methods

The fabrication of this novel monolithic bottom gate architecture is based on a 4H-SiC, 4◦ off-axis cut N+ doped substrate, which acts as the back gate. On top of the substrate is a 1µm semi-insulating homoepitaxial layer of SiC compensated with vanadium, an innovative material that serves as the dielectric layer. This homoepitaxial layer was grown by chemical vapor deposition by II-VI Incorporated. (4) Photolithography patterning and Reactive Ion Etching (RIE) were implemented for the patterning of the areas to be selectively implanted with N. Ion implantation in SiC depends on many parameters that may affect significantly the crystal and its properties. (5) (6) For this reason, simulations for the depth distribution of the nitrogen dopants as a function of the implantation dose, were performed and showed that the optimal thickness of the selectively implanted area was 300nm for a doping level of 10^{19}-10^{20} cm^{-3}. As a result, the areas that we wanted to operate as vertical conductive channels, should be firstly etched so we could reach the doped substrate (back gate). The dopant activation was a termal annealing at 1650˚C with a protective capping layer in order to prevent Si desorption from the SiC surface. EG was grown by high temperature Si sublimation method, in particular at 1750˚C under an Ar ambient flow. The structural characterization of epigraphene was performed by AFM, SEM and Raman Spectroscopy. For the fabrication of FET devices, e-beam Lithography (EBL) plus RIE was used to pattern the graphene channels. EBL was also used for the patterning of electrical contacts, in combination with thin film metal evaporation (Ti+Au) followed by resist lift off. In order to understand accurately the gate functionality, a reference sample without EG was also fabricated. In this case, Ni was sputtered as a metal contact on top of the selectively implanted areas as well as the backside of the sample. The complete architecture of our samples is shown as a cross-section scheme in Fig.1 along with an SEM cross section image of the layers stack at the implanted area in the reference sample. The latter displays a Ni metal contact, instead of the Ti+Au used in EG samples. For device evaluation, the electrical characteristics of the bottom gate and the graphene FET devices were tested.

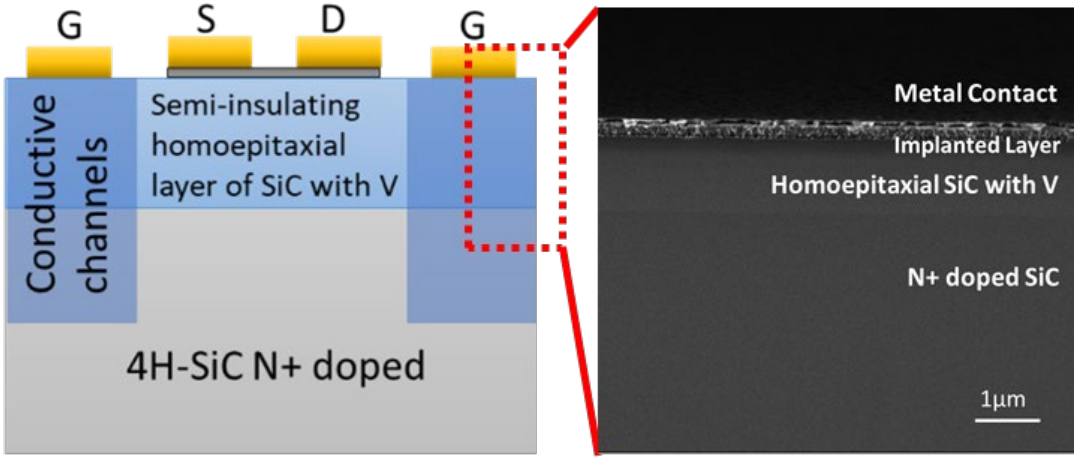

Figure 1: Cross-sectional scheme of our new approach of an EG FET device. Darker grey thin film on top of the homoepitaxial SiC layer is the patterned EG to be used as FET conduction channel. With a closer look on the implanted area of the reference sample we can see in the cross section SEM the distinctive layers of the homoepitaxy, selective implantation and gate metal contact.

Results

Firstly, we provide the structural characterization of the sample. AFM and cross-sectional SEM shown in Fig. 2 and Fig. 3, respectively, confirm that RIE step between the implanted and non-implanted area is ~ 680nm±5nm. Differences in the surface smoothness (step bunching due to EG growth) can be seen (Fig. 2). Epitaxial graphene was also characterized by SEM and AFM which showed an homogeneous and complete cover of the step-structured SiC. By AFM phase signal displaying, we can also identify the distinctive graphene wrinkles across the step edges of the SiC terraces (Fig.4). The EG quality and the number of graphene layers were analyzed by Raman Spectroscopy. The Raman spectra show a very low D peak, thus, indicating the pristine graphene quality, as its intensity would increase with the presence and amount of both structural and chemical defects. Moreover, by Raman mapping several large areas (typically 90μm×150μm), we showed that the films consist in single layer EG stripes, as for example the bright yellow stripe of Fig.5, surrounded by few layer graphene.

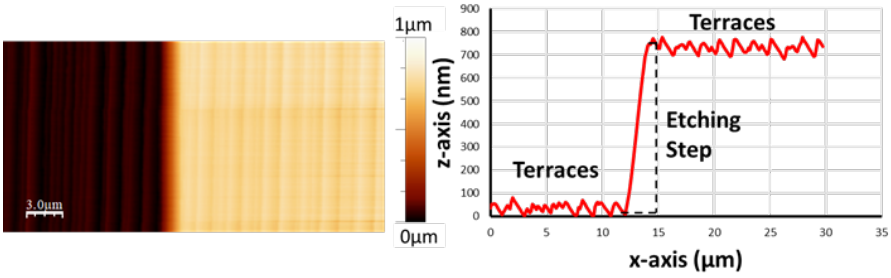

Figure 2: AFM topography image and section of the etching step transversal to the SiC steps/terraces. (Scan size: 15×30μm, z-scale: 1μm). RIE step depth (680nm) confirms that intended conductive channel thickness of ~ 300nm could be implemented. Smaller and narrower terraces also formed on both implanted and non implanted areas with no significant differences.

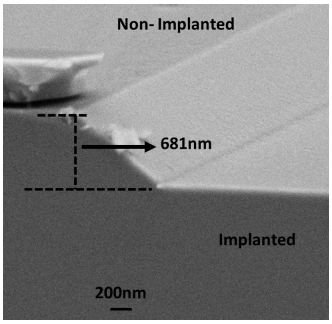

Figure 3: Cross section SEM image showing the etching step between the implanted and non implanted area.

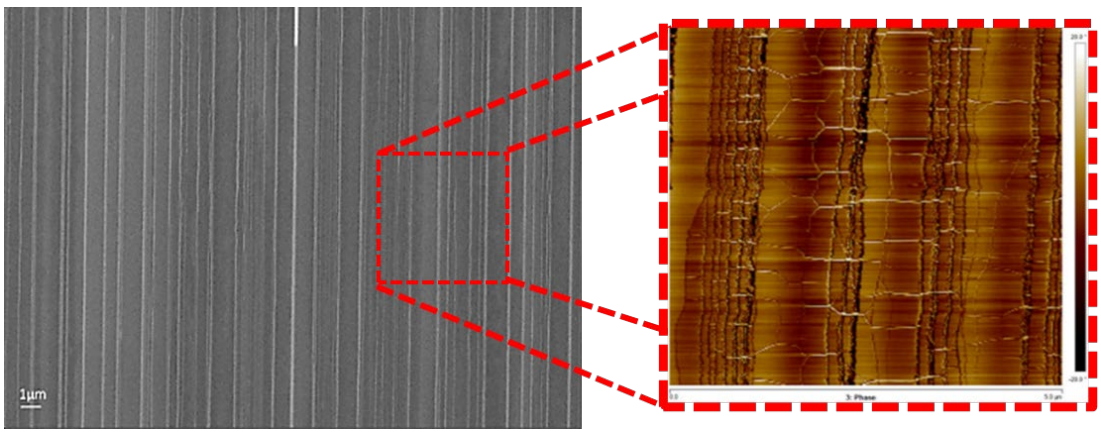

Figure 4: SEM Image of the EG homogeneously and fully covering the terrace/step-structured SiC surface. Detail of the EG material can be seen by Phase signal AFM Imaging (Scan size: 5×5μm, z-scale: 10°), particularly the characteristic EG wrinkles across the SiC steps and terraces.

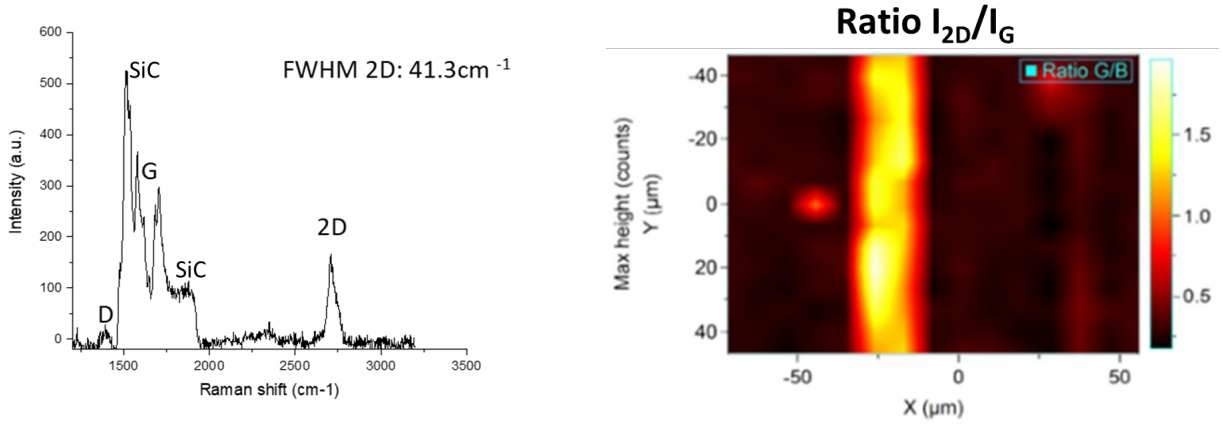

Figure 5: Exemplary Raman Spectrum (Left) with the characteristic graphene peaks (D,G,2D) and Raman Mapping (Right) showing a single layer graphene stripe, presented in bright yellow, surrounded by few layer graphene, the darker red areas.

The functionality of the back gate and the vertical conductive channels were examined by electrical testing with 2- and 4-probe methods at room temperature. The electrical testing in the reference sample shows Ohmic behaviors. Applying the transfer length method (TLM) measurements, we applied current in the back gate contacts from the sample top side increasing the spacing between them, we could plot the total resistance R_T versus contact spacing d. From these results the contact resistance (Rc) was obtained by extrapolation and is estimated at 52.5mΩ as shown in Fig.6.

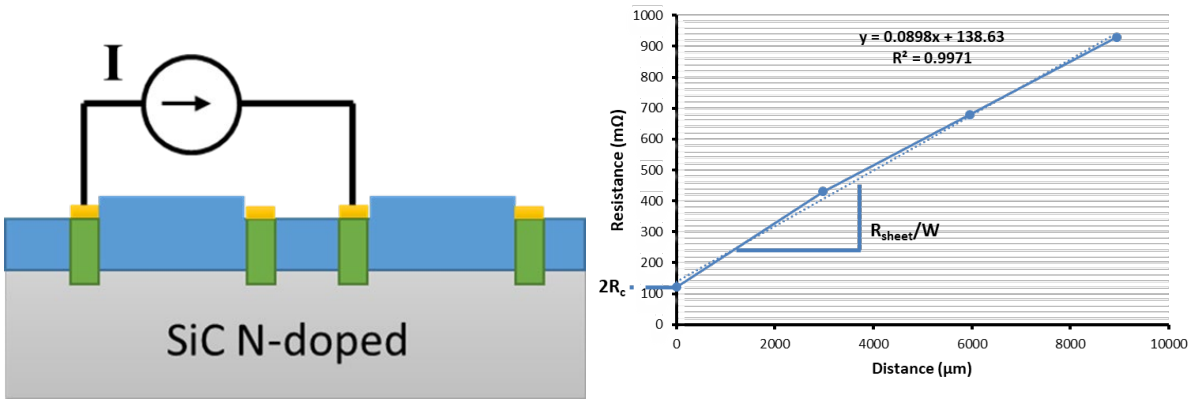

Figure 6: TLM measurements contacting the back gate metal contacts for the study of the buried gate actuation. Plotting RT as a function of d allows the estimation of Rc by extrapolation at 52.5mΩ.

Finally, the fabricated FETs were as well electrically tested. Although no lateral leakage current was detected, the vertical leakage current across the insulating epilayer becomes important, in the order of µA, after an applied gate voltage of V_G=2V.The semi-insulating homoepitaxial layer shows a rectifying behavior, where dominates the leakage current and there is no gate bias-induced charge carrier modulation of the EG channel.

Summary

An alternative monolithic bottom gate architecture for the fabrication of EG-FETs is proposed with the use of a novel material, a homoepitaxial layer of SiC compensated with Vanadium (insulating) on top of a doped SiC substrate (conductive). This approach eliminates the implantation-induced defects in the SiC crystal, potentially better-preserving the high quality of epigraphene. The electrical characteristics of the back gate proved the functionality of the gate and the selectively implanted conductive vertical channels. However, from the electrical testing of the gate, leakage current from the homoepitaxial layer of SiC compensated with Vanadium was detected, affecting the operation of the FETs. The loss of insulating properties of the homoepitaxial layer is attributed to the two applied

high temperature two annealing steps implied in the fabrication processes, specifically, the activation of the dopants and the epitaxial graphene growth. As a result adjustments are needed, for example the use of a single thermal annealing step for both processes could preserve the epilayer's properties. Furthermore, the functionality of the gate and the performance EG FET devices in low temperatures are being studied and the results will be reported in the near future. Based on this architecture more sophisticated devices such as doubly-gated EG-FET devices can be realized.

Acknowledgments

This work was supported by DOC-FAM project, which has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 754397. G.R. acknowledges Ayudas Ramon y Cajal Grant Ref. RYC-2016-21412.

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