

Clamped and Unclamped Inductive Switching of 3.3 kV 4H-SiC MOSFETs with 3D Cellular Layouts

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Abstract. This work presents for the first time a comparative numerical study on the performance of planar 3.3 kV SiC MOSFETs during clamped and unclamped inductive switching for various cell layouts and pitches. It is demonstrated that despite its larger on-state losses, the atomic lattice layout (ALL) incurs smaller switching losses than the stripe and the circular designs for all examined cell pitches. Conversely, while the ALL does turn off earlier than the other layouts during UIS, the decrease in the peak lattice temperature that it brings is predicted to be marginal if just a single unit cell is considered.

Introduction

The advantageous material properties of SiC have recently made 4H-SiC MOSFETs attractive for various power applications. In particular, the superior performance trade-off (between the specific resistance R_{on}^* , the breakdown voltage V_{br} , and the total switching time t_{switch}) that SiC MOSFETs offer compared to Si devices have allowed for improvements in the efficiency and the reliability of the power system, enabling operation at a higher junction temperature [1]. Nevertheless, despite these advantages of the semiconductor, the increased power density in SiC MOSFETs can aggravate the heat extraction process and hence compromise the reliability of the packaging and the metallisation.

In this context recent studies have looked into the possibility to alleviate these issues by using advanced cellular layouts [2, 3]. However, while the static behaviour of these 3D designs is now well understood [2-4], the variation of their dynamic response during both nominal and fault switching conditions, such as unclamped inductive switching (UIS), with the cell pitch W_{cell} requires further study. The latter case becomes particularly important at high V_{br} ratings of 3.3 kV and above. That is why this work proposes a comprehensive numerical study on the electro-thermal performance of 3.3 kV planar 4H-SiC MOSFETs during both UIS and clamped inductive switching for three different cell layouts (stripe, circular, and the atomic lattice layout [4]) at a range of cell pitches.

Methodology

The layouts of the examined 3.3 kV designs can be observed in Fig. 1. Here the circular and the ALL are simulated in 2D by solving the drift-diffusion equations for the unit cell in cylindrical coordinates around their respective axis of symmetry. The drift region has a thickness of 30 μm and is doped n-type at $3 \times 10^{15} \text{ cm}^{-3}$, while the p-well is implemented using a retrograde profile matched to a process simulation [5]. A channel length of 300 nm is assumed, with the acceptor doping at the surface being $\sim 2 \times 10^{17} \text{ cm}^{-3}$. The interface is described using the D_{it} distribution for the Si-face from [6] (assuming only acceptor states above the midgap level), along with a positive fixed charge density of $1.75 \times 10^{12} \text{ cm}^{-2}$. In turn, the p-short contact half-width is set to 2 μm . The cases with a different cell pitch are obtained by adjusting the width of the JFET region, while the termination area is neglected.

The above structures are implemented in Sentaurus TCAD [7] and are then inserted into the circuit in Fig. 2 (without the freewheeling diode for UIS mode). Here the unit cells are scaled so as to get an

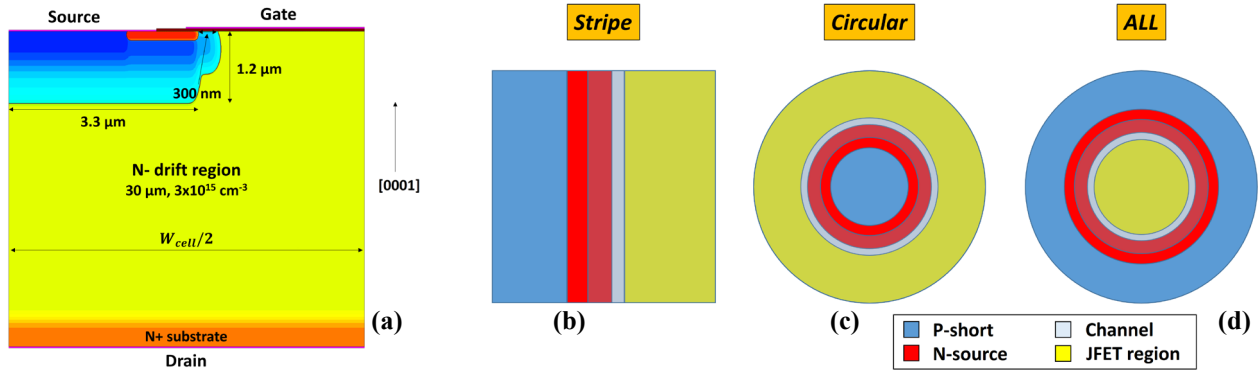


Fig. 1: Cross-section of a half unit cell of the examined 3.3 kV MOSFET (a) and top views of the stripe (b), circular (c), and ALL (d) topologies (drawn to scale for a 12 μm cell pitch). The darker tones in (b-d) signify the area over which the gate oxide is placed.

active area of 0.15 cm^2 . A default diode from the TCAD's in-built SPICE library in [7] is used for the clamped inductive switching case. Conversely, a fixed thermal resistance of 0.3 $\text{cm}^2\text{K/W}$ is placed at the drain for UIS mode. Unless otherwise stated, all subsequent results are for $W_{\text{cell}} = 12 \mu\text{m}$.

Results and Discussion

The performance of the above designs is first examined at nominal inductive switching conditions for an on-state drain current of 100 A/cm^2 . In agreement with [4], the circular design is found to have the lowest resistance of all layouts for typical values of W_{cell} (Fig. 3 (a)). Conversely, the ALL attains a comparable R_{on}^* only at larger W_{cell} due to its saddle junction, which increases the channel, JFET, and spreading resistances for small W_{cell} (although it also increases the breakdown voltage compared to the other layouts (Fig. 3 (b)). Still, this drawback of the ALL should be less important at a higher V_{br} rating (and JFET doping), where the drift region forms the dominant contribution to R_{on}^* .

On the other hand, from Fig. 4 (a-b) it can be seen that the ALL (circular) attains the fastest (slowest) response of all layouts during both turn-on and turn-off (for a 12 μm cell pitch). In particular, the ALL exhibits a shorter Miller plateau during both switching instances. These results are confirmed by the C/V waveforms in Fig. 5, where the ALL's C_{gd} is an order of magnitude smaller than in the other designs. This drop of the Miller capacitance arises from the wider lateral extension of the depletion region brought about by the ALL's saddle junction (as seen by the sharper slope of C_{gd} at $V_{\text{ds}} \sim 0 \text{ V}$) and also from the smaller gate contact area (and hence weaker gate-drain coupling) of the ALL compared to the other designs. The ALL can hence be expected to display a smaller C_{gd} and lower switching losses also at other W_{cell} values. Nonetheless, the smaller C_{gd} of the ALL also leads to notably larger oscillations in the drain current I_d at turn-off if the same gate resistance R_g is used for all layouts (Fig. 4 (b)). Thus, it may become necessary to employ a larger R_g so as to reduce dI_d/dt and hence obtain a cleaner turn-off waveform (albeit at the cost of increased switching losses).

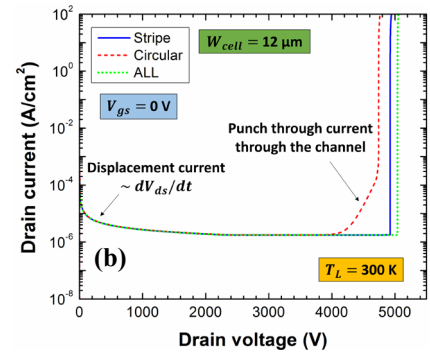
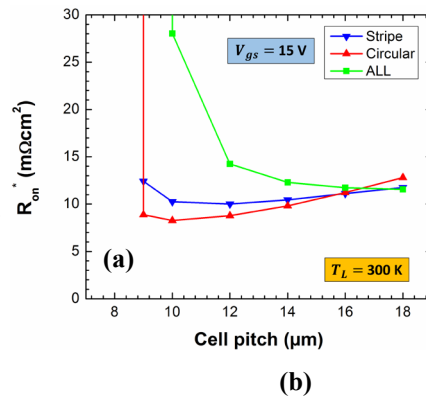
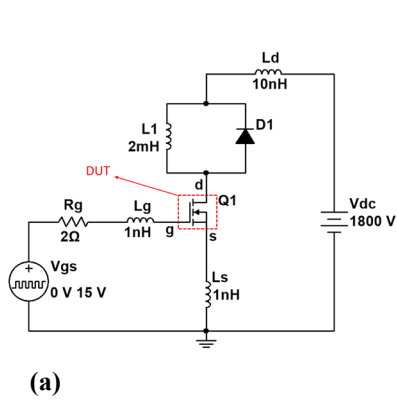


Fig. 2: Circuit used for the switching simulations. The diode D_1 is removed for UIS mode.

Fig. 3: Variation of R_{on}^* with W_{cell} (a) and off-state I/V curves (b) of the examined designs. The ALL has the highest V_{br} , yet its R_{on}^* becomes competitive only at large W_{cell} .

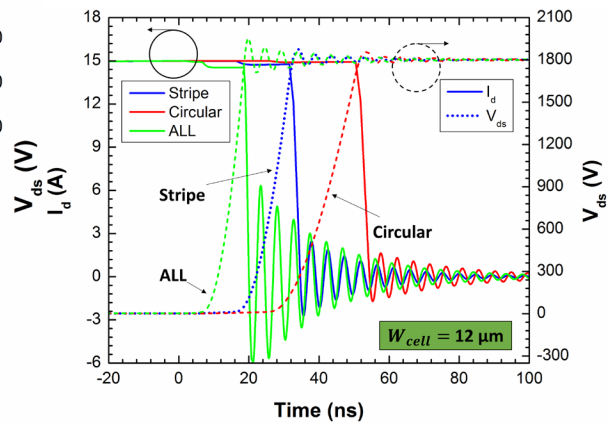
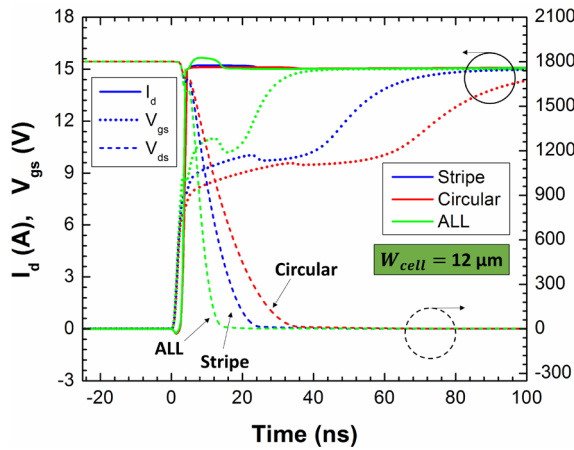


Fig. 4: Turn-on (a) and turn-off (b) characteristics of the examined layouts (for a cell pitch of 12 μm) during clamped inductive switching. The ALL (circular) displays the fastest (slowest) response with the smallest losses, yet it also exhibits increased oscillations.

The variation of the switching responses with W_{cell} can be seen in Fig. 6. Here the losses are computed using the electron current through the channel (hence power dissipation due to capacitive charging is neglected). It can be observed that both E_{loss} and the switching time t_{switch} (defined as the sum of the 0/95 % rise time of V_{gs} during turn-on and the time until the first zero-crossing of I_d at turn-off) increase monotonically with W_{cell} for each layout due to the larger C_{gd} (and hence wider Miller plateau) of the structures with a bigger pitch. The ALL not only has the fastest response for all cases, but the reductions in E_{loss} and t_{switch} that it produces grow at larger cell pitches. At the same time, the amplitude of the observed oscillations falls as W_{cell} is increased (thanks to the larger C_{gd}). Conversely, at small W_{cell} the ALL's advantage in E_{loss} weakens and gets overruled by its larger R_{on}^* .

The responses of the structures during UIS (with D_1 removed) are now presented in Fig. 7 (a-c). Although the differences between the layouts are rather small as only a single scaled unit cell is considered, the ALL (circular) still clearly dissipates the inductor current I_d faster (slower) than the others. This can be explained with the larger (smaller) breakdown voltage V_{br} of the ALL (circular) (Fig. 3 (b)) due to its saddle (cylindrical) junction [4]. Indeed, since the voltage across the load L_1 is $-L_1 \times dI_d/dt \approx (V_d - V_{dc})$, I_d should fall faster in a layout with a larger drain voltage V_d . The more rapid turn-off of the ALL is found to compensate for the extra heating due to the larger V_{ds} , allowing it to attain the lowest peak temperature T_{max} (and E_{loss}). Nonetheless, this reduction is only ~ 10 K (≈ 2 %).

The same trend can also be seen at other cell pitches (Fig. 7 (d)). Here both the turn-off time $t_{turn-off}$ and the peak T_{max} increase with W_{cell} for all layouts due to the corresponding drop of V_{br} with W_{cell} .

The lowest (highest) degree of self-heating is again attained by the ALL (circular). Still, although the performance differences become somewhat clearer at larger W_{cell} (due to the greater variation of V_{br} with the layout), the ALL's advantage during UIS (in case of a single unit cell) remains negligible.

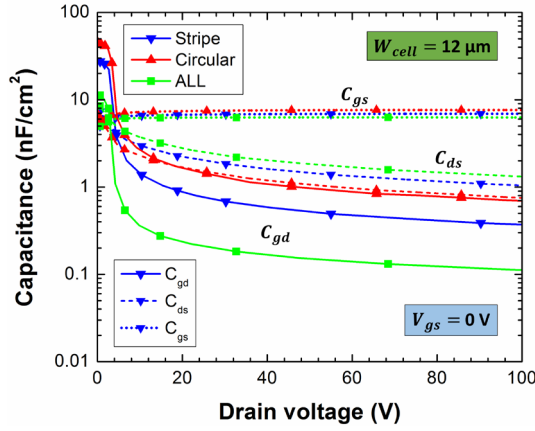


Fig. 5: C/V waveforms of the examined layouts for a W_{cell} of $12 \mu\text{m}$. The ALL (circular) displays the smallest (largest) C_{gd} and C_{gd}/C_{ds} ratio.

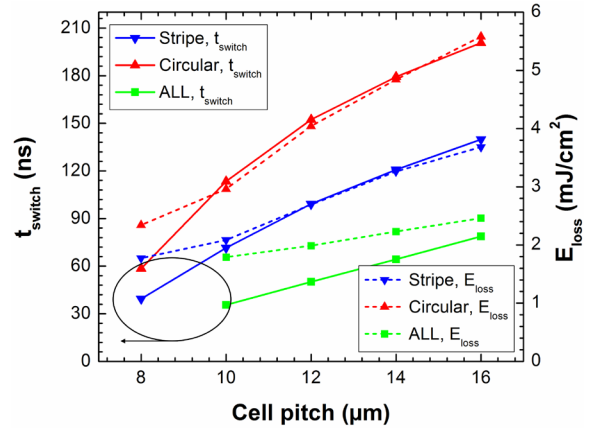


Fig. 6: Evolution of the switching time t_{switch} and the total switching losses E_{loss} with the cell pitch W_{cell} .

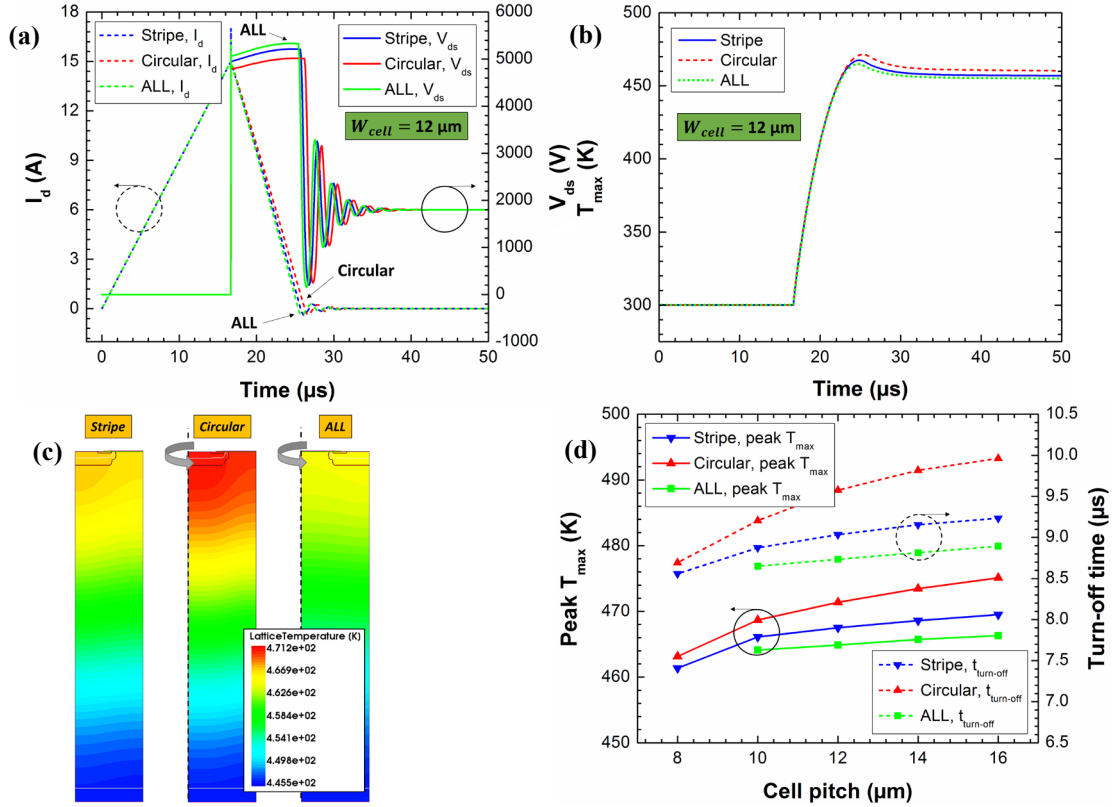


Fig. 7: I_d/V_{ds} (a) and T_{max} (b) responses of the layouts during UIS, lattice temperature profile (for $W_{cell} = 12 \mu\text{m}$) at time $t = 25 \mu\text{s}$ (c), and evolution of the UIS response with W_{cell} (d).

Conclusion

In this paper the impact of the cell layout and the cell pitch on the switching speed and losses of 3.3 kV planar SiC MOSFETs has been investigated numerically. It has been shown that while the circular design attains the lowest R_{on} , it incurs larger switching losses than the other layouts. At the same time, the ALL attains the smallest E_{loss} thanks to its reduced C_{gd} and hence becomes competitive for designs with a sufficiently large pitch. Conversely, the improvement during UIS due to the isolated effect of the ALL's unit cell is predicted to be marginal. In order to assess if this advantage of the ALL can become truly significant in a real device, the entire die needs to be considered in the analysis.

References

- [1] A. Q. Huang, Power Semiconductor Devices for Smart Grid and Renewable Energy Systems, Proceedings of the IEEE 105 (2017) 2019-2047.
- [2] X. Q. Liu et al., Impact of cell geometry on zero-energy turn-off of SiC power MOSFETs, Material Science Forum 924 (2018) 756-760.
- [3] A. Agarwal, K. Han, and B. J. Baliga, Impact of cell topology on characteristics of 600V 4H-SiC planar MOSFETs, IEEE Electron Device Letters 40 (2019) 773-776.
- [4] B. J. Baliga, Fundamentals of power semiconductor devices, Springer Science & Business Media, 2010.
- [5] L. Knoll et al., Planar 1.2 kV SiC MOSFETs with retrograde channel profile for enhanced ruggedness, 31st International Symposium on Power Semiconductor Devices and ICs (2019) 211-214.
- [6] H. Yoshioka, T. Nakamura, and T. Kimoto, Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance, Journal of Applied Physics 111 (2012) 014502.
- [7] Sentaurus Device User Guide, Synopsys, Mountain View, CA, USA, 2019.