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On the Short Circuit Electro-Thermal Failure of 1.2 kV 4H-SiC MOSFETs with 3D Cell Layouts

Nazareno Donato[1,a*], Kaloyan Naydenov[1,b], Florin Udrea[1,c], Andrei Mihaila[2,d], Gianpaolo Romano[2,e], Stephan Wirths[2,f] and Lars Knoll[2,g]

[1]Department of Engineering, University of Cambridge, Cambridge, UK.

[2]Hitachi ABB Power Grids, Semiconductors, Lenzburg, Switzerland.

[a]nd391@cam.ac.uk, [b]kn334@cam.ac.uk, [c]fu1000@cam.ac.uk, [d]andrei.mihaila@ch.abb.com, [e]gianpaolo.romano@ch.abb.com, [f]stephan.wirths@ch.abb.com, [g]lars.knoll@hitachi-powergrids.com

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Abstract. In this manuscript, the short circuit (SC) capability of 1.2 kV vertical double diffused SiC MOSFET with different layout topologies is investigated. 3D finite element electro-thermal simulations have been carried out in order to assess the performance of five different cell topologies. It has been found that while the maximum drain current density observed during a SC event agrees well with the specific on-state resistance behaviour, the maximum temperature evolution in the unit cell follows the opposite trend. This behaviour can be explained by the relatively poor spreading of the carriers in the JFET region (of the atomic lattice layout (ALL)) at small cell pitches (CP) ~ 8 μm, which can lead to the formation of a filament with a high current density and heat generation.

Introduction

Initially manufactured for the 600 V range by Rohm in 2010 and immediately followed by the first commercial 1.2 kV 4H-SiC MOSFET from Cree, SiC MOSFETs are now commercially available in either discrete or module configurations mainly for automotive and traction applications. Regarding 1.2 kV 4H-SiC MOSFETs, manufacturers have opted for different cell designs (symmetric/asymmetric trench, planar etc.), in order to tackle issues related to the low mobility at the Si-face, dielectric reliability, gate charge hysteresis, NBTI and PBTI, and bipolar degradation[1-2]. Compared to Si-counterparts, SiC MOSFETs allow for an increased power density and maximum junction temperature (Tjmax), while improving the efficiency and reducing the size of the power electronic system. While the maximum junction temperature itself does provide a useful indication of the device's resistance towards abnormal electrical events such as unclamped inductive switching (UIS) and short circuit (SC), fast thermal transients due to the high-power density are often what limits the reliability of the device, the metallization, and the packaging material[3]. In this context, advanced unit cell topology could be beneficial in suppressing the contribution related to the channel resistance and reducing the fast dT/dt. In Si, the unit cell layout is known to affect several static (specific on-state resistance ($R_{ON}S$) and breakdown voltage BV) and dynamic (C_{GD}/C_{GS} ratio) electrical characteristics of the power MOSFET [4]. Nevertheless, to date, the impact of the cell layout on the short circuit (SC) performance has not been reported yet in the literature. Thus, this study presents a complete investigation on the thermal runaway failure mechanism for several SiC MOSFET layouts. This type of failure mechanism is obtained when the thermally generated carrier concentration exceeds the background doping concentration and the device reaches an intrinsic state with the formation of a low Ohmic current-path.

Methodology

The different cells analysed are displayed in Fig. 1(a-e). Circular and ALL have been solved by means of cylindrical coordinates. Conversely, the array and Hex layouts have been simulated by using 3D unit cells that account for 1/8 and 1/12 of the total cell. Ideal Neumann conditions have been applied to the geometrical boundaries. A layer of positive fixed charges ($1.75x10^{12}$ cm^{-2}) has been added at the SiC/SiO_2 interface. The drift (buffer) region's doping and thickness have been set to 10 µm (1 µm) and $1x10^{16}$ cm^{-3} ($5x10^{18}$ cm^{-3}). The implanted profiles have been matched from a process-based simulation, both the p+/n+ regions are 1µm long and the channel length is fixed at 300 nm for all the geometries. The threshold voltage is identical for all topologies analysed in this study.

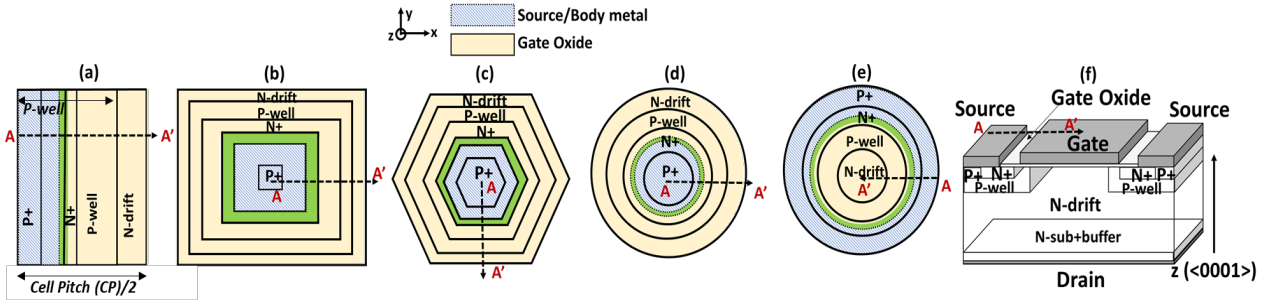

Fig.1. Top views of (a) stripe (b) array, (c) hex, (d) circular, (e) ALL, (f) cross-section of the stripe.

The SC capability of each structure is examined through single pulse short circuit (type I) mixed-mode simulations, using the circuit in Fig. 2(a). A single thermal interface has been added at the drain contact with a specific thermal resistance of 0.3 cm^2 K/W. This situation reproduces well the typical heat transfer configuration in which the top area of the device is less thermally conductive compared to the substrate. Reflective heat boundary conditions have been assumed at the geometrical boundaries of the device. For the purpose of this work, thermo-mechanical effects, convection and radiation heat exchange, gate oxide failure or cell-to-cell unbalances have not been accounted for [5].

Results and Discussion

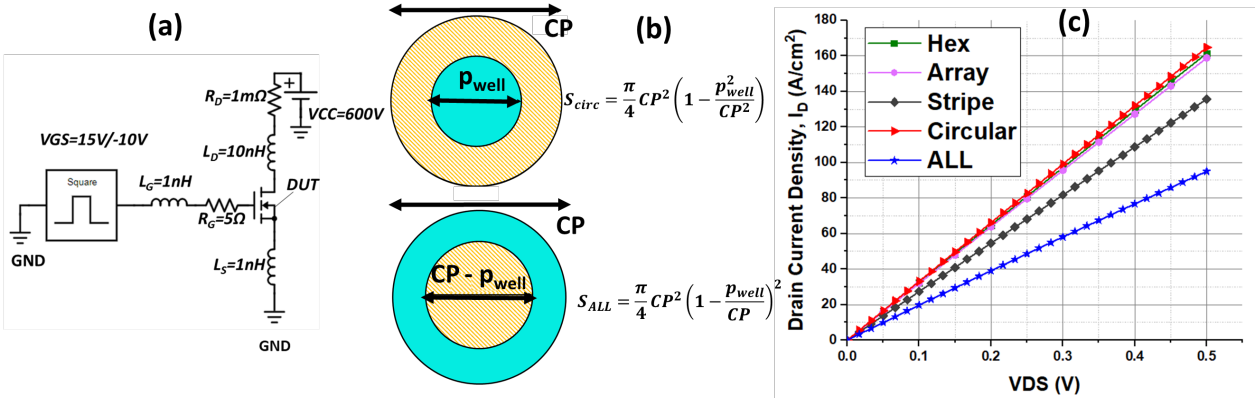

Fig.2 Schematic circuit used for the SC (type I) simulations(a), top view conduction area (orange) for circular and ALL which shows that the area S_{ALL}<S_{CIRC} (b) and output IV at T=300K, V_{GS}=15V(c).

$$\frac{\partial(c_L T)}{\partial t} = \vec{\nabla}\cdot(\kappa\nabla T) - \vec{\nabla}\cdot\left(\vec{J}(\varphi_{F,n}+\Pi)\right) + \dot{Q}_{transient} + \hbar\omega G_{opt} \quad (1)$$

$$\dot{Q}_{transient} = (E_C + \frac{3}{2}k_B T)(R_{net} - \vec{\nabla}\cdot\vec{J}/q) \quad (2)$$

$$-\vec{\nabla}\cdot\left(\vec{J}(\varphi_{F,n}+\Pi)\right) = \frac{J^2}{\sigma} - T\vec{J}\cdot\nabla S_{Seebeck} - (\varphi_{F,n}+\Pi)\vec{\nabla}\cdot\vec{J} \quad (3)$$

In Fig.2(c), the simulated $R_{ON}S$ for SiC devices reproduces well the experimental and theoretical trends observed in [1] for Si-devices, with the circular MOSFET outperforming the other layouts in terms of $R_{ON}S$. Similar ON-state performance (as well as SC performance in Fig.3(a) and breakdown voltage, not shown) can be observed for the array, hex, and circular layouts.

Note that the formation of the channel along the Si-face (x-y plane) allows for the variation of the channel mobility along the different crystal faces (which could affect the outcome of the comparison for trench-based MOSFETs) to be neglected. The structure's electrothermal response is described, using the classical thermodynamic model (Eq.1-3) [6-7].

This expression is based on the continuity equation, which relates the rate of change of the internal energy of the system (composed of the lattice and the carriers) to the energy flux due to conduction via Fourier's law, Joule and Thomson heating (second term), optical generation, and an additional term, which accounts for the energy's dynamic variation with the carrier density. The Peltier coefficient Π here is computed assuming Thomson's second relation and Mott's formula for the Seebeck coefficient. The SC drain current density (J_D) and the maximum and average lattice temperatures (T_{max}, T_{avg}) for a 5μs SC pulse (CP=8μm) are shown in Fig. 3 (a-b). It can be observed that T_{avg} follows the same trend (with the cell's topology) as J_D. This also agrees with the (expected) variation of $R_{ON}S$ with the cell layout (shown in Fig. 2 (c)).

Conversely, T_{max} varies in the exactly opposite way. The increased local heat generation in the ALL cell can be explained with the stronger (local) Joule heating effect (where $Q_{Joule}= J^2/\sigma$ as shown in Eq.3). Indeed, the ALL's smaller JFET area density (calculated in Fig. 2(b)) limits the spreading of the current and hence increases the (local) current density, effectively creating a current filament.

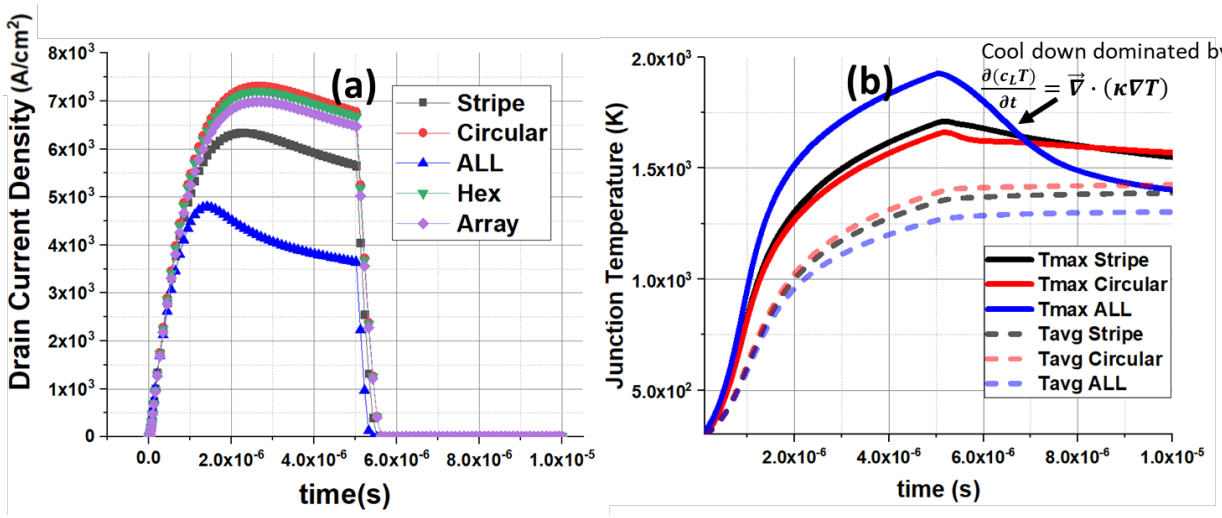

Fig. 3 SC waveforms of (a) the drain current density and (b) T_{avg} and T_{max} for a fixed CP=8 μm.

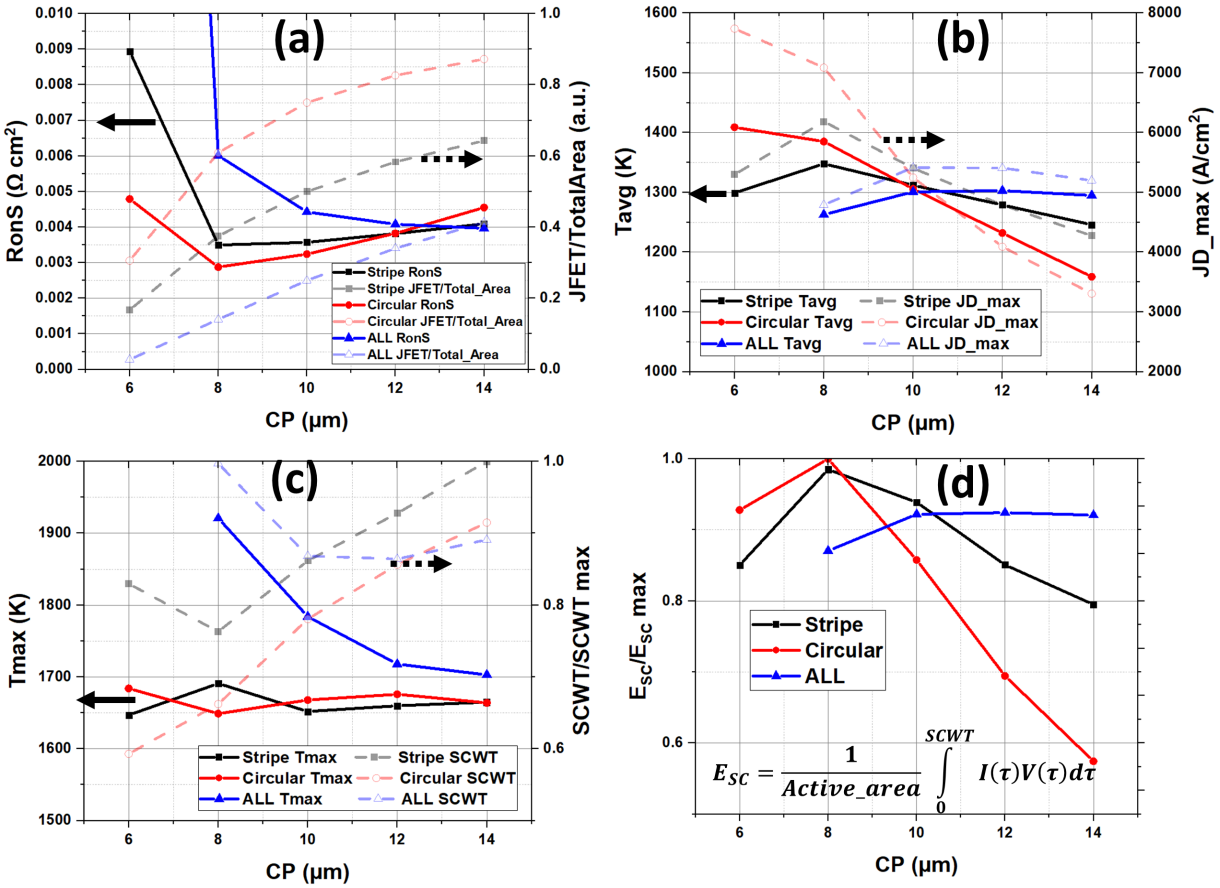

Fig.4. (a)RonS (T=300K) and JFET area/total cell area for different CP; (b)Average junction temperature(Tavg) at t=5 μs and maximum SC drain current density(JD_max); (c) Maximum junction temperature (Tmax) at t=5 μs and normalized short circuit withstand time (SCWT) extracted at the value at which JD reaches again JD_max due to current density increase related to the thermal runaway; (d) normalized short circuit critical energy density vs CP for different layouts.

The cells' behaviour for different CPs is presented in Fig. 4 (a-d). Here T_{avg} correlates well with the peak short circuit current (J_{D_max}) and the critical SC energy (E_{sc}). Indeed, the higher T_{avg} of the circular reduces the SCWT due to premature thermal runaway. More interesting is the evolution of T_{max} with CP, where a non-monotonic trend can be observed for the circular and stripe designs, but not for the ALL (Fig. 4 (c)). This differs from the variation of the JFET area density in Fig. 4 (a) and can be explained through examination of the temperature distribution in the top of the cell (Fig. 5). In the case of the ALL, the peak temperature point lies deep inside the JFET region (and farther from the channel than in the other designs) for all examined CP (Fig. 5). This is a consequence of the smaller conduction area in the JFET region. At larger CP, however, the JFET component of $R_{ON}S$ reduces monotonically, which allows for improved current spreading (in the JFET region) and hence slowly shifts the point of the peak current density (and of Joule heating) to the interface. Conversely, while a similar trend can be seen in the stripe cell, the depth (relative to the surface) of the location of T_{max} is smaller (due to the larger JFET area). In fact, for the circular, the point of T_{max} remains next to the SiC/SiO_2 interface for all examined CP. Nevertheless, unlike in the ALL, the degree of current spreading in the circular and stripe designs saturates above 10μm CP, due to the newly added lateral resistance along the length of the accumulation layer. Thus, $R_{ON}S$ eventually starts to rise with CP (due to the inefficient area consumption). More importantly, this also leads to a saturation of the local Joule heating profile and thus of T_{max} (unlike in the ALL, where it falls continuously with CP).

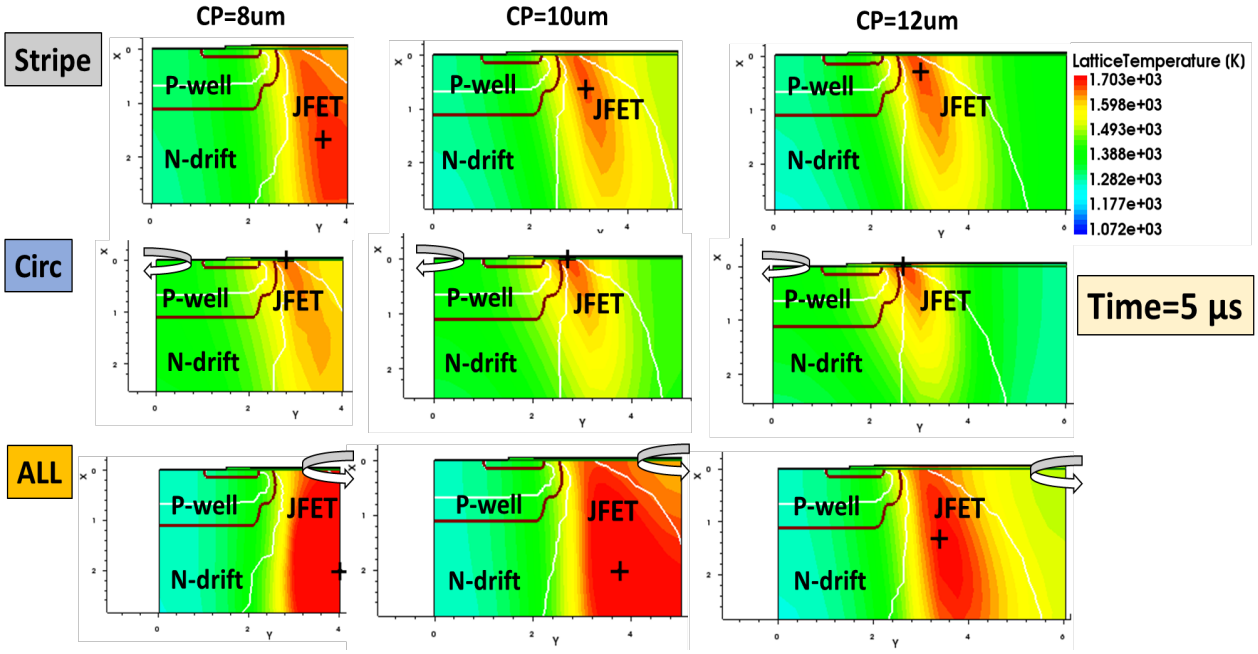

Fig. 5. Lattice temperature profile at the top of the unit cell for the stripe, circular and ALL layouts at t=5 µs. The cross mark depicts the location of the peak lattice (junction) temperature point.

Conclusion

In conclusion, this work has clearly demonstrated that there exists a strong correlation between the evolution of the maximum junction temperature (hotspot) and the cell layout, which is not only a function of the JFET area density but also of the current density profile and current spreading in the JFET/accumulation region. Moreover, the average local junction temperature, as well as the location of the hotspot, are both responsible for the device's thermal runaway failure mechanism.

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