

# Design of an Integrated Power Module for Silicon Carbide MOSFET with Self-Compensation of the Magnetic Field

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**Abstract.** Compactness, efficiency, and light weight are the key topics in the design of power conversion systems for transportation applications. This demand is achievable by using wide band gap devices such as SiC devices, characterized by the high switching speed and low on-resistance. However, this trend imposes new challenges and the effect of parasitic elements of power package during switching transient becomes significant. Hence, new packaging solutions should be investigated for addressing this concern. This paper presents a new multichip power module architecture, where its design considering capacitive and inductive stray elements is carried out. Using Ansys Q3D Extractor, electromagnetic simulations are achieved to extract the inductive and capacitive parasitic element of one leg of a three-phase inverter.

## Introduction

The Silicon (Si) material is a semiconductor used in many power electronics applications. The latest technological developments have led to minimal dimension requirements that would be a hard physical limit for this material. Thus, the standard solution proposed to overcome these limits is to replace Si with Silicon Carbide (SiC) material [1]. In fact, SiC MOSFETs have shown several advantages over the similarly rated Si IGBTs, such as a higher switching speed and thus lower switching losses. Hence, SiC devices enable the fabrication of converter systems with high performance, high efficiency, and high power density, meeting better new market requirements [2]. However, using these SiC-based switches makes the system very sensitive to parasitic circuit elements. Also, they can lead to higher electromagnetic interferences (EMI), voltage, and current ringing during switching. For example, high di/dt in a switching cell might result in a severe turn-off overvoltage due to the presence of the parasitic stray inductance that must be minimized. Therefore, to take full advantage of the good performances of SiC devices and ensure a good operation of power converters, the optimization of their packaging technology is necessary [3].

In this paper, we propose a new design of a multichip power module, with low parasitic inductance specifications and symmetrical parasitic capacitances. The presented design is based on optimizing the placement of embedded transistors in a PCB layout which allows a self-compensation of the magnetic field that reduces the parasitic inductances of the circuit [4].

## Design Principle

It is well known that a low-inductive switching loop is necessary to obtain fast switching. As well, to avoid large EMI during the switching of the transistors, a special attention to the electromagnetic compatibility (EMC) design rules are mandatory. Hence, this section presents the characteristic of

the design that considers capacitive and inductive stray elements to obtain high switching speed capabilities.

**Inductance of the overall current commutation loop ( $L_{CCL}$ ).** To reduce  $L_{CCL}$ , several techniques are considered. As shown in the cross section view of Fig. 1, the power switches are integrated between two PCBs (PCB1 and PCB2) with the flip-chip technology. This technology demonstrates considerable improvements in switching performance, since it allows decreasing  $L_{CCL}$  and improving the symmetry of common mode capacitances when compared to conventional packages [5]. Also, the flip-chip technology applied to the transistors, reduces the surface of the switching cell, and minimizes  $L_{CCL}$ .

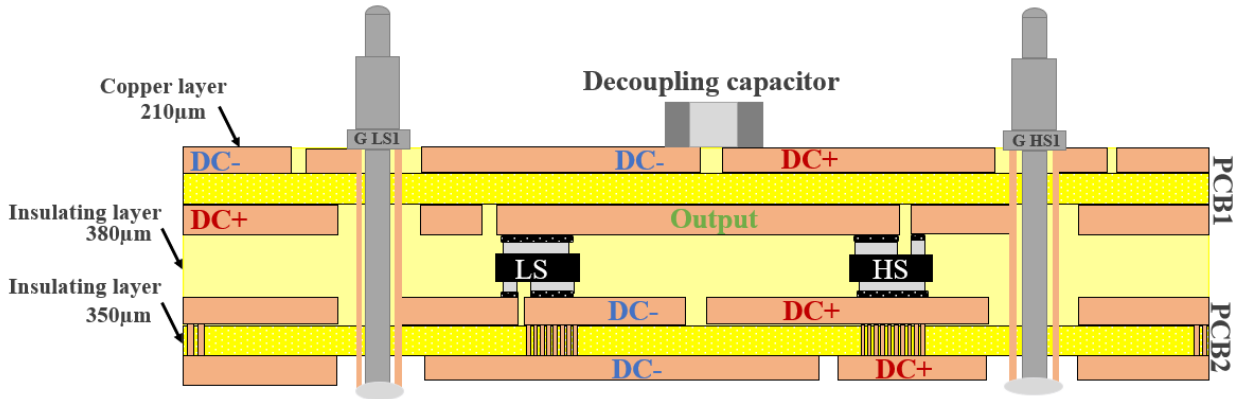


Fig. 1: Cross section of the proposed power module.

In addition to these features, special attention is paid to the position of the transistors. In our design, both high side (HS) and low side (LS) switches are composed of two SiC MOSFET dies in parallel (Fig. 2a). As shown in the bottom view of PCB1 represented in Fig. 2b, the HS1 MOSFET is placed diametrically opposed to the HS2 (same for LS1 and LS2). This arrangement allows a self-compensation of the magnetic fields created by the opposite switching loops, loop (1) and loop (2) in Fig. 2c, which ensures minimization of the global parasitic inductance of the switching cell.

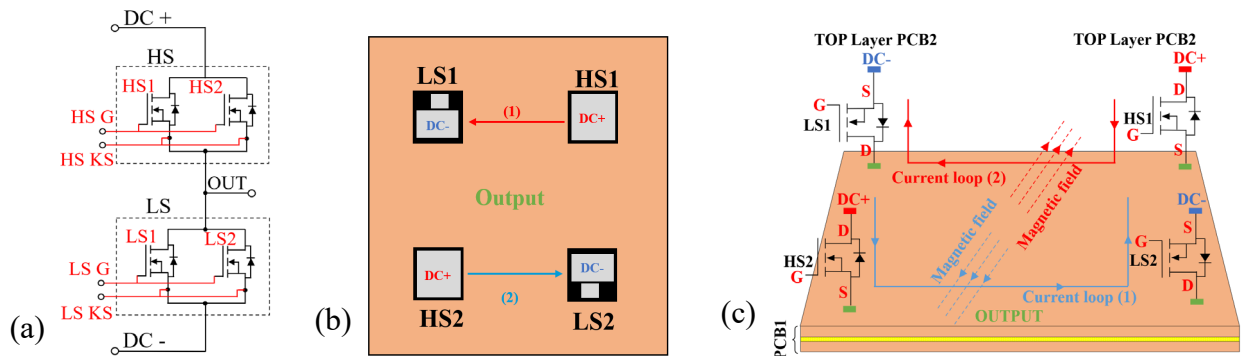


Fig. 2: Proposed technology. (a) Electrical scheme. (b) Positioning of transistors. (c) Self-compensation of the magnetic fields.

**EMC.** With short switching times, when SiC components are used, the capacitive coupling elements create a considerable impact on the conducted EMC. As shown in Fig. 3, the common mode (CM) capacitor at the output node (OUT), is due to the layout of the module, the interconnections, and the load. The high  $dv/dt$  at this node generates common mode currents through  $C_{OUT}$ . Also, the CM current is conducted by the capacitor of gate driver insulation ( $C_{iso}$ ) that must be reduced. Although,  $C_{DC+\_GND}$  and  $C_{DC-\_GND}$  constitute a recycling path to the CM current inside the module. They can be considered as a part of the CM filter. To keep the advantage of  $C_{DC+\_GND}$  and  $C_{DC-\_GND}$ , bus voltage must be stable enough, and it is necessary to have a symmetrical layout at DC+ and DC-. Also, the

symmetrization of  $C_{OUT\_DC+}$  and  $C_{OUT\_DC-}$ , which are parallel to the output capacitances of HS and LS transistors respectively, is necessary to have a simultaneous switching of these transistors.

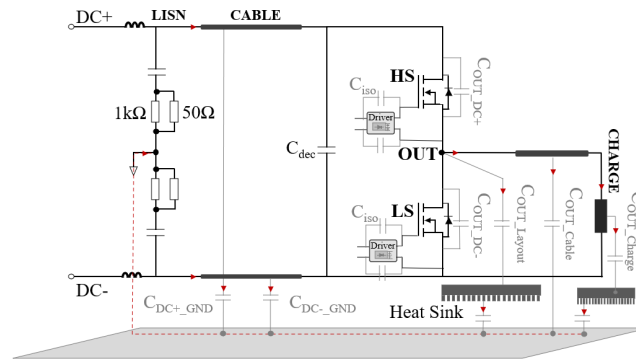


Fig. 3: Representation of the parasitic capacitors.

### Q3D Simulations Results

To verify the advantage of this innovative power packaging technology that combines (i) the flip-chip of the MOSFETs and (ii) the diametrically opposed position (designated as configuration 1), a performance study was carried out to compare this first configuration (Fig. 4a) with two others (configuration 2 and 3). Configuration 2 presents a non-crossed position of the transistors but keeps the flip-chip technology (Fig. 4b) that should confirm the interest of the self-compensation of the magnetic field in configuration 1. Also, configuration 3 presents a classical disposition of the transistors without a flip-chip (Fig. 4c), with an architecture closer to the one of conventional packages that should demonstrate the importance of the symmetrical layout in configuration 1.

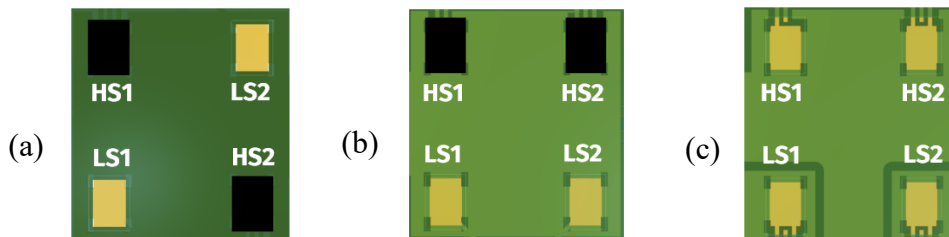


Fig. 4: Positioning of transistors. (a) Configuration 1. (b) Configuration 2. (c) Configuration 3.

**Stray inductances.**  $L_1$  and  $L_2$  shown in Fig. 5, represent the stray inductances, due to the packaging, of branch 1 and 2 respectively, and  $M_{12}$  represents the mutual inductance between these branches.

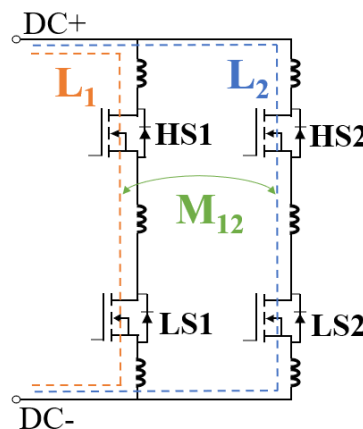


Fig. 5: Self and mutual inductance of paralleled branch.

The total parasitic inductance is represented by the Eq. 1:

$$L_{\text{total}} = \begin{bmatrix} L_1 & M_{12} \\ M_{12} & L_2 \end{bmatrix} \quad (1)$$

The equivalent parasitic inductance of the CCL can also be represented by the Eq. 2:

$$L_{\text{CCL}} = \frac{L_1 L_2 - M_{12}^2}{L_1 + L_2 - 2M_{12}} \quad (2)$$

The extractions of self and mutual inductances are realized with Ansys Q3D software. To illustrate the influence of the self-compensation of the magnetic flux, the inductance matrix of the first configuration is shown in Eq. 3 and compared with Eq. 4 that represents the inductance of the second configuration.

$$L_{\text{totalConfig1}}(\text{nH}) = \begin{bmatrix} 2.2 & -0.26 \\ -0.26 & 1.8 \end{bmatrix} \quad (3)$$

$$L_{\text{totalConfig2}}(\text{nH}) = \begin{bmatrix} 2.2 & 0.275 \\ 0.275 & 1.8 \end{bmatrix} \quad (4)$$

As can be seen, the mutual inductances between paralleled branches of the first configuration are negative. The equivalent parasitic inductances  $L_{\text{CCL}}$  are 0.86nH and 1.12nH for the first and the second configuration, respectively. This proves the hypothesis of self-compensation of magnetic field, where the mutual inductances cancel 23% of the total parasitic inductance and reduces its effect.

**Common mode capacitors.** The extractions of the common mode capacitors are also realized by Ansys Q3D extractor. The results obtained for the first configuration are now compared with the second and third configurations.

Table 1: Q3D results of common mode capacitor.

	Configuration 1	Configuration 2	Configuration 3
$C_{\text{OUT\_Layout}}$ [pF]	0.08	0.08	38
$C_{\text{DC+\_GND}}$ [pF]	39	45	38.7
$C_{\text{DC-\_GND}}$ [pF]	42	45	0.4
$C_{\text{OUT\_DC+}}$ [pF]	74.4	93.5	105
$C_{\text{OUT\_DC-}}$ [pF]	73.2	98.7	49

Table 1 shows that the output capacitance due to the layout design ( $C_{\text{OUT\_Layout}}$ ) is negligible for the first and second configurations. Also, the capacitance comparison between  $C_{\text{DC+\_GND}}$  and  $C_{\text{DC-\_GND}}$  reveal that the layout at DC+ and DC- are more symmetric for configurations 1 and 2 due to the flip chip technology. Also, the optimization of the layout is clearly demonstrated by the similar values obtained for the capacitances between DC+, DC- and the output node ( $C_{\text{OUT\_DC+}}$  and  $C_{\text{OUT\_DC-}}$ ).

## Summary

In this paper, the estimation of the stray inductance of a phase leg commutation loop is studied, also the common mode capacitors are considered. The above Q3D-extracted results confirm our hypothesis concerning the minimization of the parasitic inductance of the switching loops by the self-compensation concept. To complete our study, the analysis of the proposed module should be verified by experimental studies. A double pulse test will confirm the effectiveness of mutual inductance cancellation, and an EMC test will confirm the advantages of the layout symmetrization.

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