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Significant Differences in BTI and TDDB Characteristics of Commercial Planar SiC-MOSFETs

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Abstract. Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have been produced by several vendors for commercial applications. SiC-MOSFET reliability was assessed using bias-temperature instability (BTI) and time-dependent dielectric breakdown (TDDB) characteristics. Here, we compared two planar SiC-MOSFET samples (A and B) from different vendors. The samples exhibited significantly different positive and negative BTI, time-dependent gate-current, TDDB lifetime statistics, and temperature dependence. These differences suggest NO (nitric oxide)-annealing variations.

Introduction

Silicon carbide metal-oxide-semiconductor field-effect transistors (SiC-MOSFETs) have been successfully applied to railway vehicles. They are also being applied to electric vehicles (EVs). As EVs lack a railway vehicle-like redundancy system, EVs require SiC-MOSFETs to reduce the extrinsic defects. Their reliability needs to be understood. The commercial SiC-MOSFET reliability was compared in bias-temperature instability (BTI) [1], and time-dependent dielectric breakdown (TDDB) [2,3]. Further, gate oxide integrity (GOI) [4, 5] was compared for automotive applications.

Several vendors produce SiC-MOSFETs. Here, we compared the reliability of two SiC-MOSFET samples (A and B) in BTI and TDDB.

Experimental

Both the MOSFETs exhibited a conventional planar vertical structure with a 45–46 nm-thick gate oxide when observed under a transmission electron microscope. Positive and negative BTI values (PBTI and NBTI) were measured at 200 °C using spot I_{ds} monitoring during the stress conditions as a JED0 pattern [6]. TDDBs were measured at room temperature (RT, 20–27 ℃), –60 °C, and 200 °C, under a constant voltage stress (CVS, V_{gs} = 46 or 47 V). The gate current was monitored during the stress. We employed B2902A PC-controlled source measuring units (Keysight Technologies Inc., Santa Rosa, CA), STH-120 temperature-controlled furnaces (ESPEC CORP., Osaka, Japan), and LTF-70 cold plates (Graphtec Corporation, Yokohama, Japan).

Results and Discussion

Fig. 1 depicts the PBTI (a) and NBTI (b) threshold voltage shifts (ΔV_{th}). Sample A exhibited a lower PBTI and a higher NBTI than Sample B, as reported earlier [1]. Moreover, both the samples exhibited V_{th} hysteresis [7] around 0.4 V by sweeping the gate voltage (V_{gs}: -10→25→-10 V) at 200℃. NO (nitric oxide)-annealing studies suggested higher nitrogen concentration in Sample A [8].

Fig. 2(a) depicts the TDDB time-to-breakdown (t_{BD}) at different temperatures. Sample A exhibited larger t_{BD} variation, while Sample B exhibited smaller variations. As three samples were measured

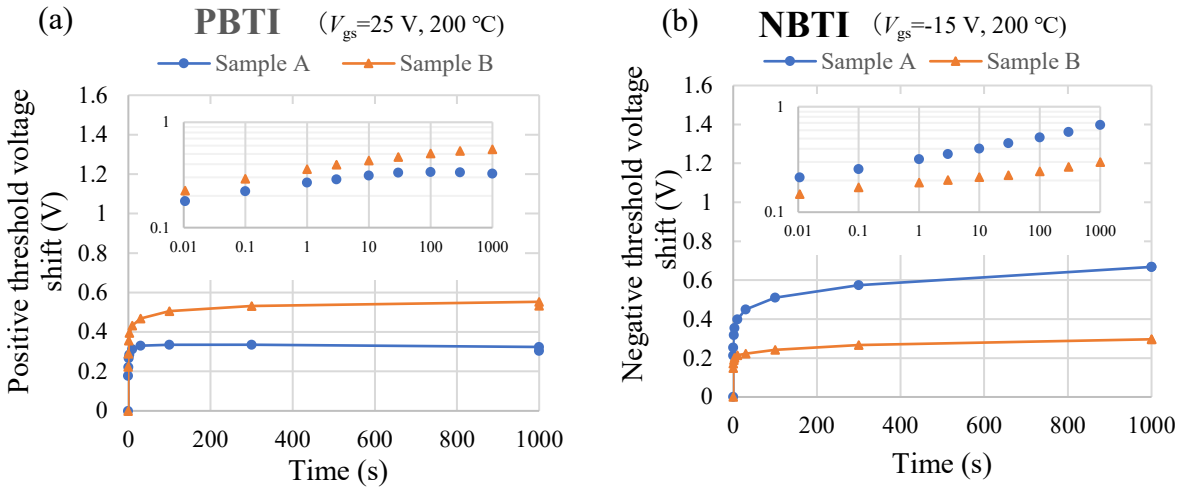

Fig. 1. Threshold voltage shifts by PBTI (a) and NBTI (b). Insets depict the logarithmic plots. The data suggest higher nitrogen concentration in Sample A than in Sample B.

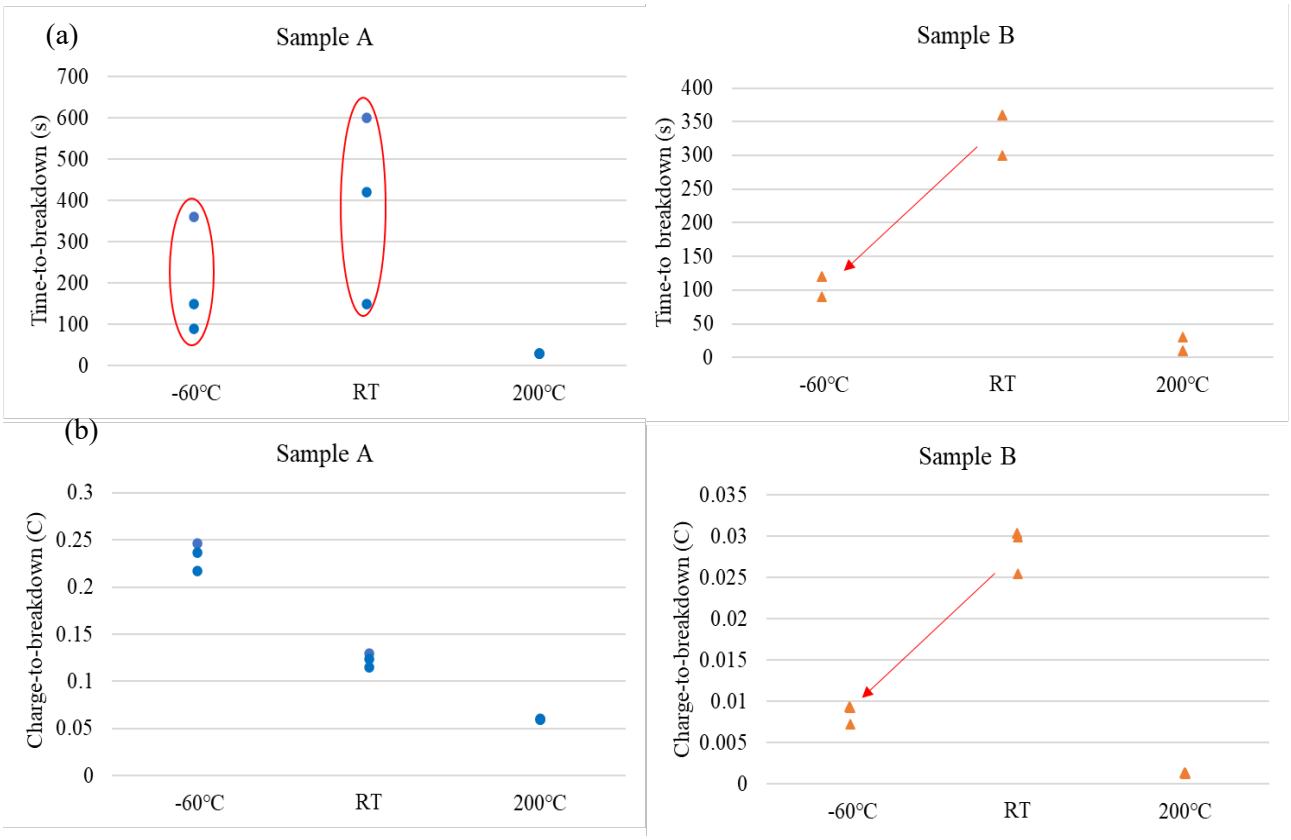

Fig. 2. Temperature dependence of t_{BD} (a) and Q_{BD} (b) at V_{gs} = 46 V. Sample A exhibited larger t_{BD} variations. Sample B exhibited anomalous temperature dependence in t_{BD} and Q_{BD}. The t_{BD} and Q_{BD} values were lower at -60 °C than at RT.

for each condition here, we present Weibull plots for t_{BD} at RT in Fig. 3(a), which were obtained from another experimental set. Sample A exhibited smaller Weibull slope than Sample B.

Fig. 4 depicts the time-dependent gate currents, $I_g(t)$, that were measured during the CVS at 47 V, RT. Sample A exhibited initial higher $I_g(t)$ that subsequently decreased, while Sample B exhibited a continuous increase. Similar V_{gs}-dependent observations were reported at 150 °C [2, 3] and 175 °C [9]. Okada et al. [10] proposed charging-induced dynamic stress in SiO_2/Si system. This elucidated TDDB anomaly upon using $I_g(t)$ behavioral pattern.

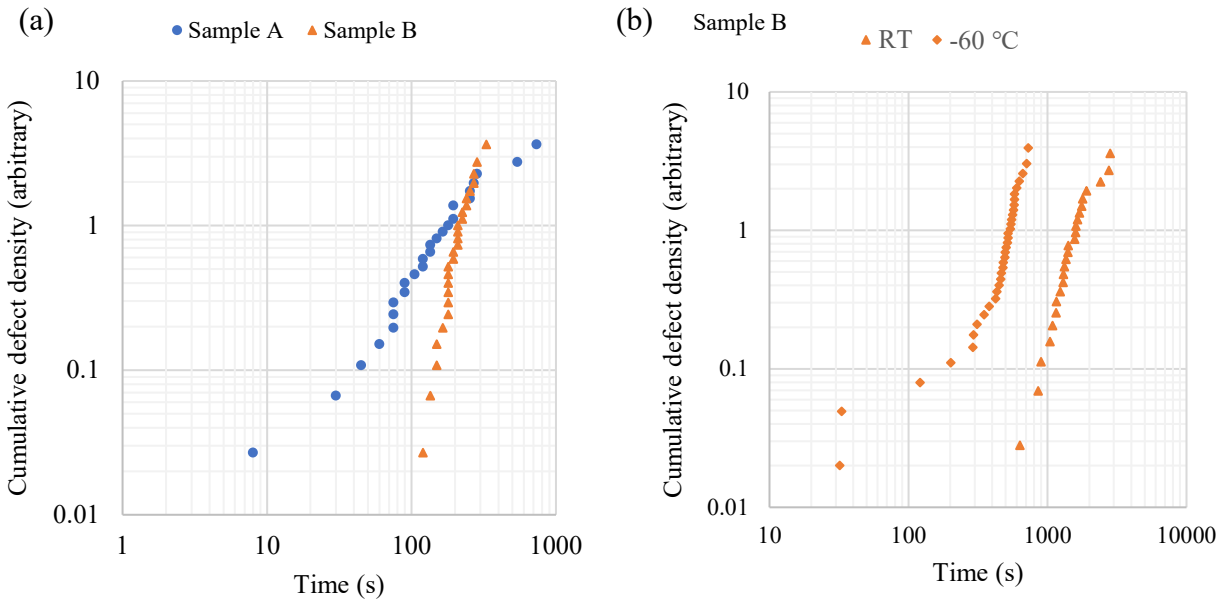

Fig. 3. Weibull plots depicting SiC-MOSFET TDDB data at V_{gs} = 47 V, RT, for samples A and B (a) and at V_{gs} = 46 V, RT and -60 °C for Sample B (b). The vertical axes are defined as -ln(1-F_i) (F_i=(i-0.3)/(n+0.4): median rank), wherein F and n denote the cumulative failure and total sample number, respectively. The cumulative defect density is defined as D(t)=-ln(1-F)/A (A: gate area). Thermostream was used in the -60 °C experiment.

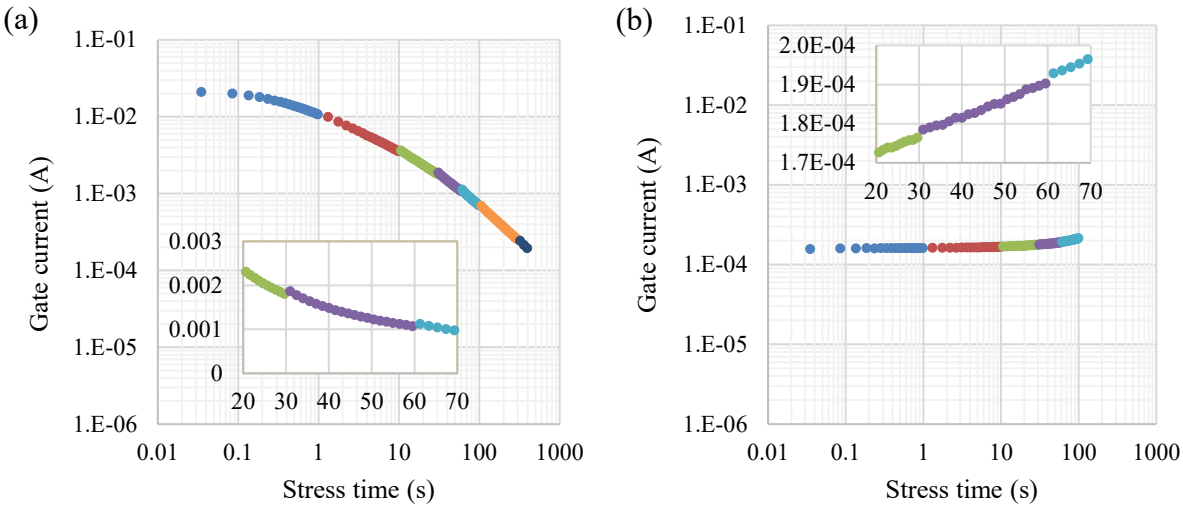

Fig. 4. Time dependence of gate current during gate stress (V_{gs}=47 V, RT). (a) Sample A and (b) Sample B. The change in color indicates the stress interruption for I–V measurements. Insets depict linear I_g increase during the interruptions, suggesting electron detrapping. The data also suggest higher nitrogen concentration in Sample A than in Sample B.

When I_g is in the decreasing phase, a sample with a larger Q_{BD} shows a much larger t_{BD} by CVS than expected. On the contrary, in the increasing phase, a sample with larger Q_{BD} suffers stronger stress than expected; thus, reducing its $t_{BD.}$ Consequently, while the former resulted in larger t_{BD} variations (as in Sample A), the latter resulted in smaller t_{BD} variations (as in Sample B).

Moreover, we elucidated the TDDB's NO-annealing dependence using test element group (TEG) chips [11]. The samples A and B corresponded to heavy and light NO-annealing situations, respectively. This argument was consistent with the BTI characteristics (Fig. 1). We hypothesized that holes and electrons were trapped near the SiO_2/SiC interface [11]. The trapped location remains to be investigated [2, 3, 5, 9].

Fig. 2 (b) depicts the calculated Q_{BD}s. Larger Q_{BD} values and normal Q_{BD} temperature dependence were observed in Sample A, as reported for SiO_2/Si system [12]. Although higher temperatures resulted in lower hot-carrier generation, the defect formed upon thermal activation. Therefore, the TDDB temperature coefficient remained positive [13]. However, an anomalous temperature dependence for t_{BD} and Q_{BD} was observed in Sample B, which resulted in the largest RT values. Weibull plots from a different experimental set are presented (Fig. 3(b)) to support this anomaly. The extrinsic mode was observed to a greater extent at -60 ℃. This phenomenon should be investigated further.

Understanding the basis of this anomaly requires further investigation. The presence of residual carbon at the SiO_2/SiC interface in an oxidized SiC sample was demonstrated in a carbon-ejection study [14]. The residual carbon might alter thermal activation during the defect formation process. The NO-annealing dependence is being investigated using the TEG chips [11].

Summary

The two SiC MOSFETs exhibited different PBTI, NBTI, TDDB statistics, and temperature dependence in commercial planar structures. These differences are probably due to NO-annealing variations.

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