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SiC MOSFET C-V Characteristics with Positive Biased Drain

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Abstract. Even if SiC MOSFETs technology has undergone huge progress in last years, there are some issues still open, such as high traps density at the SiO_2/SiC interface. This work focuses on the measurement of the Gate capacitance when a DC bias is applied between Drain and Source to characterize the SiO_2/SiC interface. The experimental curves, performed on a commercial SiC power MOSFET, exhibit a peak when the Gate voltage approaches the threshold voltage. Such peak is analyzed through TCAD simulations and its origin is addressed. Numerical analysis shows that this peak is associated to the displacement current, with a strong dependence on the traps concentration at the SiO_2/SiC interface.

Introduction

The high performance of the Silicon Carbide (SiC) [1] led to a large improvement of this technology in the last decades. SiC power semiconductor devices such as diodes and MOSFETs are now available on the market with stable performances. Although all the progress made, there are still open issues affecting this technology, such as the high traps density at SiO_2/SiC interface [2] and the hysteresis phenomena arising in the current-voltage (I-V) curves. However, the high traps density is detrimental for device performance [3]-[4], affecting channel mobility [5], threshold voltage stability [6] and leakage current amplitude. In this work, through experimental characterizations and numerical simulations, for the first time the behavior of the Gate capacitance is monitored when a DC bias is applied between Drain and Source terminals. More in detail, experimental setup and results are presented in Section 1. In order to understand these results a numerical study has been performed and presented in Section 2. Conclusions are then drawn.

Section 1

Experimental Setup and Results. The experimental setup is presented in Fig. 1a. The aim of this work is the characterization of the Gate capacitance when a DC bias is applied between Drain and Source terminals. Therefore, a ramp ranging from -20 V to 12 V is applied on the Gate with a superimposed AC small signal, Fig 1b. In addition to that, a DC bias is applied between Drain and Source. The capacitance-voltage (C-V) curves refer to the commercial planar SiC MOSFET (MSC080SMA120B4), and they have been performed by means of an Agilent 4294A Impedance Analyzer. The small signal amplitude is set to 100 mV while the frequency chosen is 100 kHz. A DC voltage has been applied between Drain and Source during the capacitance measurements, V_{DC} has been set to 1 V, in the first case, and to 2 V in the other case, Fig 1c.

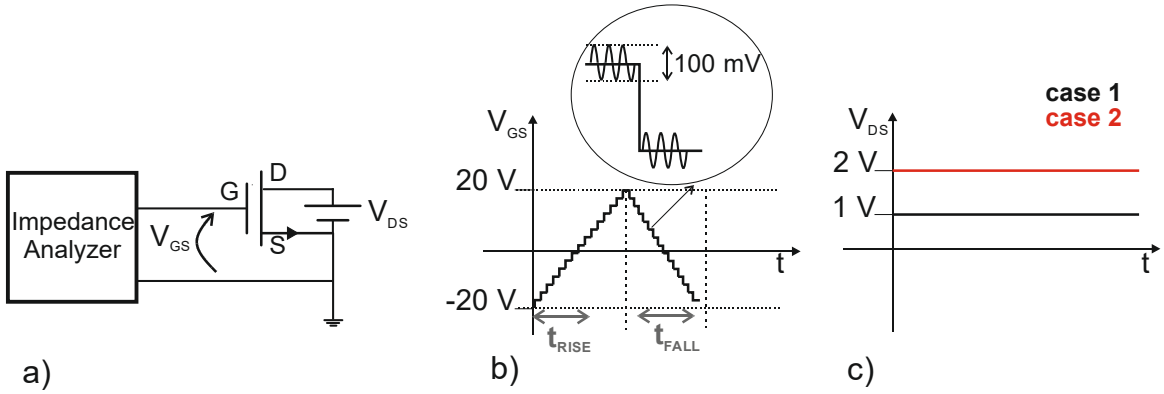


Fig. 1. a) Experimental setup used, b) V_{GS}, and c) V_{DS}.

The resulting experimental capacitance versus voltage curves are shown in Fig.2. In the accumulation and depletion region (blue and green highlighted in of Fig.2), the obtained capacitance behavior is close to capacitance behavior when no bias is applied between Drain and Source ($V_{DS} = 0$ V). Initially the capacitance is mostly due to oxide capacitance, and then it decreases due to the increase of the depletion region with applied Gate voltage. The substantial difference occurs in the inversion region: a sharp peak occurs in Fig.2 when a bias is applied to Drain, while, in the case the Drain is not biased,

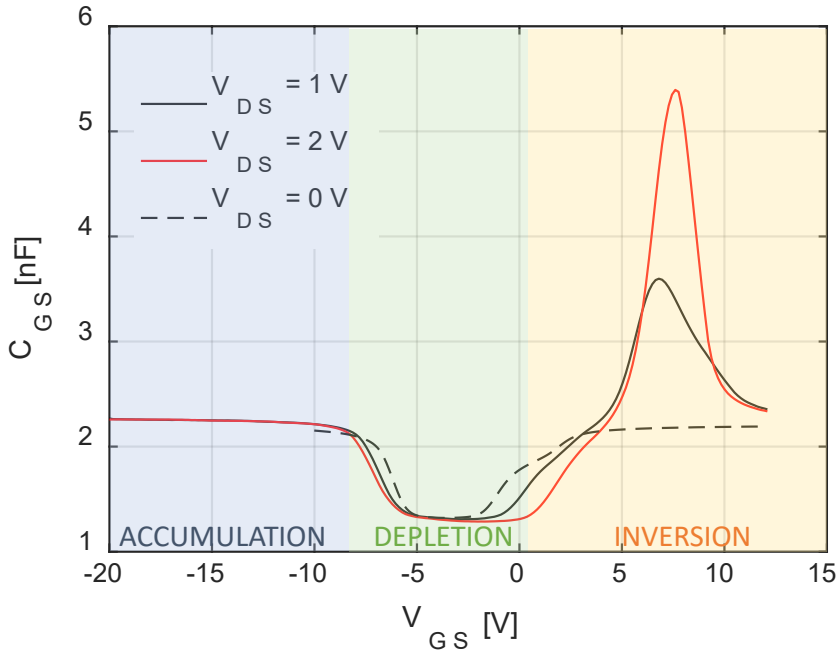


Fig. 2. Experimental C-V curves of a commercial SiC MOSFET, when a DC bias of 1 V (black) and 2 V (red) is applied between Drain and Source.

$V_{DS} = 0$ V, capacitance curve doesn't exhibit such peak. The prominent peak occurs in both cases, $V_{DS} = 1$ V and $V_{DS} = 2$ V, at a voltage which is close to the threshold voltage. This seems to suggest that the occurrence of such peak is related to traps concentration at SiO_2/SiC interface, which mainly affects the threshold voltage in the I-V curve, as will be discussed in the next Section.

Section 2

Numerical framework and results. A numerical model has been built in Sentaurus TCAD [7] to gain a better understanding on the experimental results. The structure used in this work is a reference model to approximate the commercial device [8]-[11]. The C-V curve has been carried out in

simulation taking into account the effects of long-time-constants traps. To highlight the effect of such traps, a sawtooth signal is applied to the Gate of the TCAD model and for each time step an AC simulation is carried out. In Fig.3 the simulated C-V curve is reported when a DC bias of 1 V is applied between Drain and Source, together with the relevant simulation parameters. In the same figure, the displacement current in the structure is shown, more precisely in the region near the channel, for three voltage values highlighted in the numerical C-V curve. The displacement current distribution gives a strong insight, since it can be argued that the peak occurs where such current is higher and there is a current flow through the oxide. Therefore, the arising peak has its origin in the channel region. This statement is enforced by considering the derivative of the numerical Drain current with respect to the voltage V_{GS} and the numerical capacitance-voltage curve.

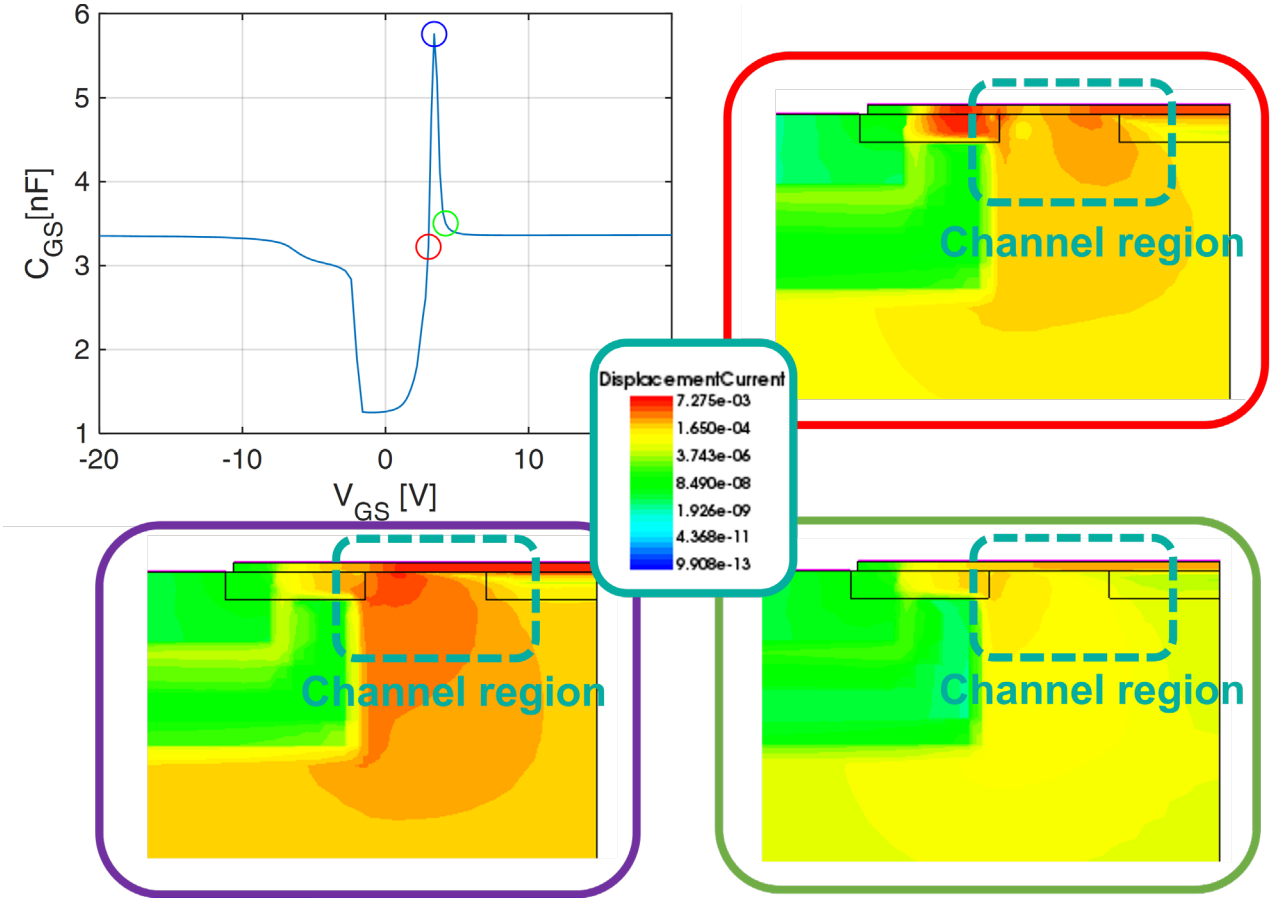
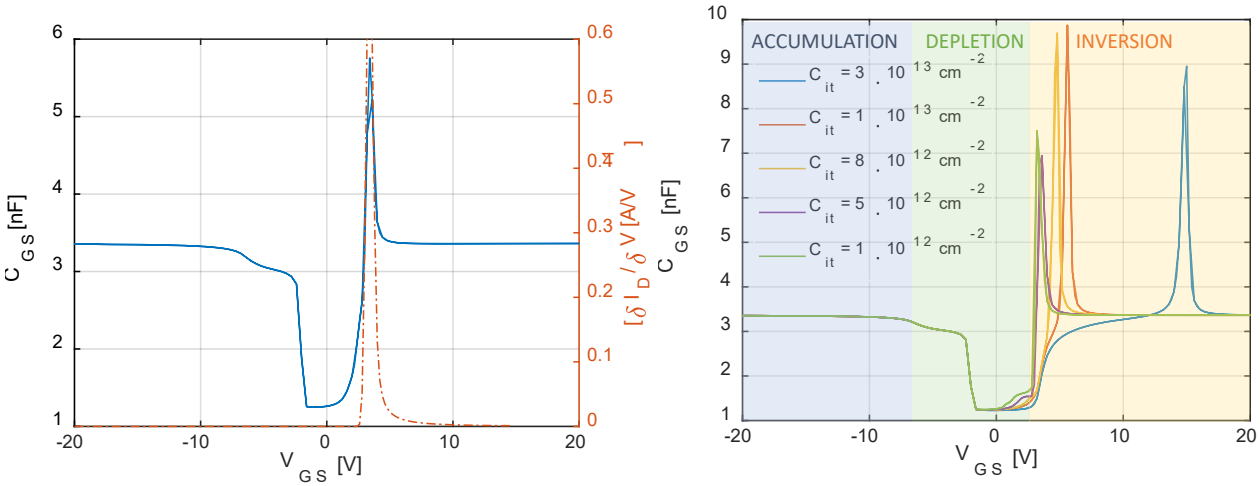


Fig. 3. Numerical C-V curve, with V_{DS} = 1 V. Insets represent displacement current in the channel region at highlighted voltage values. A fixed charge concentration, $C_{it} = 2 \cdot 10^{12}$ cm^{-2}, has been set at the SiO_2/SiC interface. The temperature set is T = 300 K, and the frequency is f = 100 kHz.



a) b)

Fig. 4. a) Numerical C-V curve, with V_{DS} = 1 V, left y-axis, and derivative of the Drain current $\delta I_D/\delta V$, right y-axis. The two curves have a peak occurring at the same voltage. b) Numerical C-V curves, with V_{DC} = 1 V, and different traps concentration at the SiO_2/SiC interface. The peak width is wider as the traps concentration increases.

In Fig. 4a, it is clear as the peak of the current derivative is occurring at a voltage V_P which is exactly the voltage at which the capacitance peak is occurring. Thus, characterizing this peak can give reliable information on traps properties. To this end, numerical results show that the higher is the trap concentration, the wider is the region where the capacitance peak occurs. In Fig.4b, the numerical C-V curves obtained with different traps concentration at the SiO_2/SiC interface are shown. Increasing traps concentration in the channel region affects the threshold voltage. This also involves a shift of the capacitance peak. From Fig.4b, it can be seen that for the higher concentration considered there is a twofold effect: not only the capacitance peak significantly shifts toward higher voltage but also the region affected is considerably wider.

Conclusions

The behavior of SiC MOSFET Gate capacitance with a positive bias applied between Drain and Source has been considered in this work. Experimental C-V curves obtained with commercial SiC MOSFETs exhibited a prominent peak in the region of the threshold voltage. The occurrence of such peak has been studied by means of TCAD framework. The numerical analysis showed that the peak occurring in the Gate capacitance is related to traps concentration at the SiO_2/SiC interface. More in detail, the capacitance peak occurs at a voltage where the displacement current is higher. This has been confirmed by comparing the C-V curve with the derivative of the Drain current. Both curves presented a peak occurring at the same voltage. Moreover, by considering different traps concentration at the SiO_2/SiC interface, the numerical analysis allowed to assess that the peak width is wider as the traps concentration increases. This means that this measurement technique supported by numerical analysis can be used as a quick tool for the device characterization and traps concentration extraction.

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