A Scalable SPICE-Based Compact Model for 1.7 kV SiC MOSFETs

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Keywords: compact modeling, silicon carbide (SiC) MOSFET, SPICE, power module.

Abstract. This paper presents a compact model implemented in SPICE environment for silicon carbide (SiC) MOSFET. The model is easily adjustable to devices belonging to different voltage and current ratings. A previous release of the model was tuned to match the performance of 1.2 kV and 3.3 kV SiC MOSFETs, while, in this contribution, an improved version of the compact model is calibrated for 1.7 kV devices. The agreement between the experimental and simulated data, achieved for both static and dynamic conditions, associated to the model simulation speed, emphasize its suitability as a tool for the simulation of converter containing wide arrangements of devices.

Introduction

SiC MOSFETs have become a commercial reality and both discrete devices and power modules are being progressively adopted in several market applications [1]. Given their increasing usage, there is a higher demand for fast and reliable electrothermal compact models of SiC MOSFETs that can help circuit designers in predicting the performance of the final converter. Switching converters are complex electrical machines and a detailed simulation of their efficiency rests upon a precise description of the losses (static and dynamic) of the underlying transistors. Nonetheless, depending on the complexity of the MOSFET model, the simulation of complex converter topologies in SPICE-like tools can be a computationally heavy task and a compromise between simulation speed and accuracy usually exists [2], [3]. Furthermore, commercial SiC MOSFETs are available in different classes of breakdown voltage (namely ranging from 650 V to 3.3 kV) and on-state resistance (namely ranging from 15 mΩ to 1 Ω), which increases the need for a common and adjustable modeling platform.

In previous literature contributions, we presented a SPICE-based model for SiC MOSFETs [4] and validated its applicability to 1.2 kV [4] and 3.3 kV [5] commercial devices. To further demonstrate its ease of scalability to family of devices of different voltage ratings, here we calibrate an improved version of the model to fit the electrical behavior of 1.7 kV SiC MOSFETs.

Methodology

Experimental Characterization. The devices under tests (DUTs) are 1.7 kV/60 A-rated SiC MOSFETs. Since the device are provided as bare dies, they were mounted onto a suitable test substrate to enable their electrical characterization (Fig. 1). The isothermal static current-voltage characteristics (I_D - V_{GS} and I_D - V_{DS}) of 17 DUTs were measured by an in-house developed pulsed curve tracer both at 25 °C and at 125 °C. Some parameters determining the on-state current and their spread were evaluated, and the resulting values are reported in Table 1. The MOSFETs exhibit some spread in their current-conduction behavior. Nevertheless, the spread of the transfer characteristics is confined within 15% (Fig. 2). Therefore, the DUT selected as reference for calibrating the model is the one exhibiting the median transfer characteristic. However, the impact of the technological fluctuations on the uneven current sharing can be easily included as reported in [6].

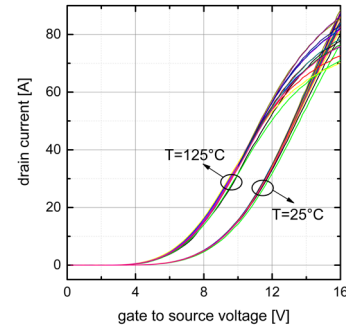Fig. 1. Example of 1.7 kV SiC MOSFET under test mounted on the test substrate.

Fig. 2. Isothermal transfer characteristics of the 17 SiC MOSFETs under test.

Table 1. Main parameters determining the current conduction and their spread measured at 25 °C.

Parameter	Threshold voltage: V_{TH} [V]	Transconductance: K_P [A/V^2]	Channel length modulation parameter: λ [V^{-1}]
Mean value ± spread	5.77 ± 0.17	0.84 ± 0.06	0.03 ± 0.004

Description of SiC MOSFET Model. The compact electrothermal model described in this work is a variant of the one presented in [4]. A schematic representation of its equivalent circuit is reported in Fig. 3, which highlights the main components used to model the static current flow. These are implemented by conventional SPICE primitives, thus aiding convergence and widening the model compatibility. The modulation of charge in the channel region is modeled by a SPICE LEVEL 3 MOSFET (referred to as M_{CH}). Following the approach suggested in [7], a standard JFET (J_{RJ}) in series with M_{CH} was used to describe the modulation of the current path due to the expansion of the space charge region in the JFET area. Such a phenomenon was previously represented in [4] through a voltage dependent resistor. The model is fully electrothermal and includes the temperature dependence of the most relevant physical parameters. Three capacitances determine the dynamic characteristics of the model. These are (i) the gate-to-source capacitance (C_{GS}) which is constant and equal to the capacitance of the LEVEL 3 MOSFET M_{CH}, (ii) the voltage dependent junction capacitance of the body diode (C_J), and (iii) the non-linear gate-to-drain capacitance (C_{GD}). The latter is modeled by an arctangent function through the relation reported in Eq. 1. This modeling choice ensures excellent simulation speed while keeping convergence issues at minimum, and, although it is reported not to be as accurate as other techniques [3], it will be shown that the simulations produce adequate prediction of the switching power losses.

$$C_{GD}(V_{GD}) = (C_{GD0} - C_{GDmin})\left[1 + \frac{2}{\pi}\arctan\left(\frac{V_{GD}}{V_{GD}^*}\right)\right] + C_{GDmin} \qquad (1)$$

The model parameters controlling the static electrical performances are calibrated through an automatic routine implemented through MATLAB and SIMetrix and outlined by the flowchart in Fig. 4. A subset of physical parameters, such as the threshold voltage (V_{TH} [V]), the current factor (K [A/V^2]), and the parameter accounting for the channel-modulation effect (λ [1/V]), are directly extracted from the experiments ant their values are used as a starting guess of an iterative optimization procedure. The procedure exploits a minimization function provided in the MATLAB optimization toolbox which progressively reduces the gap between the experimental and the simulated data.
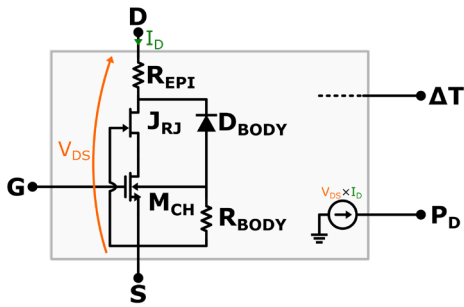
Fig. 3. Schematic representation of compact electrothermal model for SiC MOSFET. The capacitances are omitted for the sake of clarity.
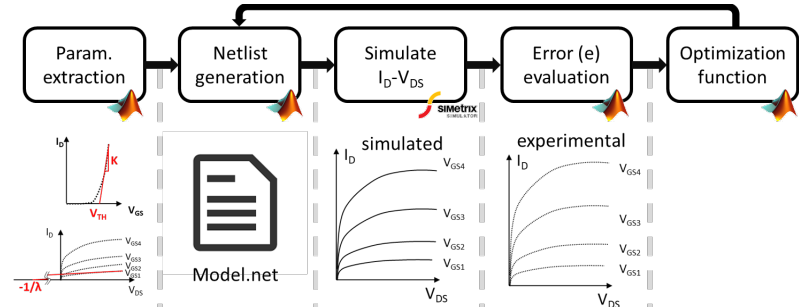

Fig. 4. Flowchart of the automatic routine for the optimization the parameters and the calibration of the static curves.

Results

From the comparison reported in Fig. 5 (a) and (b), it can be seen that excellent agreement was achieved between the experimental data and the fitted model at 25 °C. As shown by the data at 125 °C of Fig. 5 (a) and (c), the static behavior at high temperature is also correctly reproduced. To characterize the dynamic performance of the DUT, a double pulse test (DPT) on an inductive load of 1 mH was conducted by placing in series two MOSFETs in a half-bridge configuration. The high-side switch acts as a freewheeling diode since the channel conduction was inhibited by connecting the gate and source terminals together. A schematic of the DPT setup is provided in Fig. 6. The test was performed at 800 V - 28 A, with $R_G = 11 \ \Omega$ for both 25 °C and 125 °C, and careful evaluation of circuit parasitic components was carried out as it is known that they strongly affect the shape of the waveforms during switching transients [8]. As witnessed by the waveforms of Figs. 7 and 8, the model is able to precisely capture the very fast turn-on ($dV_{DS}/dt \approx 5.3$ kV/μs, $dI_D/dt \approx 275$ A/μs) and turn-off ($dV_{DS}/dt \approx 8.6$ kV/μs, $dI_D/dt \approx 225$ A/μs) switching transients, including the oscillations caused by the stray components. The accuracy of the of model is also substantiated by the comparison of Fig. 9, where the experimental and simulated waveforms of the power dissipated by the DUT are superimposed. It is worth noticing that the model not only provides a correct estimation of the switching energy, i.e., of the integral of the power dissipated during the commutations, but also of the instantaneous value of the power itself. This is of paramount relevance when it is important to take into account the time evolution of the thermal phenomena since a well-modeled power dissipation translates into an accurate time-dependent heat source [8].
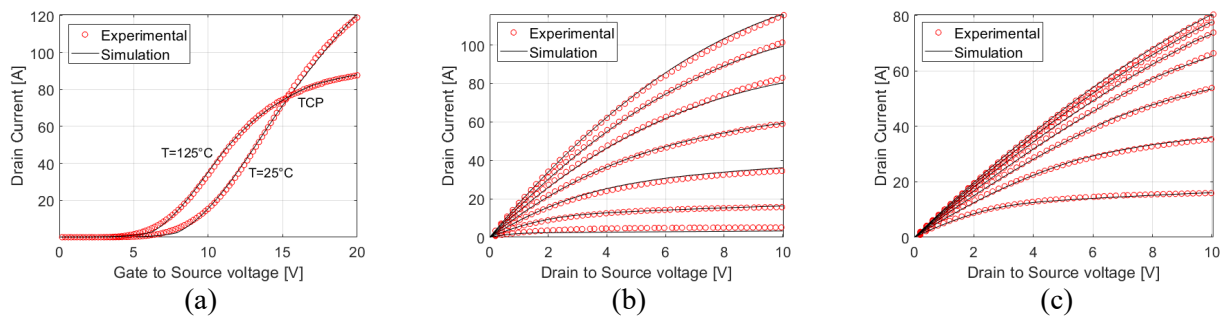

(a)

(b)

(c)

Fig. 5. Comparison between the experimental and simulated isothermal static curves for the (a) transfer characteristics, (b) output characteristics at 25 °C and (c) 125 °C.

Summary

In this paper, a SPICE-based compact model for SiC MOSFET has been presented and calibrated to the experimental data of 1.7 kV devices. The model brings several improvements to a previously published contribution and the results have shown that it can satisfactorily represent the subtleties of the static and dynamic electrical waveforms of 1.7 kV SiC MOSFETs. This type of devices constitutes an additional class of MOSFETs on which the model has been benchmarked, thus proving the ease of scalability of the model itself.
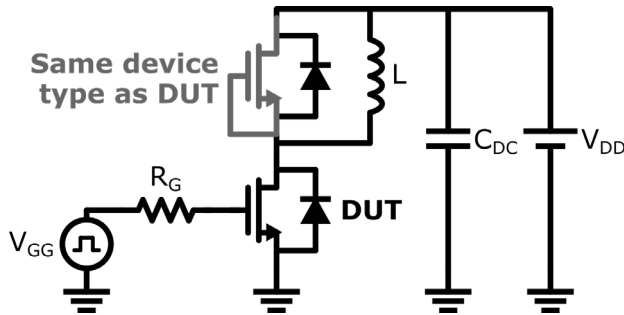
Fig. 6. Schematic of the double pulse test setup adopted for the characterization of the switching transients.

Fig. 7. Comparison between the experimental and simulated current and voltage waveforms obtained during a turn-on event on inductive load at 800 V and 28 A.
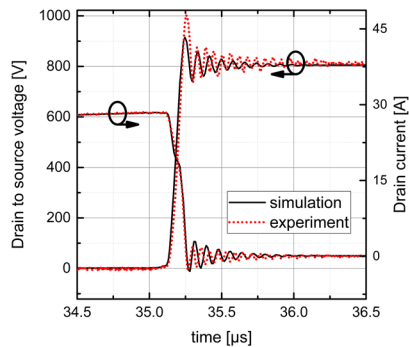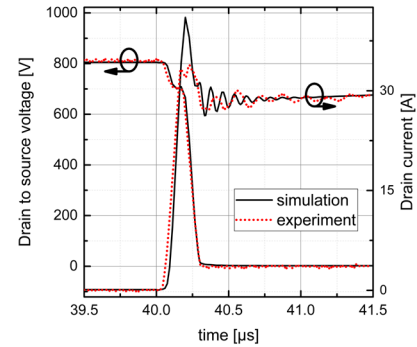

Fig. 8. Comparison between the experimental and simulated current and voltage waveforms obtained during a turn-off event on inductive load at 800 V and 28 A.
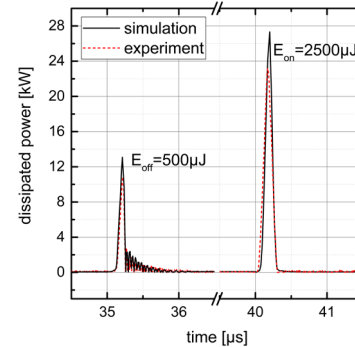

Fig. 9. Comparison between the experimental and simulated switching power dissipation obtained during a double pulse test at 800 V and 28 A.

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