SiC MOSFET C-V Curves Analysis with Floating Drain Configuration

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Abstract. SiC MOSFETs have already replaced silicon-based device in power applications, even if some technological issues are still not solved. Among others, the complex traps distribution at SiC/SiO$_2$ interface is of foremost importance. Interface traps affect the overall device behavior, modifying channel mobility and introducing hysteresis. In this work, the capacitance behavior, when the Drain terminal is floating, is studied through numerical analysis. The effects of traps distribution and its properties on such curves has been studied along with temperature effects. Experimental curves are carried out at various temperatures and compared to the same trends of numerical results.

Introduction

Silicon carbide (SiC) MOSFETs have replaced silicon devices due to the higher performance of SiC with respect to silicon material [1]. SiC has a higher bandgap and it claims a high thermal conductivity. These properties established the SiC as the most promising material for power MOSFETs. On the other hand, there are some issues not yet solved in technology, as the interface traps density at SiC/SiO$_2$ interface which affects the overall device behavior. It worth to be noted that traps density at such interface is order of magnitude higher than traps density existing at Si/ SiO$_2$ interface [2]. Traps density influences the channel mobility [3] and threshold voltage stability also introducing threshold voltage hysteresis [4-5]. For all these reasons, having a deep insight in traps density at such interface and counting on a reliable TCAD model is of paramount importance. At this purpose, experimental characterization of SiC MOSFETs together with the numerical results must be performed [6]. Experimental characterization can be obtained considering capacitance versus voltage (C-V) curves. These latter allow to gain knowledge in MOSFET behavior through all its operating regions, as the accumulation, the depletion and the inversion. Nevertheless, capacitance is affected by traps existence and obviously by geometrical and process parameters. Since traps effect varies with temperature and, more in detail, it reduces as temperature increases, experimental characterization should be carried out at different temperatures.

In this work, experimental C-V curves are carried out with a floating Drain configuration, at different temperatures. The Gate capacitance considered is measured leaving the Drain terminal floating. Using these data, we perform a qualitative analysis to gain knowledge on traps distribution existing at SiC/SiO$_2$ interface and improve device reliability. In the first part, TCAD framework and simulation are included. The numerical C-V curves are presented with different traps distribution properties. In the second part, experimental curves are presented including C-V curves. More in detail, these curves are aligned to the numerical one. Numerical analysis is employed to gain better understand in experimental curves.

Numerical Analysis

Numerical analysis has been carried out using Sentaurus environment [7]. The TCAD model of the SiC MOSFET structure considered in this work is presented in Fig.1 and TCAD models used are reported in [6, 8-11]. The effects of the SiC/SiO$_2$ interface traps on the capacitance behavior are studied by implementing the experimental setup in numerical simulations. The equivalent TCAD C-

V setup is shown in Fig.2. In this work, we analyze the SiC MOSFET capacitance behavior when its Drain terminal is floating. In this schematic, the driving voltage applied to the Gate terminal of the device under test is V_{GEN}, Fig.3, while Source terminal is grounded. Interface traps dynamics takes into account the time variation in the capacitance behavior. Traps dynamics modifies the carriers distribution as the driving voltage varies. The traps dynamics is considered by changing the t_{RISE} and t_{FALL} values of Fig.3. A small signal AC analysis is performed in Sentaurus for each time step. This framework allows to investigate the driving voltage dv/dt effect on the C-V curves. The interface traps properties considered in simulation are explicated in Fig.4. Traps distribution implemented is a square band distribution with a width, E_{TW}, and a distance from valence and conduction band equal to E_{TV} and E_{TC}, respectively. The considered model let the effects of the interface traps concentration, C_{it}, the capture cross sections, e_{Xsec} and h_{Xsec}, to be considered in the simulation.
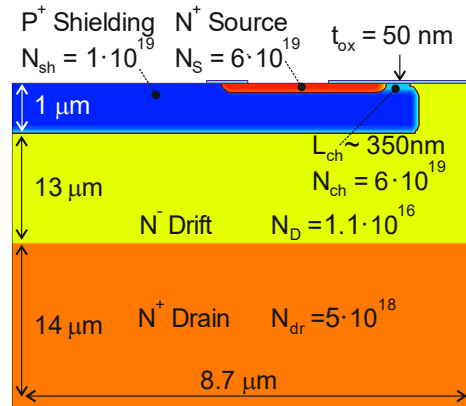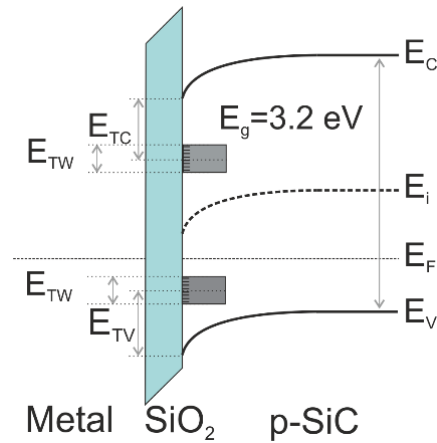

Figure 1. SiC MOSFET TCAD model adopted in this work (the structure is not to scale).
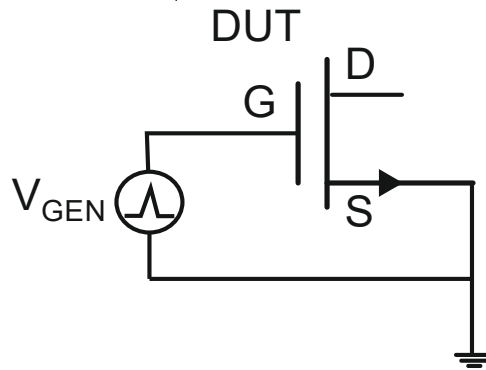
Figure 2. Schematic of the mixed-mode circuit used for the simulation of the C-V experimental setup. On the Gate terminal the driving signal is applied, Source terminal is grounded and Drain terminal is floating.
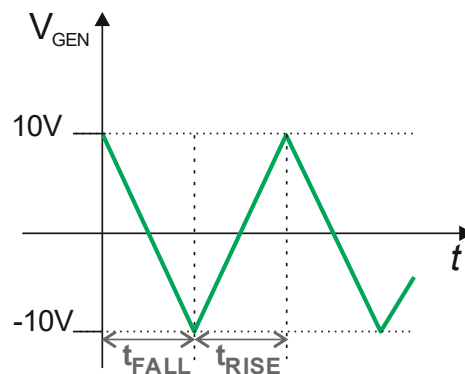

**Figure 3.** Driving voltage, VGEN, applied to the MOSFET gate.

**Figure 4.** Band diagram of the TCAD structure with trap distribution.

The numerical C-V curves are presented for acceptor type traps with varying distance from the conduction band edge, Fig.5. This numerical analysis has been performed also for donor type traps. The main outcome is that a hysteresis arises from traps existence. This hysteresis effect is not located in a particular part of the C-V curve, but different parts of such curve are affected depending on traps properties: considering different centre values of traps distribution the region "B" (threshold voltage hysteresis), highlighted in Fig. 5, is modified. More in detail, the curve with traps shifts toward left in voltage, with respect to the reference curve without traps, as the traps distribution moves nearer to the conduction band edge. A hysteresis effect occurs also in region "A", highlighted in Fig. 5, even if this part of the curve is not modified with varying E_{TC}. Also the influence of traps concentration has been considered. In Fig.6, it can be seen that increasing the concentration of acceptor like traps the region "B" of the C-V curve shifts towards right. However, varying traps concentration near conduction band doesn't not vary the region "A". From Fig.7, it can be asserted that increasing the temperature the hysteresis effect is less visible in C-V curves obtained with Drain floating.
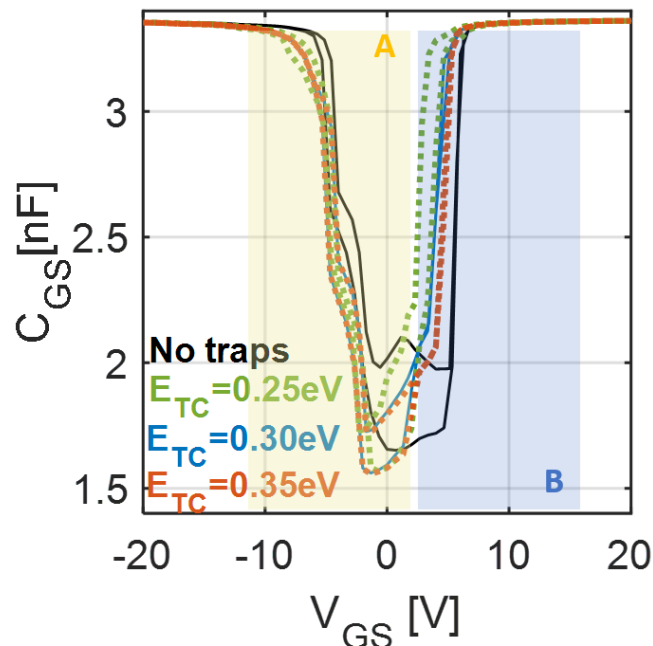
Figure 5. Numerical C-V curves without traps (markers) and with an acceptors trap band with E_{TC} varying. $C_{it}=10^{13}$ cm^{-3}, E_{TW}, $=0.2$ eV, $e_{Xsec} = h_{Xsec}= 10^{16}$ cm^2 and $t_{RISE} = t_{FALL} =300$ ms.
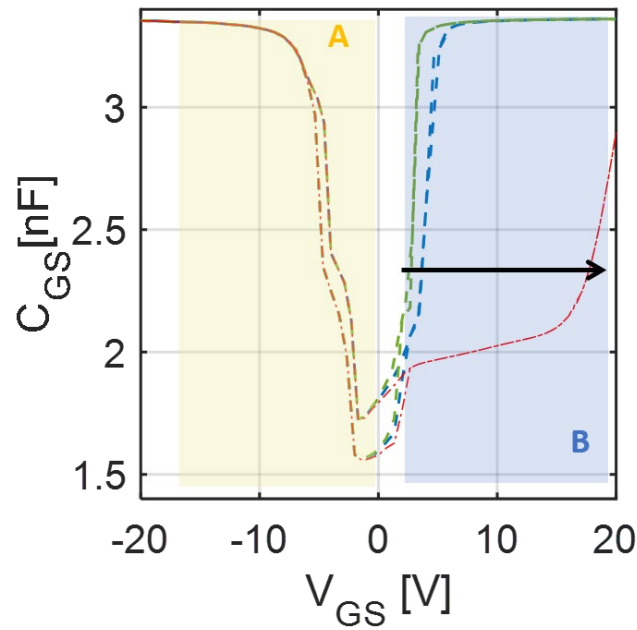
Figure 6. Numerical C-V curves with an acceptor traps distribution with C_{it} varying. E_{TC} =0.3 eV, E_{TW}, =0.2 eV, $e_{Xsec} = h_{Xsec}= 10^{16}$ cm^2 and $t_{RISE} = t_{FALL}$ =300 ms
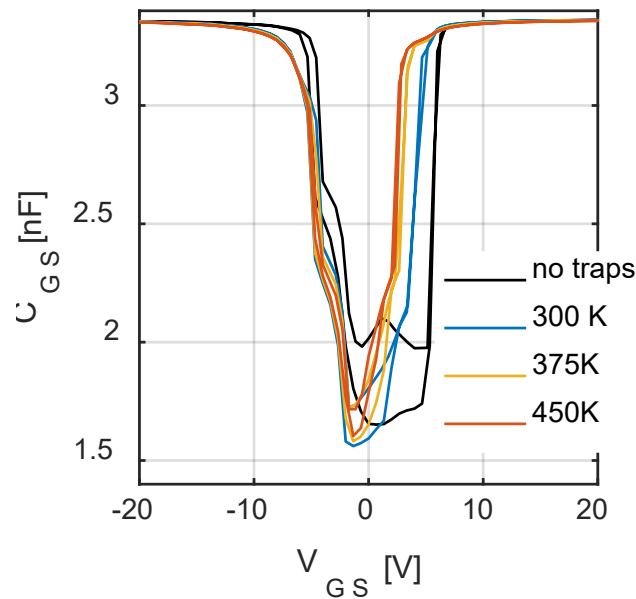

Figure 7. Numerical C-V curves with an acceptor traps distribution with temperature varying. $C_{it}=10^{13}$ cm^{-3}, E_{TC}=0.3 eV, E_{TW}, =0.2 eV, $e_{Xsec} = h_{Xsec}= 10^{16}$ cm^2 and $t_{RISE} = t_{FALL}$ =300 ms.

Experimental Data

The capacitance curves have been obtained using an Impedance Analyzer. The frequency has been imposed to 100 kHz, while the driving voltage V_{GS} has been swept from 20 V to -10 V and vice versa $t_{RISE} = t_{FALL}$ =300 s. The capacitance behavior is different depending on the sweep direction of V_{GS} [6]. For this reason, two sweeps have been considered, the first one from positive to negative voltage (sweep down) and the second one from negative to positive voltage (sweep up). The C-V curves obtained for obtained for a commercial 1200 V SiC MOSFET device are shown in Fig.8. Considering these curves, it is clear as the hysteresis effect consists not only in the shift of the curves obtained during the sweep up and the sweep down but in a considerable distortion of the two curves considered. Two hysteresis effects are visible in these measurements: a first one occurring in the region A of

Fig.8, and the second one taking place around the threshold voltage, region B of Fig.8. Considering the C-V curve obtained numerically for a structure without traps [6], [10], it is evident that the experimental curves show an unexpected behavior. This obtained behavior is caused to a complex traps distribution existing in the device at the SiC/SiO$_2$ interface. This traps distribution cannot be easily measured accessing only to device package and in a non-destructive analysis. Hence the need to perform numerical analysis, on the considered device, in a more complex way. This analysis includes TCAD simulations of the device under test considering interface traps distribution and it allows to have a clearer insight in the device physics along with the experimental capacitance curve behavior. A better understand in traps distribution can be gained by considering the temperature behavior of the C-V curves. In Fig.8, the C-V curves at different temperatures obtained following the same setup values described above have also been reported. The devices under test have been heated at the following temperatures: 300 K, 375 K and 450 K. The hysteresis effect is less evident as temperature increases, when Drain terminal is floating. From these measurements, it can be inferred that the capacitance behavior suffers of visible hysteresis effects.
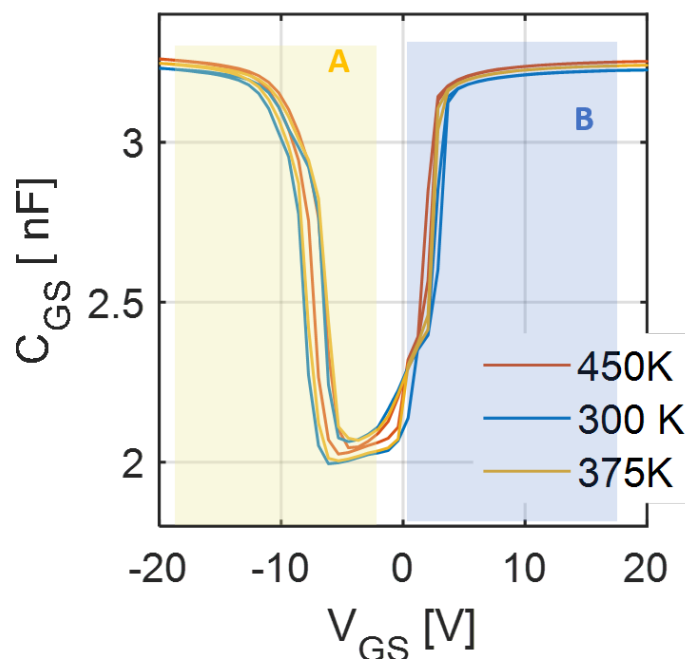
Figure 8. Experimental C-V curves of a commercial SiC power MOSFETs, Cree CMF20120, obtained with floating Drain.

Conclusions

In this work, SiC MOSFET experimental capacitance has been presented when the Drain terminal is floating. These data confirmed behavior of numerical results. TCAD analysis led to a better understanding on the complex traps distribution at the SiC/SiO$_2$ interface. An accurate characterization of the device under test has been performed on the so-measured capacitance taking into account temperature. More in detail, capacitance behavior in temperature highlighted that hysteresis effect is exacerbated at lower temperature.

References

[1] Baliga, B. J. "Fundamentals of power semiconductor devices". Springer Science & Business Media (2010).

[2] C. Raynaud, J. L. Autran, J. B. Briot, B. Balland, N. Becourt, T. Billon, and C. Jaussaud. "Comparison of trapping–detrapping properties of mobile charge in alkali contaminated metal-oxide-silicon carbide structures." Applied physics letters 66, no. 18: 2340-2342 (1995).

[3] V. V. Afanasev, M. Bassler, G. Pensl, and M. Schulz. "Intrinsic SiC/SiO2 interface states." physica status solidi (a) 162, no. 1: 321-337 (1997).

[4] Peters D. et al. "Investigation of threshold voltage stability of SiC MOSFETs." ISPSD (2018).

[5] Okamoto M. et al. "Coexistence of small threshold voltage instability and high channel mobility in 4H-SiC (0001) metal–oxide–semiconductor field-effect transistors." Applied Physics Express, vol. 5, nr. 4, p.041302 (2012).

[6] Maresca, L. et al. "Influence of the SiC/SiO2 SiC MOSFET Interface Traps Distribution on C–V Measurements Evaluated by TCAD Simulations", IEEE Journal of Emerging and Selected Topics in Power Electronics, DOI 10.1109/JESTPE,2940143 (2019).

[7] Sentaurus, T. C. A. D. "Manuals." Synopsys Inc., Mountain View, CA 94043 (2009).

[8] Romano, G., et al. "Short-circuit failure mechanism of SiC power MOSFETs." 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD). IEEE (2015).

[9] Romano G. et al. "A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs." IEEE Journal of Emerging and Selected Topics in Power Electronics 4.3, p.978-987 (2016).

[10] Matacena, Ilaria, et al. "Evaluation of Interface Traps Type, Energy Level and Density of SiC MOSFETs by Means of CV Curves TCAD Simulations." *Materials Science Forum*. Vol. 1004. Trans Tech Publications Ltd, 2020.

[11] Maresca, Luca, et al. "TCAD model calibration for the SiC/SiO 2 interface trap distribution of a planar SiC MOSFET." *2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*. IEEE, 2020.