Experimental Analysis of C-V and I-V Curves Hysteresis in SiC MOSFETs

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Abstract. SiC MOSFETs have already replace silicon-based device in power applications, even if some technological issues are still not solved. The most important of them is related to the complex traps distribution at SiC/SiO₂ interface. Interface traps affect the overall device behavior, modifying channel mobility and introducing hysteresis. In this work experimental C-V and I-V curves are carried out on various commercial SiC MOSFET at different temperatures. The focus is the comparison of hysteresis arising in trench and planar SiC MOSFETs.

Introduction

Silicon carbide (SiC) MOSFETs have replaced silicon devices due to the higher performance of SiC with respect to silicon material [1]. SiC has a higher bandgap and it claims a high thermal conductivity. These properties established the SiC as the most promising material for power MOSFETs. On the other hand, there are some issues not yet solved in technology, as the interface traps density at SiC/SiO₂ interface which affects the overall device behavior. It worth to be noted that traps density at the mentioned interface is order of magnitude higher than traps density existing at Si/SiO₂ interface [2]. Traps density influences the channel mobility [3] and threshold voltage stability introducing also threshold voltage hysteresis [4-5]. For all these reasons, having a deep insight in traps density at such interface and counting on a reliable TCAD model is of paramount importance. At this purpose, experimental characterization of SiC MOSFETs together with the numerical results must be performed [6], [7]. Experimental characterization can be obtained considering current versus voltage (I-V) curves and capacitance versus voltage (C-V) curves. These latter allow to gain knowledge in MOSFET behavior through all its operating regions, as the accumulation, the depletion and the inversion. Nevertheless, capacitance is affected by traps existence and obviously by geometrical and process parameters. This is the case also for transfer I-V characteristics which are influenced by traps distribution. Since traps effect varies with temperature and, more in detail, it reduces as temperature increases, experimental characterization should be carried out at different temperatures.

In this work, after a theoretical introduction to the traps effect on the C-V and I-V curves, experimental C-V curves and I-V curves are presented at different temperatures. This analysis is performed on two different types of SiC MOSFETs: planar and trench devices. These data highlight that in planar devices the hysteresis occurs in both C-V and I-V curves, while this is not the case for trench MOSFETs where the hysteresis stands only in C-V curves.

Traps Effects in SiC MOSFETs

Traps at the SiC/SiO2 interface may introduce hysteresis in the C-V and I-V curve of a SiC MOSFET. Moreover, a strong threshold voltage temperature coefficient may occur if the trap concentration is very high, as for SiC MOSFET devices. In order to better understand traps effects on C-V and I-V curves, numerical analysis has been carried out using Sentaurus environment [8]. The results are presented in this work for a planar SiC MOSFET structure, Fig.1 [6-11] as an example

to carry out general results. The effects of the SiC/SiO₂ interface traps on the capacitance behavior are investigated by implementing the experimental setup in numerical simulations. The equivalent TCAD C-V setup is shown in Fig.2. In this schematic, the driving voltage applied to the gate terminal of the device under test is V_{GEN}, Fig.3. Interface traps dynamics takes into account the time variation in the capacitance behavior. Traps dynamics modifies the carriers distribution as the driving voltage varies. The traps dynamics is considered by changing the t_{RISE} and t_{FALL} values of Fig.3. A small signal AC analysis is performed in Sentaurus for each time step. This framework allows to investigate the driving voltage dv/dt effect on the C-V curves. The interface traps properties considered in simulation are explicated in Fig.4. Traps are considered through a square band distribution with a width, E_{TW}, and a distance from valence and conduction band equal to E_{TV} and E_{TC}, respectively. The adopted approach allows to take into account the effects of interface traps concentration, C_{it}, the capture cross sections, e_{Xsec} and h_{Xsec}, in the numerical model.
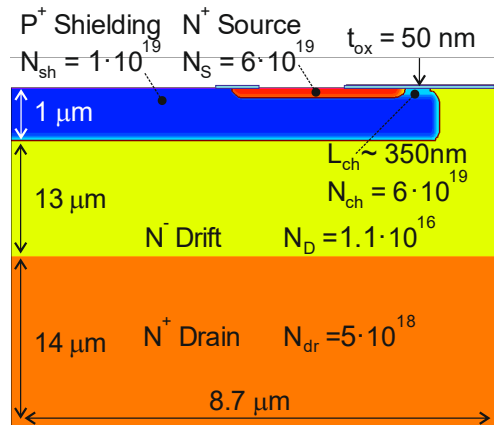

Figure 1. SiC MOSFET TCAD model adopted in this work (the structure is not to scale).
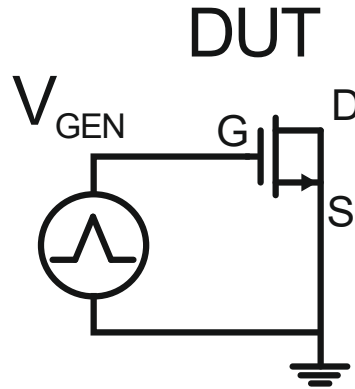

Figure 2. Schematic of the mixed-mode circuit used for the simulation of the C-V experimental setup.
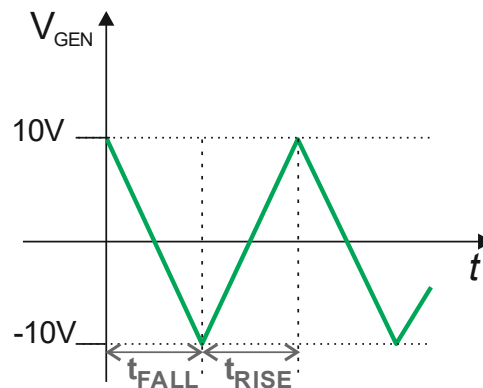

Figure 3. Driving voltage, V_{GEN}, applied to the MOSFET gate.

The numerical C-V curves are presented for acceptor type traps with varying distance from both the conduction and the valence band edge, Fig.5. This numerical analysis has been performed also for donors type traps. The main outcome is that a hysteresis arises from traps existence. This hysteresis effect is not located in a particular part of the C-V curve but different part of such curve are affected depending on traps properties: a) Acceptor type traps near to the valence band affect the region "A", highlighted in Fig. 5; b) Acceptor traps near to the conduction band affect the region "B" (threshold voltage hysteresis), highlighted in Fig. 5; c) Acceptor or donor type traps can be identified by comparing C-V curves obtained from the structure with an interface trap distribution with the C-V curve of the structure without traps taken as reference. Same conclusions drawn in a) and b) apply to the analysis made considering donors type traps in the simulated structure.
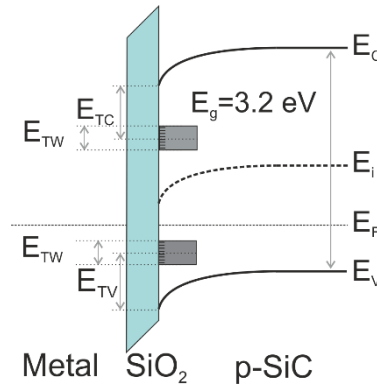

Figure 4. Band diagram of the TCAD structure with trap distribution.

The effects of traps distribution on transfer characteristics (I_D-V_{GS}) have also been studied, Fig.6. A hysteresis effect arises for V_{GS} sweeping from both positive and negative voltage. The numerical framework implemented for the transfer characteristic simulations is shown in the inset of Fig.6. The voltage imposed between Drain and Source terminals is equal to V_{DS}=15 V, the voltage applied on the Gate, V_{GS}, has been scanned from 10 V to 0 V and vice versa. A hysteresis effect occurs for V_{GS} in the range [4 V, 6 V].
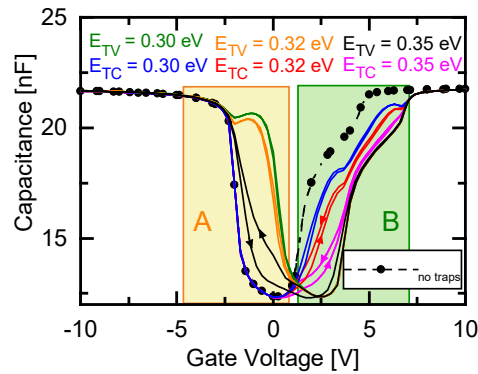

Figure 5. Numerical C-V curves without traps (markers) and with an acceptors trap band with E_{TV} and E_{TC} varying. C_{it}=10^{13} cm^{-3}, E_{TW}, =0.1 eV, e_{Xsec} = h_{Xsec}= 10^{16} cm^2 and t_{RISE} = t_{FALL} =1 ms.
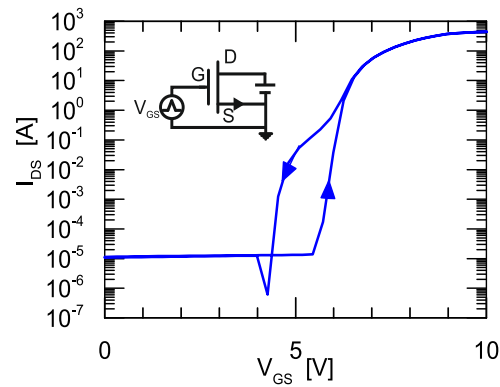
Figure 6. Numerical transfer characteristic obtained considering an acceptor traps distribution with E_{TV} =0.35 eV. In the inset the simulation framework adopted.

Experimental Data

Experimental characterization has been carried out through C-V and I-V curves on both planar and trench SiC MOSFETs. The two considered devices are commercial MOSFETs: device #1 [12] as planar structure and device #2 [13] as trench structure. The capacitance curves have been obtained using an Impedance Analyzer. The frequency has been imposed to 100 kHz, while the driving voltage V_{GS} has been swept from 20V to -10V and vice versa t_{RISE} = t_{FALL} =300 s. The capacitance behaviour is different depending on the sweep direction of V_{GS} [6]. For this reason, two sweeps have been considered, the first one from positive to negative voltage (sweep down) and the second one from negative to positive voltage (sweep up). The C-V curves obtained for the two considered devices are shown in Fig.1. Considering these curves, it is clear as the hysteresis effect consists not only in the shift of the curves obtained during the sweep up and the sweep down but also in a considerable distortion of the two curves considered. It worth to be noticed that the hysteresis effect in device #1 stands only for V_{GS} higher than -15 V, since the two curves overlap in the remaining range. Two hysteresis effects are visible in these measurements: a first one occurring in the region A of Fig.7, and the second one taking place around the threshold voltage, region B of Fig.7. Considering the C-V curve obtained numerically for a structure without traps [6], it is evident that the experimental curves show an unexpected behaviour. The obtained behaviour is caused to a complex traps distribution existing in the device at the SiC/SiO$_2$ interface. This traps distribution cannot be easily measured accessing only to device package and in a non-destructive analysis. Hence the need to perform numerical analysis, on the considered device, in a more complex way. This analysis includes TCAD simulations of the device under test considering interface traps distribution and it allows to have a clearer insight in the device physics along with the experimental capacitance curve behaviour. A better understand in traps distribution can be gained by considering the temperature behaviour of the C-V curves. In Fig.8, the C-V curves are obtained following the same setup values described above. The devices under test have been heated at the following temperatures: 300 K, 375 K and 450 K. The hysteresis effect is less evident as temperature increases in both structures. From these measurements, it can be inferred that the capacitance behaviour of both the planar and the trench SiC MOSFETs considered suffers of visible hysteresis effects.
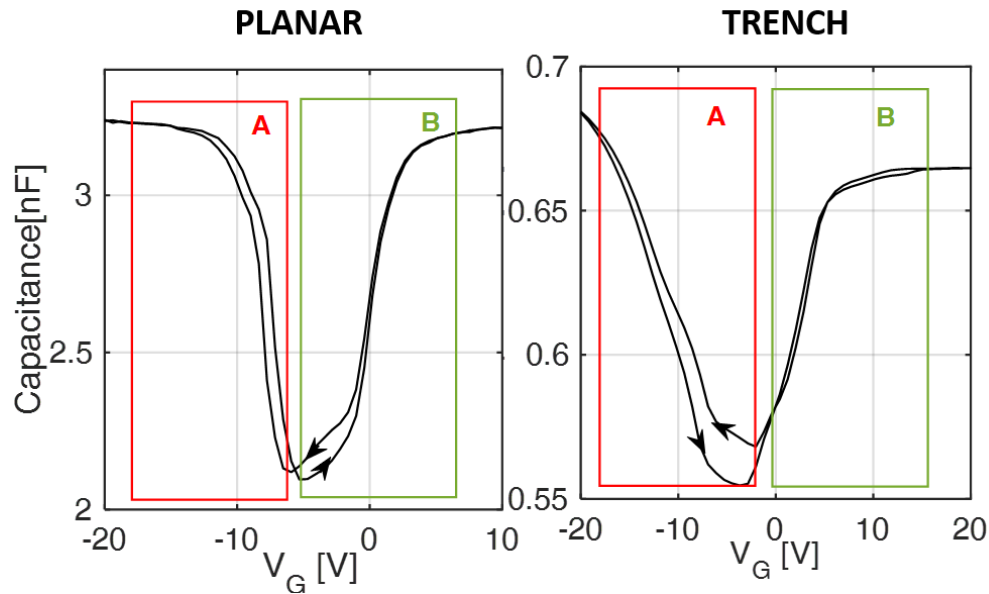
Figure 7. Experimental C-V curves of the two SiC power MOSFETs considered, Cree CMF20120 and Infineon 12M1H140.
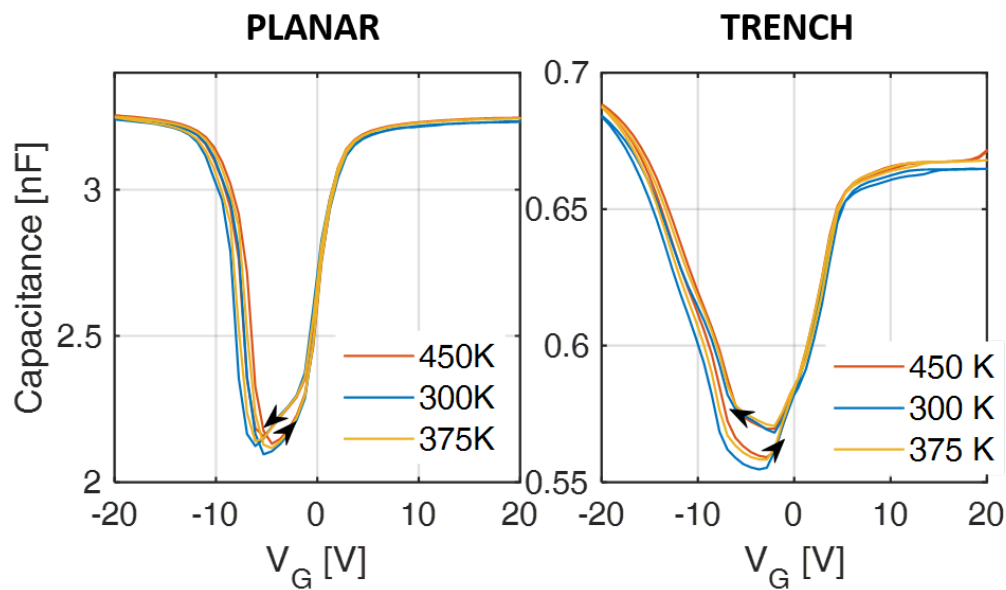

Figure 8. Experimental C-V curves of the two considered devices with temperature varying.

The characterization of the devices under test has been performed also in terms of transfer characteristics. In Fig.9 the I_D-V_{GS} characteristics are shown. These curves have been obtained for a temperature of 300 K, 375 K and 400 K. The curves have been carried out using a pulse I-V tracer. The pulse width has been set to 80 μs. The voltage imposed between Drain and Source terminals is equal to V_{DS}=10 V, the voltage applied on the Gate, V_{GS}, has been scanned from 0 V to 20 V and vice versa. It can be stated from Fig.9, that hysteresis effect is visible only in the planar structure considered, and more in detail this effect is more visible for lower temperature. The I-V curves relative to the trench structure don't show any hysteresis effects.
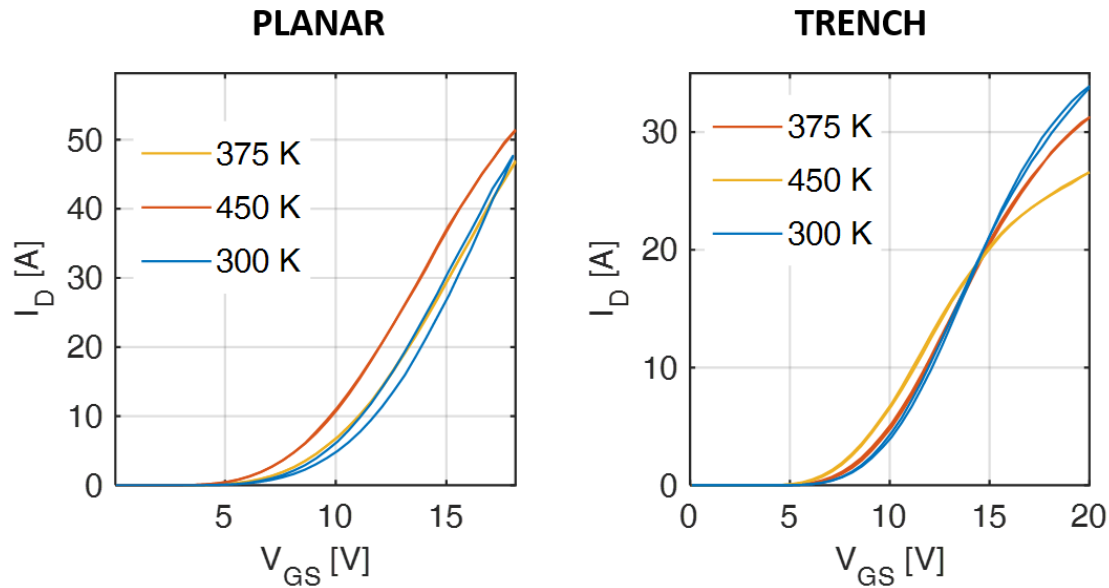
PLANAR   **TRENCH**

Figure 9. Experimental I_D-V_{GS} characteristics obtained for different temperature values for the two considered devices.

Conclusions

In this work, two types of SiC MOSFETs have been characterized: a planar device and a trench structure. Two commercial power SiC MOSFETs have been considered. The characterization has been performed through C-V and I-V curves. From these curves hysteresis effects emerged. More in detail, for planar device hysteresis effects occur in both C-V and I-V curves. For what it concerns the considered trench device, the hysteresis is only visible in C-V curves. All the considered curves have been obtained also with increasing temperature. In particular, considering the C-V curves for both devices it can be stated that hysteresis effects are less visible with increasing temperature.

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