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Behavior of Shockley-Type Stacking Faults in SiC Superjunction MOSFET under Body Diode Current Stress

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Abstract. We evaluated stacking faults expanding by body diode current stress in the SiC Semi-SJ MOSFET for the first time. It was found that body diode degradation of the SJ MOSFETs tends to be smaller than that of conventional Non-SJ MOSFETs. Detailed crystal evaluations revealed that the stacking faults did not expand into the SJ structure. It is assumed that the expansion stops due to low carrier densities. The result suggests that the SJ device has a high potential as a device for suppressing the body diode degradation.

Introduction

Silicon carbide (SiC) has excellent properties such as high maximum electric field and high thermal conductivity. The SiC MOSFET shows lower power loss characteristics than Si MOSFET and has been used as a commercial power device. SiC superjunction (SJ) MOSFET is promising as the next-generation power device with further low on-resistance. In recent years, excellent electrical characteristics of 1.2 kV- and 3.3 kV-class SJ MOSFETs have been demonstrated [1-3]. On the other hand, it is well known that the electrical characteristics of SiC MOSFETs such as on-resistance and forward voltage (V_f) are degraded by the expansion of stacking faults (SSFs) due to body diode current stress [4, 5]. The mechanism and suppressing methods for the expansion of SSFs have been investigated in the Non-SJ SiC MOSFET. In this study, we investigated the behavior of SSFs in the SiC SJ MOSFET for the first time, which expands by body diode current stress. The attractive advantages of SJ MOSFET were discussed in comparison to Non-SJ MOSFETs.

Experiment

Figure 1 shows a cross-sectional schematic of the 1.2 kV-class SJ MOSFET and Non-SJ MOSFET used in this study. The fabrication flow of a 1.2 kV-class Semi-SJ MOSFET is as follows. First, an n-epi layer was grown on a 4H-SiC n-type substrate with an off-cut angle of 4° toward the [11–20] direction. Next, the SJ layer, an epitaxial layer containing the p-type pillar, was fabricated on the n-epi layer by multi-epitaxial method with aluminum ion (Al+) implantation. We defined the p-type pillar as p-pillar and the remaining n-type region as n-pillar. The doping concentrations of the n-epi, p-pillar, and n-pillar are 1.8×10^{16} cm^{-3}, 5.5×10^{16} cm^{-3}, and 3.0×10^{16} cm^{-3}. The thicknesses of n-epi layer and SJ layer are 3.8 μm and 5.2 μm. The p-pillar was patterned in stripes in parallel to [11-20] direction with a pitch of 5.0 μm. A trench gate MOSFET with a cell pitch of 5 μm was employed as the MOSFET structure. The trench bottom p-region functioning as a gate shielding structure is in contact with the source electrode. A buffer layer that enhances hole recombination was not introduced

on the substrate to intentionally expand the SSF from the epi/sub interface [6]. All SJ devices used in this study are Semi-SJ type MOSFET, which consists of an n-epi layer and SJ layer. Non-SJ MOSFETs were prepared as reference samples, with a 10 μm thick drift layer and same chip size as SJ.

The body diode current was applied under stress conditions with current densities of 50-1200 A/cm^2 and the chip temperature of 100-250°C. The stress of 1200 A/cm^2 was applied in pulses with the total on-state time of 5 minutes, and the other current stresses were applied in DC for 10 minutes. The forward I-V characteristics of the MOSFETs were measured before and after the body diode current stresses using a curve tracer Keysight B1505A. The chip temperature and the gate voltage were set to 40°C and -5V, respectively. After the current stresses and I-V measurements, the electrodes and the oxides were removed and photoluminescences were measured. A band pass filter of 460 nm was used to observe SSFs in the SJ MOSFET. Some samples were evaluated in more detail by using the synchrotron radiation topography and cross-sectional TEM. Carrier densities during body diode current stress were calculated by using Sentaurus TCAD simulation.

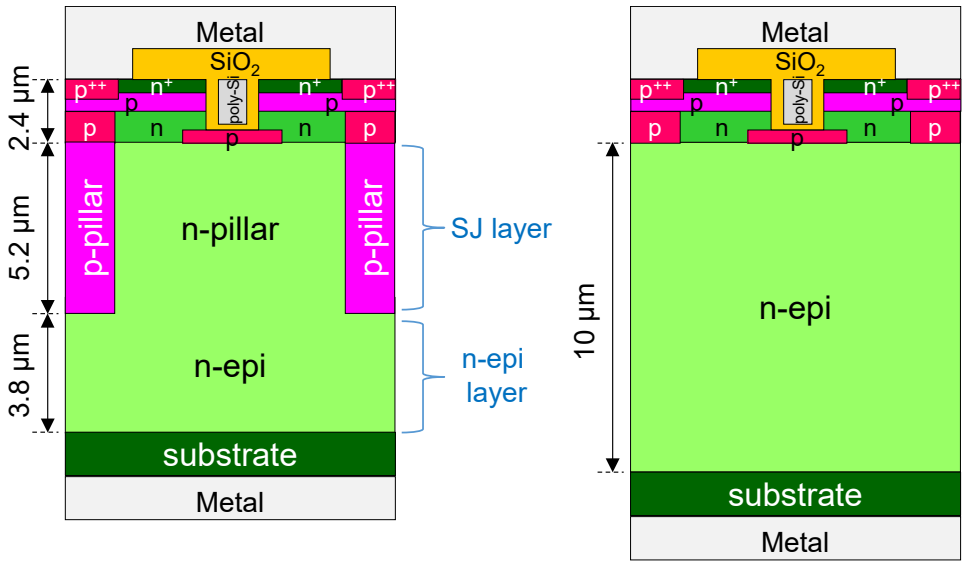

Fig. 1. Schematic of the 1.2 kV-class SJ MOSFET and Non-SJ MOSFET.

Results and Discussion

Body diode current stresses were applied in the order of 50, 300, and 1200 A/cm^2. Figure 2 shows the shift of the V_f against the body diode current stresses. The V_f is defined as the voltage at the current density of 550 A/cm^2 in the I-V characteristics. The V_f shift in typical Non-SJ MOSFET are 3.6 mV for 300 A/cm^2 and 4.5 mV for 1200 A/cm^2. In contrast, the V_f shifts in the SJ MOSFET is 2.0 mV for 300 A/cm^2, which is smaller than that of Non-SJ MOSFETs, and there is no further significant increase even by applying 1200 A/cm^2.

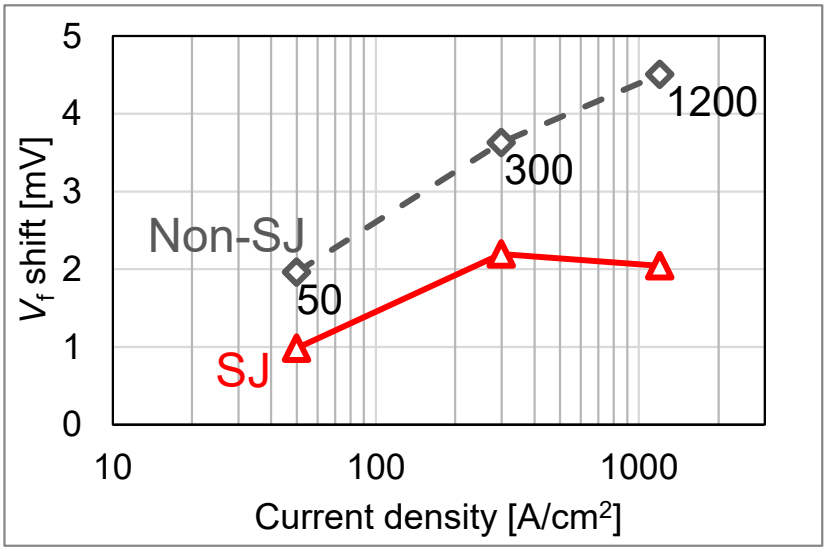

Fig. 2. Shift of forward voltage plotted against current density of the body diode current stresses of the Non-SJ and SJ MOSFETs.

The V_f shift is caused by SSFs expansion because the SSFs have high resistance and prevent the current path. Thus, the size of SSFs correlates with the V_f shift. The sizes of the triangular SSFs after the stress were evaluated by PL images. Figure 3 shows PL images of typical triangular SSFs in Non-SJ and SJ MOSFETs measured for various current densities. The SSF expands in a basal plane with a 4° tilt. Therefore the thickness of the epitaxial layer where the SSF expands is estimated by the width of the horizontal direction. The width of SSF in Non-SJ is 140 µm, which is equivalent to the thickness of the drift layer. On the other hand, the width of SSF in SJ MOSFETs is only 58 µm, which is less than the entire thickness including the SJ layer and n-epi layer. This means that the SSF does not expand throughout the entire drift layers. The width of SSF is equivalent to the thickness of the n-epi layer and is almost the same when the current density is increased up to 1200 A/cm^2.

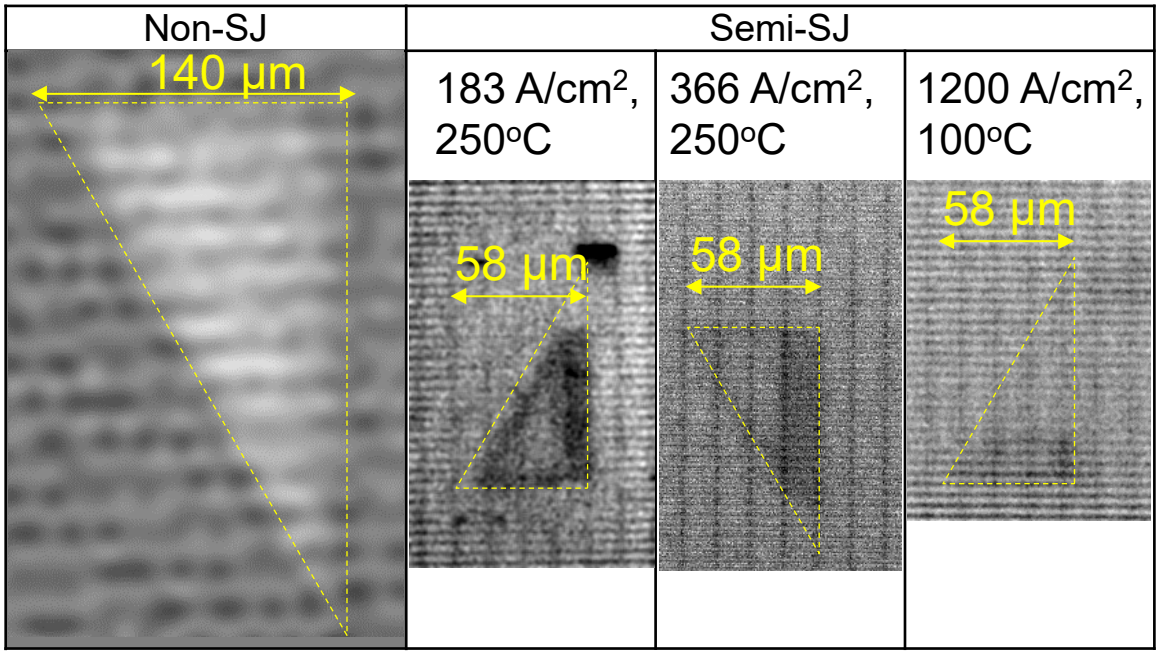

Fig. 3. Photoluminescence images of epitaxial layer of Non-SJ and SJ MOSFETs.

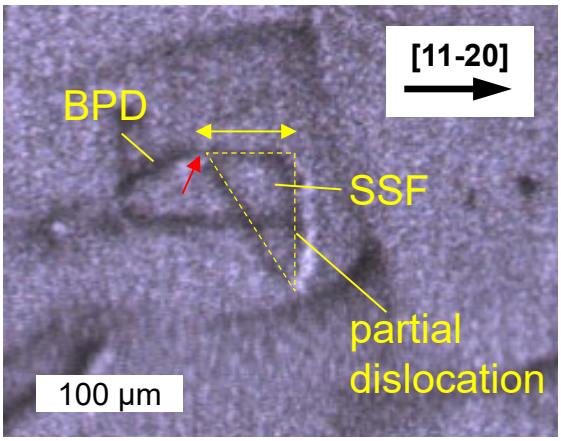

Fig. 4. Synchrotron radiation topographic image of SSF in SJ MOSFET.

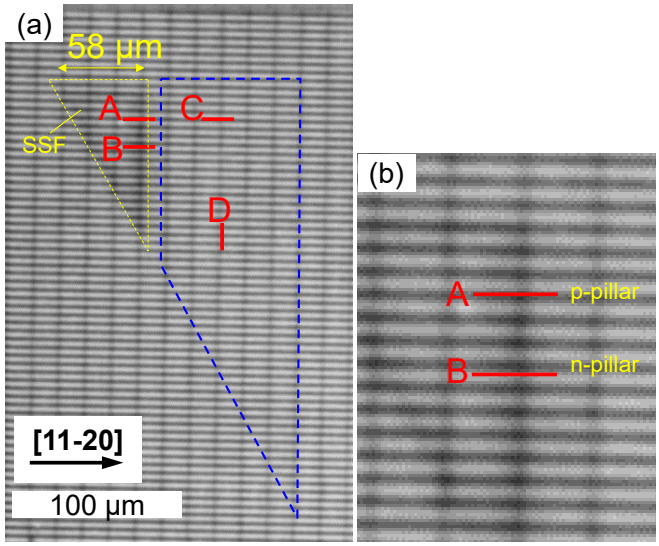

Fig. 5. (a) PL image of SJ MOSFET. A-D indicates the area for cross-sectional TEM observation. (b) Magnified image near the line segments A and B

The PL images of SSFs are not clear in SJ MOSFETs because the high doping densities of p- and n-pillars weaken the contrast of the SSFs. Therefore it is uncertain whether the SSF is really small or same size as Non-SJ but invisible due to the high doping density. The overall shape of SSFs was confirmed by synchrotron radiation topography, which allows observation of partial dislocations and basal plane dislocations (BPDs) without the effect of doping density. Figure 4 shows the synchrotron radiation topographic image of SSFs with the SiC [0-2210] as the diffraction surface in the SJ MOSFET sample. The current density of 183 A/cm^2 has been applied at the chip temperature of 250°C. Partial dislocations were clearly observed at the boundary around the SSF. The width of the SSF indicated by the yellow arrow is almost the same as that observed by the PL. The BPD is also observed near the corner of the SSF, indicated by the red arrow. It was confirmed that the SSF starts expanding from the BPD and the width in SJ MOSFETs is less than that assumed from the thickness of the entire drift layer.

Cross-sectional TEM images of SJ MOSFETs were taken to confirm the position where SSF stopped. Figure 5(a) shows a PL image in the SJ MOSFETs after current stress of 183 A/cm^2. The yellow dashed line indicates the size of SSFs observed by PL and the blue dashed line indicates the size of SSF if it had expanded to the entire drift layer. However, no SSFs are visible inside the blue dashed line. Figure 5(b) is a magnified image near the line segments A and B that are inside the p-pillar and n-pillar, respectively, and cross the boundary of visible SSFs.

Figure 6(a) and (b) show cross-sectional TEM images and schematics correspond to the line segments A and B. The SSFs were found in both images at a depth position of 7.6 μm from the SJ-MOSFET surface, indicating the presence of a SSF in the n-epi layer. Figure 6(c) is a cross-sectional TEM image corresponding to line segment C, which is the position shifted by 50 μm from line segment A toward the [11-20] direction. No SSFs were observed in the TEM image, indicating the SSFs are not present in the p-pillar. Figure 6(d) is cross-sectional TEM images corresponding to line segment D, which has the orthogonal direction to the line segment C. SSFs were not observed in the p- and the n-pillars. These results indicate that the expansion of SSF is stopped near the interface between the n-epi layer and the SJ layers. It is expected that the SJ structure or its fabrication process is causing the suppression of the SSF expansion.

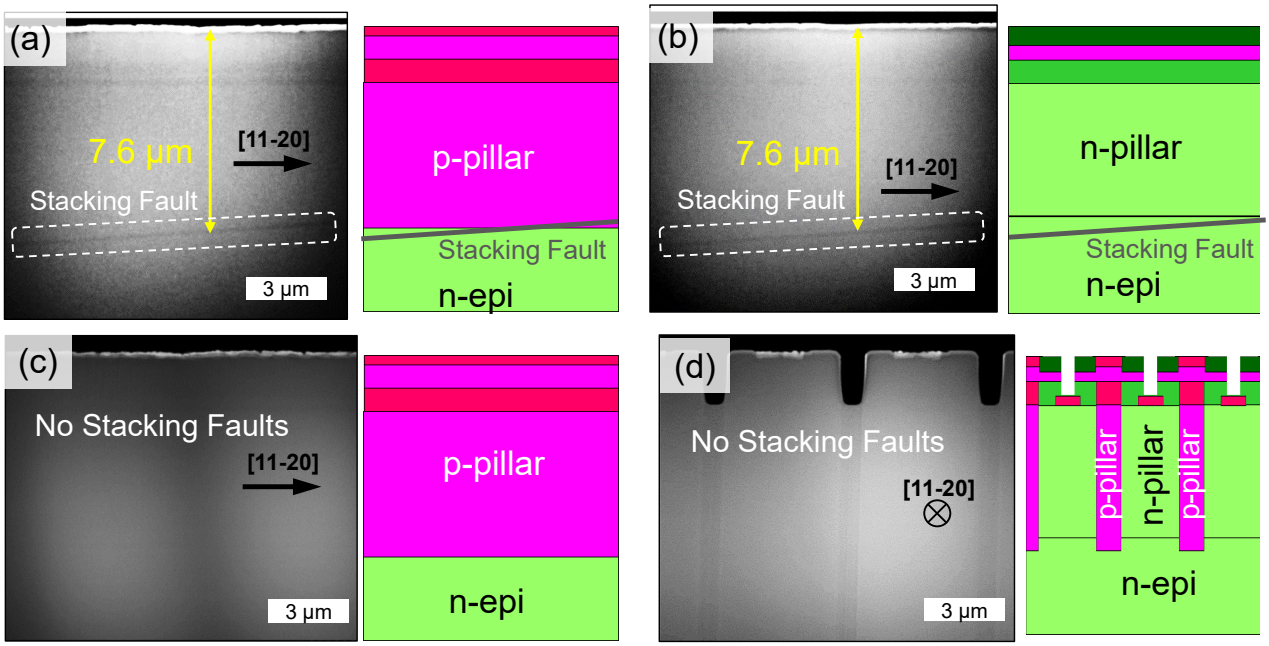

Fig. 6. Cross section TEM images and their schematics of SJ MOSFET. The cross-sectional TEM images (a-d) correspond to the line segments A-D.

We consider the mechanism for stopping the expansion of SSFs in terms of carrier density because carrier density is one of the most important factors for the expansion of SSF. Electron and hole densities under the body diode current stress were estimated by using a device simulator. Figure 7 shows the cross-sectional structure and cut line plots under stress conditions with the current density of 300 A/cm^2 and the chip temperature of 250°C. The cut line positions are inside the p-pillar for the electron density, and inside the n-pillar for the hole density. The carrier lifetime of SiC is assumed to be shortened by the ion implantation damage and high doping density, so it is set to 1/10 of the typical value within the p-pillar and n-pillar [7]. In the Non-SJ, the electron and hole densities are estimated to be 5×10^{16} cm^{-3} and 4×10^{16} cm^{-3} over the whole area of the drift layer. They are high enough to expand SSFs because threshold excess carrier density at 250°C is estimated at around 5×10^{15} cm^{-3} [8, 9]. On the other hand, in the SJ MOSFETs, the electron and hole densities near the interface between the n-epi layer and the SJ layer are estimated to be much lower than those of Non-SJ, and close to the threshold excess carrier density.

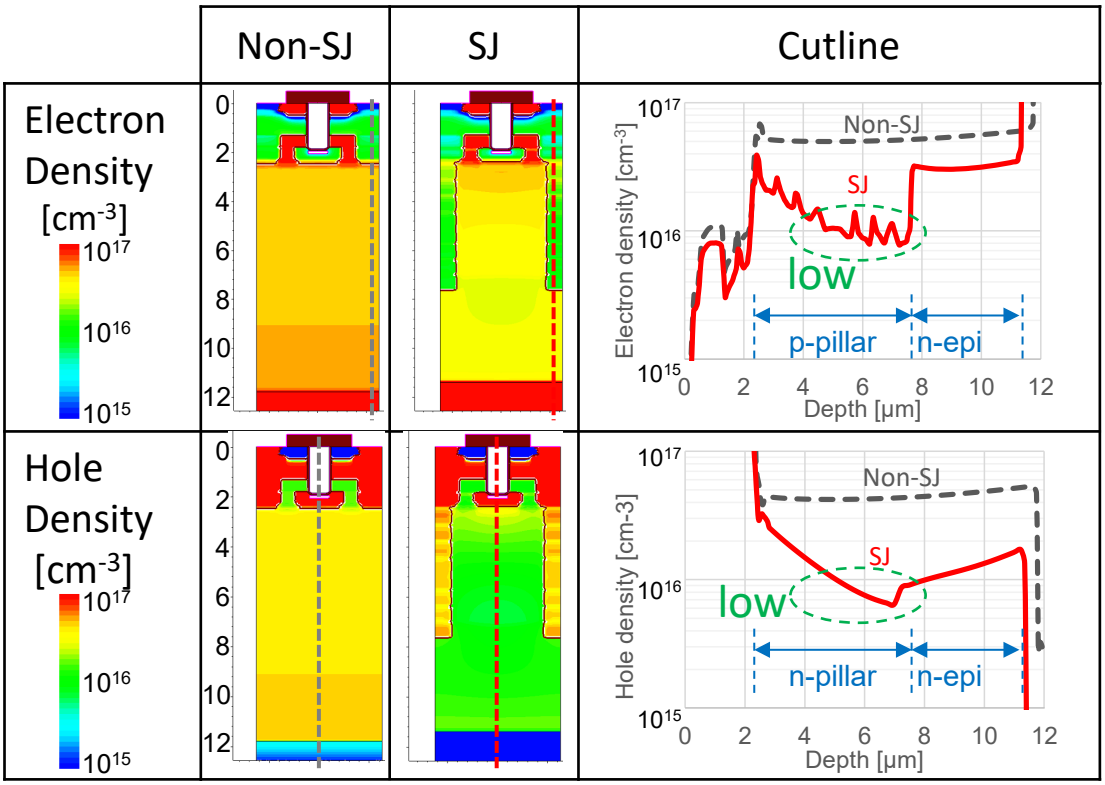

Fig. 7. Cross-sectional structure of Non-SJ and SJ MOSFETs. Right figures show electron and hole density profiles along the cut lines.

Figure 8 shows a 3D cross-sectional schematic of the SSF in the SJ MOSFET. Most of BPDs propagating from substrates are converted to threading edge dislocations (TEDs) at the n-epi layer/substrate interface. The SSFs expand along the basal plane from the BPDs near the n-epi layer/substrate interface. The expansion of SSF goes through the n-epi layer due to the high carrier density in the n-epi layer. When the SSFs reach the bottom of the SJ layer, the expansion stops in [11-20] direction due to the low carrier density which is shorted by the ion implantation damage and high doping density. It is expected that in the case of full-SJ with a long p-pillar, the expansion of SSFs is further small and the body diode degradation is more suppressed. If the SJ structure suppresses the expansion of SSFs even in a wide temperature range and high current density, it is possible to use body diode without Shottky diode in parallel with MOSFET. This may lead to chip cost deduction. This suppression of body diode degradation is an attractive advantage of SJ-MOSFET.

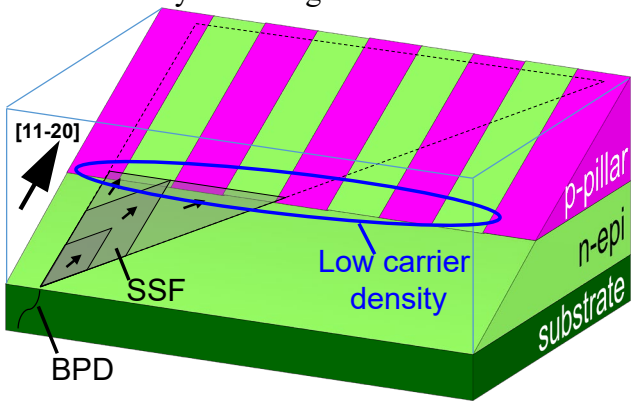

Fig. 8. 3D cross-sectional schematic of SSF in the SJ MOSFET.

Summary

In this study, we investigated the behavior of SSFs expanding by body diode current stress in the SiC SJ MOSFET for the first time. It was demonstrated that the expansion of SSF was effectively suppressed even at the high current density of 1200 A/cm^2 and found that SJ MOSFET had a smaller SSF size and lower forward voltage shift than Non-SJ MOSFET. The expansion of SSFs stops near the interface between the n-epi layer and SJ layers due to low carrier densities in the SJ layers. The MOSFET with the SJ structure has a high potential as a device not only reducing the on-resistance but also for suppressing the body diode degradation. In the future, the attractive advantage of SJ-MOSFET will contribute to expanding the application area of SiC SJ devices. We will investigate in detail high voltage class devices and Full-SJ devices in the future.

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