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Robustness of Semi-Superjunction 4H-SiC Power DMOSFETs to Single-Event Burnout from Heavy Ion Bombardment

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Abstract. We compare the failure mechanism and performance of a silicon carbide (SiC) semi-superjunction (semi-SJ) power DMOSFET against pure SJ and conventional DMOSFET when struck by a single heavy ion. The Single-Event Burnout (SEB) failure mechanism was identified as the thermal runaway from second breakdown resulting in mesoplasma formation. The semi-SJ design shifts the mesoplasma location from the drift/substrate interface seen in the control device structures to a location along the center of the P-pillar and closer towards the DMOSFET surface, thus significantly improving the SEB threshold voltage (V_{SEB}). The V_{SEB} varies with pillar width and ratio of pillar thickness to drift layer thickness. A maximum value of V_{SEB} is reached when the pillar to drift layer ratio is 0.9 and the pillar width is 2.4 μm. The semi-SJ SEB/breakdown voltage ratio is 100% and 13% higher than the pure SJ and conventional DMOSFET, respectively. Using a new Figure of Merit (FoM), which accounts for the tradeoff between V_{SEB} and on-state performance, we find that the SiC semi-SJ DMOSFET achieves a FoM that is 1.8 and 8 times higher than SJ and conventional DMOSFET, respectively, making the semi-SJ a competitive candidate for radiation hardened applications.

Introduction

Vertical 4H-SiC based power devices are of interest in power electronics applications that require breakdown voltages (BV) greater than 300V by providing improved efficiency compared to Si-based devices. Even greater efficiency can be achieved using a superjunction (SJ) design, which can reduce $R_{on,sp}$ significantly below the 1-D limit [1]. In space applications, however, high-voltage 4H-SiC power devices are susceptible to the single-event burnout (SEB) due to heavy ion strikes, causing the catastrophic destruction of the device. It has been shown experimentally that SEB, in conventional DMOSFETs, can occur at less than 50% of the device rated blocking voltage [2]. The failure process has been analyzed by simulations, and it is initiated by the generation of an electron-hole plasma from the heavy ion strike, enhancing the electric field at the N epitaxial/N+ substrate interface (Kirk effect), leading to the formation of a mesoplasma at the interface [3]. Further simulation study shows that the SEB threshold voltage (V_{SEB}), for conventional DMOSFETs, can be increased by inserting a buffer layer between the epitaxial and substrate layers, which helps suppress the electric field enhancement [4]. In this paper, we demonstrate that the V_{SEB} can be increased substantially in semi-SJ devices which are derived from SJ devices by adding a uniformly doped layer between SJ pillars and substrate.

Semi-SJ Simulation Models

The semi-SJ model investigated has a 31 μm thick drift layer (X_{Total}), with a portion of the drift taken up by the alternating N+/P+ SJ pillars (X_{SJ}) and the remaining thickness having a uniformly

doped layer (X_{TFL}) labeled as triangular field layer (TFL) seen in Fig. 1b. The TFL is designed so that a triangular electric field profile forms across the TFL when the device undergoes avalanche breakdown. Two different pillar widths for the SJ portion were explored (1.2 µm and 2.4 µm) along with 3 different semi-SJ ratios (0.9, 0.75, and 0.5), which is calculated by dividing X_{SJ} by X_{Total}. The semi-SJ structure was also compared against a pure SJ and conventional DMOSFETs with equal total drift region thickness seen in Fig. 1c and 1d.

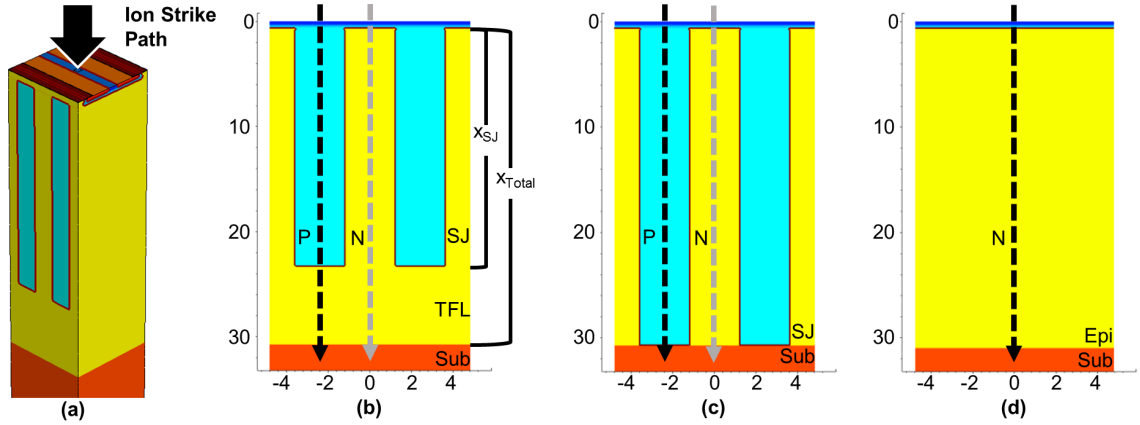

Fig. 1. Simulation models showing a) 3-D view of the semi-SJ, 2-D cross-section of b) semi-SJ, c) SJ, and d) conventional DMOSFETs. Black dotted lines denote simulated heavy ion path. Axis in µm.

Single-Event Burnout Simulations and Results

The SEB event was simulated using 3-D transient electro-thermal models described in prior work [3]. The heavy ion used in these simulations is a 1289 MeV silver ion with a linear energy transfer of 46 MeV-cm^2/mg. Center of the P- and N-pillar strike locations were investigated, however it was found that the P-pillar is the weakest location and only these results will be presented. SEB was declared when the lattice temperature reaches 3000 K in simulation, which is the decomposition temperature of SiC and has previously been found to produce SEB results that are in agreement with test results from conventional DMOSFETs [3].

Fig. 2 shows the V_{SEB} for various pillar widths and semi-SJ ratios used for the semi-SJ DMOSFET. The pure SJ and the conventional DMOSFET results are for semi-SJ ratios of 1 and 0 in the figure, respectively. The maximum V_{SEB} occurs when the semi-SJ ratio is 0.9, and the V_{SEB} is 2050V. This configuration is used to discuss the SEB failure mechanism. When the heavy ion strikes the SiC crystalline lattice, electron-hole pairs are generated [5,6], and the resulting density exceeds the background doping concentration by several orders in the drift region. These charge carriers traverse the devices to their respective terminals, with the electrons going towards the drain

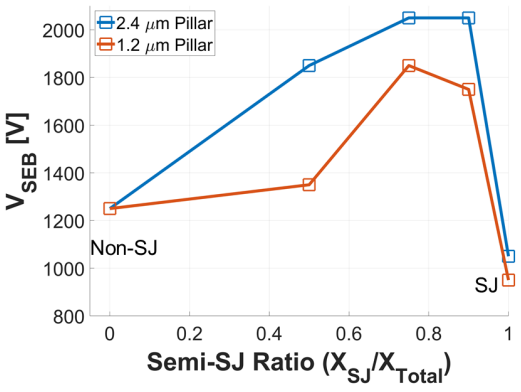

Fig. 2. V_{SEB} dependence on semi-SJ ratio for 2.4 and 1.2 µm pillar widths.

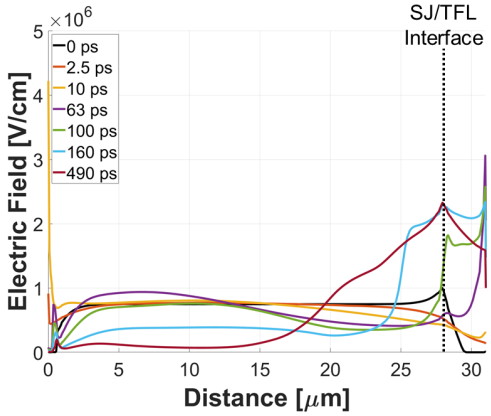

Fig. 3. 1-D time evolution of electric field for 0.9 semi-SJ ratio and pillar width 2.4 µm along the heavy ion track at 2100 V.

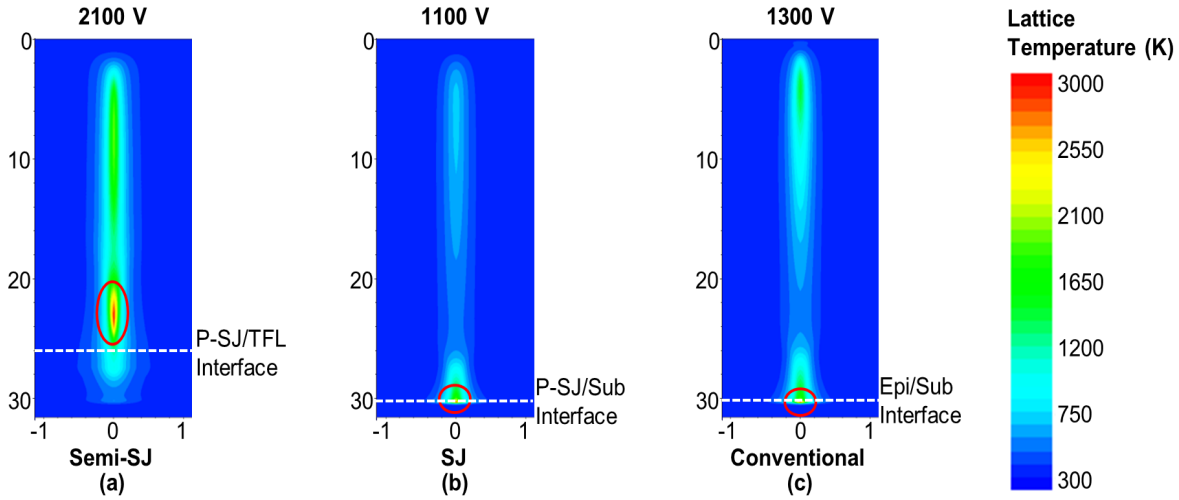

Fig. 4. 2-D lattice temperature graphs showing the failure location (formation of the mesoplasma) for P-pillar strikes of 2.4 µm widths of a) Semi-SJ, b) SJ, and c) conventional DMOSFET designs. Axis in µm.

and the holes towards the source contact. This movement results in the distortion of the electric field profile, a typical phenomenon of the Kirk effect, as seen in Fig. 3. By 2.5 ps, an enhancement is seen under the source contact (0 µm) and at the TFL/substrate interface (31 µm). This behavior is due to the buildup of excess holes and electrons under the source contact and TFL/substrate interface, respectively. The field under the source contact is short-lived and by 63 ps, it effectively disappears because the carriers short the source/body and body/drift junctions, causing an injection of electrons from the source region. These electrons help to balance the excess holes and effectively neutralize the surface electric field.

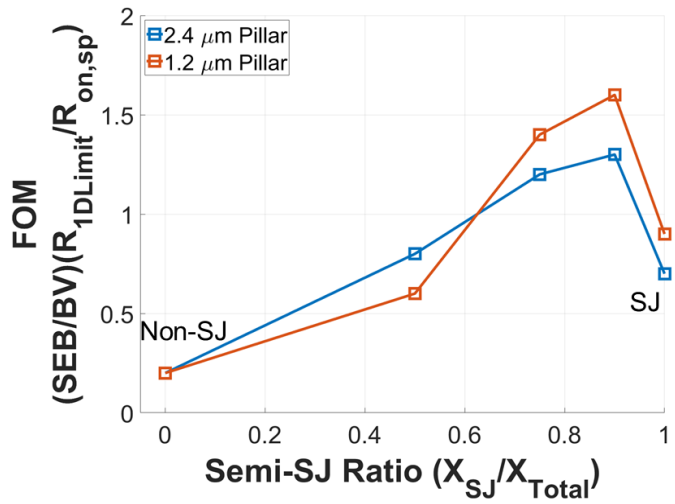

Fig. 5. FoM dependence on semi-SJ ratio for 2.4 and 1.2 µm.

Despite the surface field reduction, the field at the TFL/substrate interface continues to increase and reaches a maximum value of 3.1 MV/cm by 63 ps. This field enhancement would normally lead to significant impact ionization causing additional carriers to be generated yielding high localized current densities and eventually the formation of a mesoplasma [3,4]. This is the failure mechanism and location for both the conventional and pure SJ DMOSFET seen in Fig. 4b and 4c. However, with the introduction of the TFL, the electric field starts to shift from the TFL/substrate interface to the SJ/TFL interface by 100 ps. Despite the shifting of the electric field and the reduction from 3.1 to 2.3 MV/cm by 490 ps, the semi-SJ DMOSFET experiences SEB near SJ/TFL interface as seen in Fig. 4a. The failure mechanism is due to the sustained heating near the interface from the charge carriers generated from the impact ionization event leading to the formation of a mesoplasma 26 µm

deep in the SJ layer. This shifting of the electric field and the resulting mesoplasma significantly improves the V_{SEB} to almost twice that of the pure SJ and conventional DMOSFETs.

Table 1. Summary of static and SEB performance of SJ, conventional, and semi-SJ DMOSFETs

Semi-SJ Ratio	V_{SEB} (V)		BV (V)		$R_{on,sp}$ (mΩ-cm^2)		$R_{1DLimit}$ (mΩ-cm^2)		FoM: SEB/BV*$R_{1DLimit}$/$R_{on,sp}$	
	2.4 μm	1.2 μm	2.4 μm	1.2 μm	2.4 μm	1.2 μm	2.4 μm	1.2 μm	2.4 μm	1.2 μm
1.0	1050	950	5103	5077	4.2	3.2	13.6	13.5	0.7	0.9
0.9	2050	1750	4911	4897	4.1	3.2	11.7	11.6	1.3	1.6
0.75	2050	1850	4631	4619	4.2	3.4	8.8	8.8	1.2	1.4
0.5	1850	1350	4145	4146	4.9	4.3	6.3	6.5	0.8	0.6
0.0	1250		3354		8.0		5.2		0.2	

Performance Comparison

Table 1 summarizes the simulated static on-state and blocking characteristics, SEB performance, and a new Figure of Merit (FoM) for all three DMOSFET (conventional, SJ, and semi-SJ) designs. This new FoM highlights the tradeoff between SEB and on-state performances. In Fig. 5, we can see, using this new FoM, that the overall performance of these Semi-SJ DMOSFETs is 78-86% better than that of SJ devices. This is due to the substantial, 64-116%, improvement in the V_{SEB} in both SJ and conventional devices (Fig. 2), with only a small, less than 10%, increase in specific on-resistance. In addition, the failure (mesoplasma formation) location has shifted to a spot about 26 μm from the surface within the P-pillar for the Semi-SJ case, as illustrated in Fig. 4a. This change in mesoplasma location allows a higher blocking voltage to be supported during heavy ion bombardment by mitigating the peak electric field and suppressing carrier impact ionization cascades. Additionally, when compared to commercially available 1200 V rated conventional DMOSFETs [7], the specific on-resistance is only 19% higher when using the best FoM design with pillar width of 1.2 μm and a semi-SJ ratio of 0.9.

Summary

Using simulations, the mechanisms for SEB failure in semi-SJ power devices from a single heavy ion strike have been investigated. We have shown that the failure is due to the enhancement of the electric field at the SJ/TFL interface causing thermal runaway from impact ionization leading to the formation of a mesoplasma. When compared to the pure SJ and conventional DMOSFET designs, the semi-SJ can achieve superior SEB performance that is almost twice that of either SJ or conventional and a specific on-resistance that is 60% lower than the conventional. This makes the semi-SJ DMOSFET design a suitable candidate for applications requiring radiation hardening.

Acknowledgments

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