Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 8-12
doi:10.4028/p-8302i1

Submitted: 2021-09-22
Revised: 2022-02-11
Accepted: 2022-03-14
Online: 2022-05-31

Liquid Si-Induced 4H-SiC Surface Structuring Using a Sandwich Configuration

Yann Jousseaume[1,a*], François Cauwet[1,b], Gabriel Ferro[1,c]

[1]Laboratoire des Multimatériaux et Interfaces, Université de Lyon, 6 rue Victor Grignard, 69622 Villeurbanne, France

[a]yann.jousseaume@univ-lyon1.fr, [b]francois.cauwet@univ-lyon1.fr, [c]gabriel.ferro@univ-lyon1.fr

Keywords: Surface structuring, step-bunched morphology, sandwich, liquid silicon

Abstract. In view of obtaining a step bunched morphology on large 4H-SiC surfaces, a sandwich configuration is investigated. A piece of silicon is melted between two 4H-SiC 4° off wafers, allowing a better spreading of the liquid than a Si drop approach. This successfully leads to highly step-bunched surfaces, though with irregular steps. The most regular step and terrace stuctures were found to be the result of epitaxial growth via a dissolution-precipitation process occuring from the edges to the center of the wafers. This is probably caused by radio-frequency induced electromagnetic convection within liquid Si. This process is quenched when using smaller liquid thickness.

Introduction

Despite the attractive properties and already wide use of silicon carbide in power electronics, the performances of SiC metal-oxide-semiconductor field effect transistors (MOSFETs) remain limited due to low channel mobility. A high density of electrically active defects at the SiO_2/SiC interface is being held accountable for this limitation [1]. While the origin of these interfacial traps is still under debate, recent experimental studies [2] attribute them to the micro/macro step-bunched morphology inherent to commonly used off-axially grown epitaxial surfaces [3]. Such a morphology is expected to critically impact the quality of the SiO_2/SiC interface, for instance by initiating non-ideal oxidations and nonstoichiometric near-interface regions [4].

A recent study has found that MOS capacitors fabricated on macrostepped surfaces show a systematic decrease of the interface traps density of ~10-15% compared to “standard” samples [5]. Although this work gave an interesting direction for further study, it also raised the issue of controlling the formation of such 4H-SiC macrostepped surfaces. A simple way would be to put a 4H-SiC wafer in contact with a liquid Si drop [6,7]. The induced atomic rearrangement would generate the reconstruction of the 4°off surface with very large terraces of few µm width, which is more than 100 times wider than those found in standard epitaxial surfaces grown by chemical vapour deposition (CVD). But while such a Si drop approach was appropriate for preliminary demonstration and for small areas of ~0.5 cm^2, its extrapolation to industry-scale areas (full 4-6" wafer) is clearly not straightforward. A substancial increase in the sample size would require the development of a set up where the liquid silicon would be more spread over the SiC surface. This is the goal of the present work.

Experimental

In order to force the spreading of the liquid Si, a sandwich configuration is investigated. The sandwich consists in a SiC/Si/SiC stacking where a piece of n type Si wafer is placed in between two 4H-SiC (0001) 4°off Si-face wafers (see Fig. 1 left). To avoid any Si loss upon melting from the 4H-SiC wafers sides, the chosen lateral size of the bottom wafer (SiC bottom) is larger than the top one (SiC top), i.e. 2x2 cm^2 and 1.2x1.2 cm^2 for the bottom and top wafers, respectively. The pressure applied by the top wafer should force the liquid Si to spread on both surfaces until reaching the square edges of the SiC-top wafer (Fig. 1 right). Such natural spreading is expected to lead to homogeneous Si liquid thickness between the SiC wafers, which are thus considered parallel. We

will also assume that the area occupied by the liquid Si is equal to the surface of the SiC-top wafer, with no liquid overflow (this was confirmed experimentally). With these assumptions, we are able to calculate the theoretical liquid thickness from the mass of the initial Si wafer piece.

After ultrasonic cleaning in methanol of each part of the assembly, the stacking is placed upon a graphite susceptor which is then inserted in a RF-heated homemade vertical cold wall CVD reactor working at atmospheric pressure under H_2. Such cold wall configuration under flowing H_2 can generate substantial vertical thermal gradient if the sample is thick enough. A typical experiment consists in heating the assembly above Si melting point (1550-1600°C) for 30-120 min and then cooling it. The elaboration conditions of the samples studied here are listed in Table 1. After removing the sample from the reactor, the solidified Si is chemically etched in a mixture of $HF+HNO_3$ for several hours. The obtained reconstructed surfaces of both SiC top and bottom wafers are examined on the one hand using optical microscopy to study the obtained macrostepped morphology, and on the other using mechanical profilometry to check the homogeneity of the surface structuring process and the possible occurrence of any mass transport phenomenon.

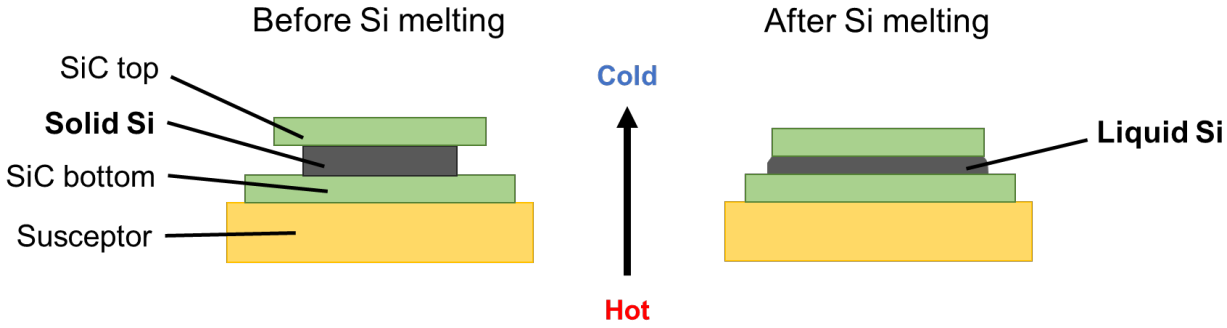

Figure 1. Schematics of the investigated sandwich set up and the expected thermal gradient direction in this configuration before and after Si melting.

Table 1. Elaboration conditions of the investigated samples.

Sample	Temperature [°C]	Time [min]	Si liquid thickness [µm]
A	1550	30	30
B	1550	120	30
C	1600	30	30
D	1550	30	400

Results and Discussion

First, as shown in Fig. 2, every 4H-SiC wafer treated in this work displays a pronounced macrostep bunching which is easily visible by optical microscopy. Interestingly, in the case of the SiC top wafers, 100% of the surface is step-bunched. This confirms the potential of the liquid Si interaction approach for macro-structuring of 4H-SiC surfaces on large areas. But the precise step structure of each wafer varies depending on both its position within the stack and the experimental conditions. For instance, the bottom wafers always display wider terraces than the top ones. Comparing samples A and B, it can be noted that an increase from 30 to 120 min of the interaction duration does not a have a significant effect on the resulting SiC surface morphology. Increasing temperature from 1550°C (sample B) to 1600°C (sample C) has a more pronounced effect essentially for the bottom SiC, which displays wide but highly irregular steps. Increasing Si liquid thickness from 30 to 400 µm (sample D) leads to a significant improvement of the straightness of the steps which are now clearly all parallel. This is precisely towards such a surface reconstruction that the present work aims at. The uniformity of this reconstruction has yet to be verified, as well as the possible occurrence of mass transport within the system. For that purpose, 3D profilometry mapping on both top and bottom wafers of samples B and D (Fig. 3) was performed. It can be observed that the “best” reconstructed surface of sample D is also the less homogeneous in terms of

height variation across the wafer. On this sample, both top and bottom wafers display a butterfly-like pattern with positive (up to +6 µm) height while the edges are delimited with -6 to -9 µm depressions. In the case of sample B (with only 30 µm liquid thickness, Fig. 3 right), the 3D maps are visibly much flatter on both top and bottom wafers, even though the bottom SiC wafer displays a central bumping at ~ +3 µm with edge delimitation at ~ -4µm.

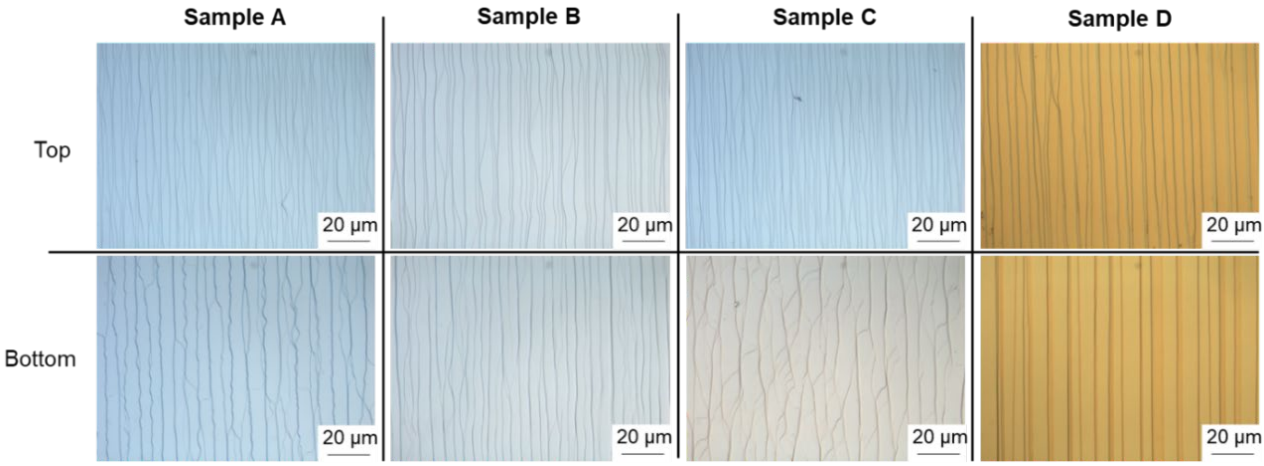

Figure 2. Optical microscopy images of the top and bottom SiC wafers from the investigated assemblies (see Table 1) after interaction with molten Si. Images are taken at the center of each wafer.

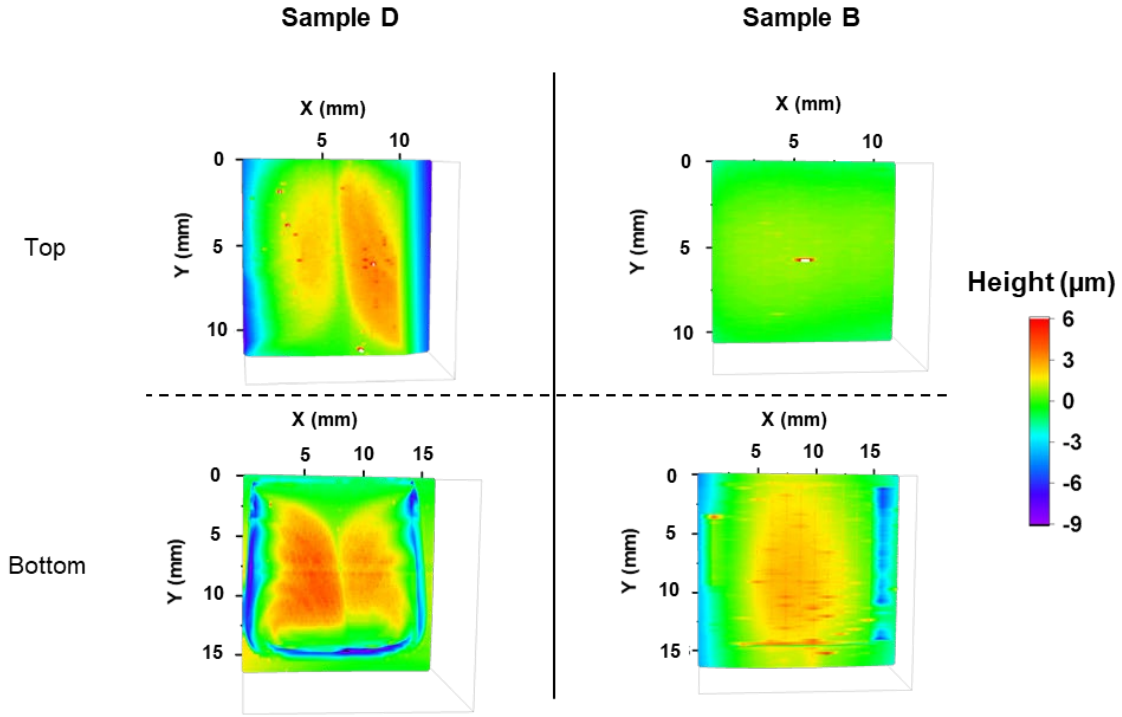

Figure 3. 3D profilometry maps of the top (up) and bottom (down) 4H-SiC wafers of sample D and sample B.

The 3D mapping results suggest that some matter transport, from the edges to the center of the wetting area, occurs on both SiC wafers of the same assembly. All seems to happen like if the edges were preferentially etched and the dissolved carbon was transported to the center where it precipitated to form epitaxial SiC. The fact that both top and bottom wafers display the same pattern suggests that this dissolution-precipitation process takes place on the same SiC surface and not from one surface to the other. According to the expected vertical thermal gradient within the assembly during the treatments (see Fig. 1), one would have expected the main C transport to be from the

bottom SiC (hotter) to the top SiC (colder). This is definitely not the case here since growth evidently occurs on the bottom surfaces of both B and D samples. Such results obviously raise an interrogation on the very existence of a vertical thermal gradient in this set up. However, the previously mentionned differences in morphology for both wafers of the same stack (see Fig. 2) suggest that these surfaces are not at the same temperature, though the resulting thermal gradient is probably too small to counterbalance the edge-to-centre mass transport. The latter phenomenon could originate from convection rolls generated by the intense magnetic field coming from the RF heating [8,9]. Such rolls would transport C more efficiently than the thermal gradient would do, as evidenced in liquid phase SiC growth experiments [10]. The butterfly pattern would then just reflect the forced convection scheme that happens within the liquid Si. The fact that the mass transport pattern is less pronounced for smaller liquid thickness is another hint towards the presence of these convection rolls, as they require a certain amount of liquid to form.

Considering the main purpose of this work which is to generate a well controlled step bunching for further MOS studies, it is important to keep in mind that the most wanted morphology (with wide and regular terraces) was exclusively spotted at the center of sample D, where some SiC growth occurred. This means that the SiC doping at the surface of these areas may have varied due to this growth, possibly being out of the targeted range for MOS. The doping level of these reconstructed surfaces has thus to be verified before considering a broader development of the presented process. Finally, if less parallel macrosteps are deemed suitable enough for MOS fabrication, a structured top SiC wafer resulting from an interaction with 30 µm liquid thickness could then be a good compromise since it exhibits an apparently growth-free and homogeneous step-bunched surface.

Summary

A sandwich configuration-based process for macrosteps design on large areas 4H-SiC(0001) 4° off surfaces has been studied. Despite the homogeneous spreading of the liquid Si and the demonstration of such structuring, uncontrolled mass transport occurs within the liquid, arguably caused by convection rolls. Further study is needed for pursuing the obtention of a regular macrostepped morphology while avoiding SiC growth.

Acknowledgement

This work has been financially supported by French ANR in the framework of the 19-CE24-0007 "Risemos" project.

References

[1] A. Chatterjee, A. Bhat, K. Matocha, Investigation of electrically active defects of silicon carbide using atomistic scale modeling and simulation, Phys. B Condens. Matter, 401–402, (2007), 81–84

[2] J. Woerle, B. C. Johnson, C. Bongiorno, K. Yamasue, G. Ferro, D. Dutta, T. A. Jung, H. Sigg, Y. Cho, U. Grossner and M. Camarda, Two-dimensional defect mapping of the SiO2/4H−SiC interface, Phys. Rev. Mater., 3, 8, (2019), 084602

[3] T. Kimoto, Z. Y. Chen, S. Tamura, S. I. Nakamura, N. Onojima and H. Matsunami, Surface morphological structures of 4H-, 6H- and 15R-SiC (0001) epitaxial layers grown by chemical vapor deposition, Jpn. J. Appl. Phys., 40, 5R, (2001), 3315–3319

[4] P. Fiorenza, F. Iucolano, G. Nicotra, C. Bongiorno, I. Deretzis, A. La Magna, F. Giannazzo, M. Saggio, C. Spinella, F. Roccaforte, Electron trapping at SiO_2/4H-SiC interface probed by transient capacitance measurements and atomic resolution chemical analysis, Nanotechnology 29 (2018) 395702

[5] M. Camarda, J. Woerle, V. Souliere, G. Ferro, H. Sigg, U. Grossner and J. Gobrecht, Analysis of 4H-SiC MOS Capacitors on macro-stepped surfaces, Mater. Sci. Forum, 897, (2017), 107–110

[6] D. Chaussende, L. Parent-Bert, Y. J. Shin, T. Ouisse and T. Yoshikawa, Effect of aluminum during the high temperature solution growth of Si-face 4H-SiC, Mater. Sci. Forum, 858, (2016), 37–40

[7] V. Soulière, D. Carole, M. Camarda, J. Woerle, U. Grossner, O. Dezellus and G. Ferro, 4H-SiC(0001) surface faceting during interaction with liquid Si, Mater. Sci. Forum, 858, (2016), 163–166

[8] U. Burr and U. Müller, Rayleigh-Bénard convection in liquid metal layers under the influence of a horizontal magnetic field, J. Fluid Mech., 453, (2002), 345–369

[9] Y. Tasaka, T. Yanagisawa, K. Fujita, T. Miyagoshi and A. Sakuraba, 2D oscillation of convection roll in a finite liquid metal layer under a horizontal magnetic field, J. Fluid Mech., 911, (2021), 1–24

[10] F. Mercier, J.-M. Dedulle, D. Chaussende and M. Pons, Coupled heat transfer and fluid dynamics modeling of high-temperature SiC solution growth, J. Crystal Growth 312 (2010) 155–163