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Interfacial Dislocation Reduction by Optimizing Process Condition in SiC Epitaxy

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Abstract. Interfacial Dislocation (ID) in SiC epitaxy was investigated. It is known that generation of interfacial dislocation on SiC epitaxy depends mainly on misfit strain between substrate and the epilayer. In this paper we investigate the impact of temperature profile, doping profile of the epilayer and resistivity of the substrates on the formation of interfacial dislocation in epilayers. Our preliminary results show that thermal profile during the epitaxy plays a key role in formation of interfacial dislocation in epilayers. We demonstrated reduction or elimination of interfacial dislocation in epilayers by optimizing the temperature profile of the substrates during the epitaxial growth.

Introduction

Silicon carbide is a material of choice for high power electronics due to its superior electronic and thermal properties [1]. However, reduction of defects in SiC epitaxy is challanging for reliable device performance. Defects can adversly impact the device performance by increasing leakage current, forward voltage degradation, higher on resistance etc. Among various defects, basal plane dislocation (BPD) is particularly detrimental due to its unpredictable forward voltage degradation under stress [2]. Hence, reduction in BPD is desired to achieve improved device reliability. While most of the BPDs in epitaxy are due to the propagation of BPDs from the substrate to epilayer, BPD can also be generated in epitaxy during the formation of interfacial dislocation (ID) since interfacial dislocations are accompanied by a pair of BPDs (Fig. 1). The BPDs in interfacial dislocations are shown after KOH etching in Fig. 1a. and in PL images in Fig. 1b. Interfacial dislocations are generated when their critical thickness are exceeded [3]. Hence, in order to reduce in grown BPDs, it is essential to reduce or eliminate interfacial dislocation, especially for thicker epilayers. In this paper we investigate the influence of doping concentration, temperature profile, and we optimize the process to reduce or eliminate ID in epilayers. Our preliminary results suggest temperature profile plays a dominant role for the formation of ID during the epitaxial growth.

Experimental

Commercial grade CVD reactor was used to grow epitaxial layers with a thickness of 12.5µm. 4H substrates (150mm diameters). Reactor pressure and temperature were kept fixed with a fixed doping concertation of 1 x 10^{16} (N-type) and a C/Si ratio of ~1. Epitaxial growths were performed at ~1600°C, with a fixed growth rate and for a film thickness of 12.5 µm. A buffer layer of a thickness of 1µm and a doping of 1 x 10^{18} was used for these epilayers.

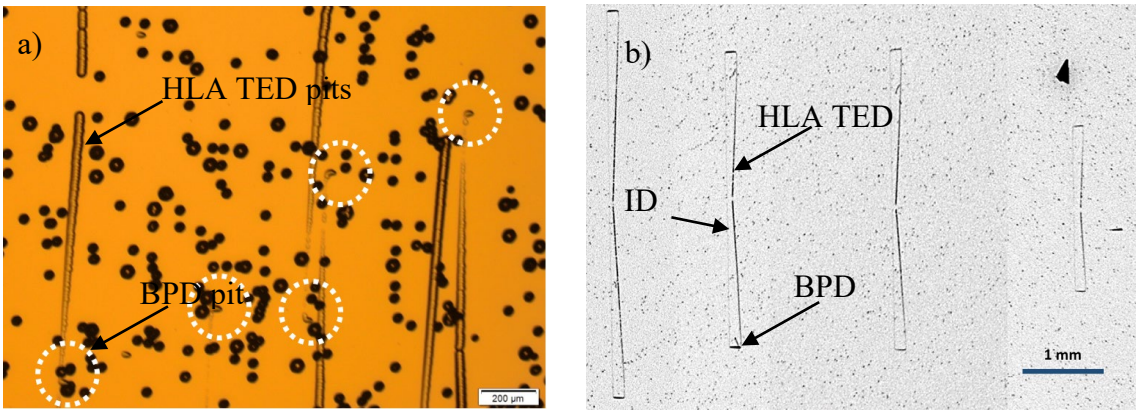

Fig. 1: a) Half loop areays of TEDs are shown after KOH etching. Apair of BPDs shown in dotted circles seen after KOH etching b) PL image of the interfacial dislocation is shown for an epilayer. BPDs in PL images are seen as dark horizontal lines at the top and bottom of the interfacial dislcoations.

Temperature profile over the wafer region was varied by changing the geometry of the graphite parts. Simulation was performed to determine the temperature profile using a commercially available software. Candela CS920 PL imaging was employed to detect and count defects in the epilayer, and KOH etching was performed to decorate the defects. For these epilayers, we visually count the number of interfacial dislocations from the PL imaging as shown in Fig 1(b)

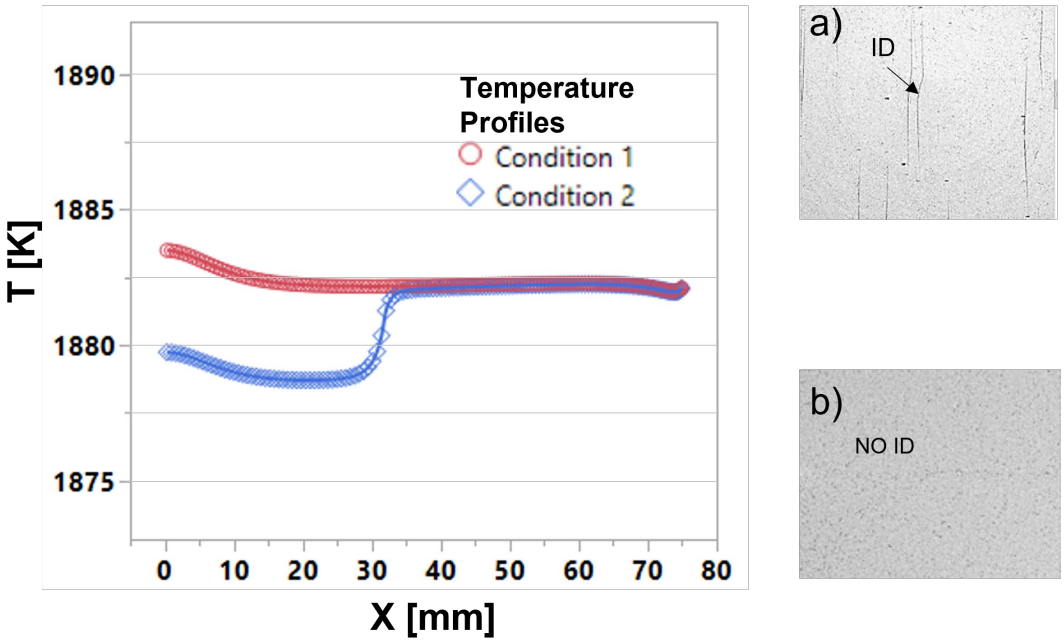

Fig. 2: a) Temperature profile with higher temperature at the center of the wafer generates higher interfacial dislocation (a) and temperature profile with lower temperature at the center generates lower interfacial dislocation (b).

Discussion

To study the effect of temperature profile, we grew epitaxy with both bowl shape and dome shape temperature profiles. In the dome shape temperature profile, the center temperature is higher than the edge (Fig. 2, condition 1). On the other hand, center is lower than edge for bowl shape temperature profile (Fig. 2, condition 2). When epitaxy was grown with a dome shape temperature condition, we observed high number interfacial dislocations in the center of the epilayers. However, if epilayer was grown using a bowl shape temperature profile, we see a much lower density of interfacial dislocation in the epilayer than that of in a dome shape temperature profile (Fig. 3). This

can be explained by misfit stress created by thermal strain [3-5]. We believe that misfit strain is higher when temperature on the center of the wafer is higher than the edge of the wafer. On the other hand, misfit related strain was lowered by optimizing the temperature profile. We believe, with the optimization, the temperature profile is flattened compared to the non- optimized condition.

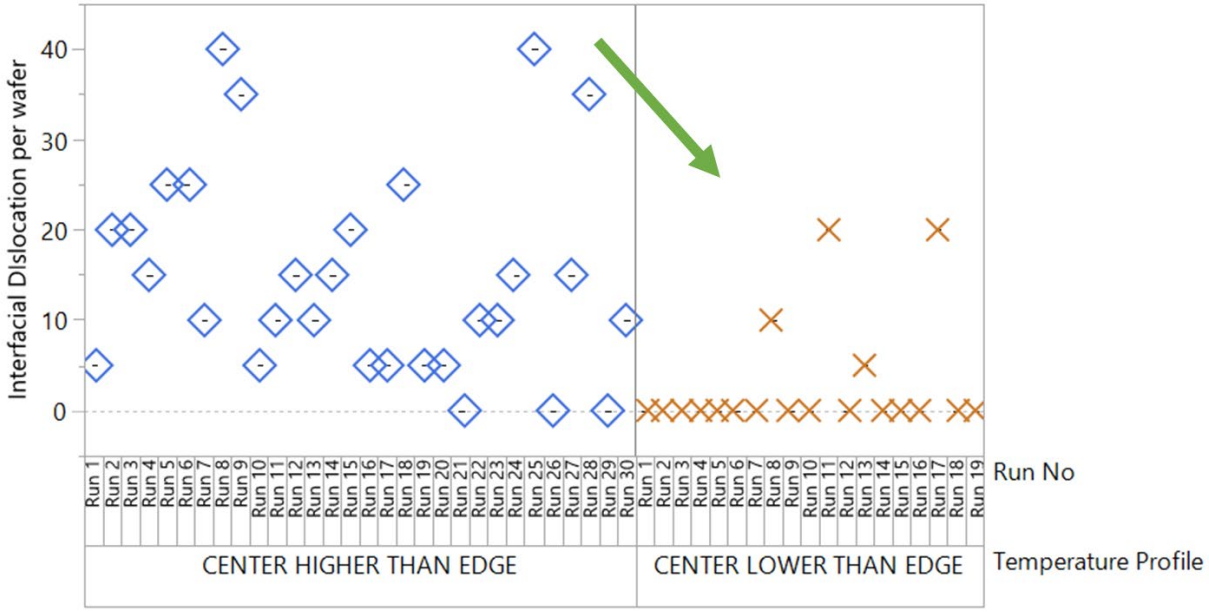

Fig. 3: Variability plot to compare interfacaial dislocaiton for two different temperature profiles. Higher number of interfacial dislocaiton is seen when center temperature is higher than the temperature at the edge. Interfacial dislocaiton was reduced significantly with optimizaiton of temperature profile.

Misfit strain can also be created by doping mismatch between substrate and epilayer, as lattice distortion can occur due to doping mismatch [3]. To investigate the impact of doping mismatch, we compared resistivity profile of bare wafers, and doping profile of the epilayers with higher and lower interfacial dislocation (Fig. 4) conditions. We divded wafers into two groups. Group including wafers with 0 interfacial dislocation was named as "good" and group including wafers with interfacial dislocation >=10 was named as "bad" (Fig. 4). For our case, doping profile of epilayers with low interfacial dislocation were comparable to the doping profiles of epilayers with higher interfacial dislocation (Fig. 4a). Doping profiles of the buffer layers were also comparable for these epilayers. Typical edge and center doping concentration is shown in Fig. 4b for these epilayers. Similarly, we compared the doping profile of the substrates used for these epilayers. We do not observe any clear correlation for doping profile of the wafers to the generation of interfacial dislocation. Doping profiles of the wafers with low interfacial dislocations were comparable to the doping profile of the wafers with higher interfacial dislocations in the epilayers. These results indicates that the doping concentration related misfit may not have as strong impact as thermal misfit to generate ID during the epitaxy.

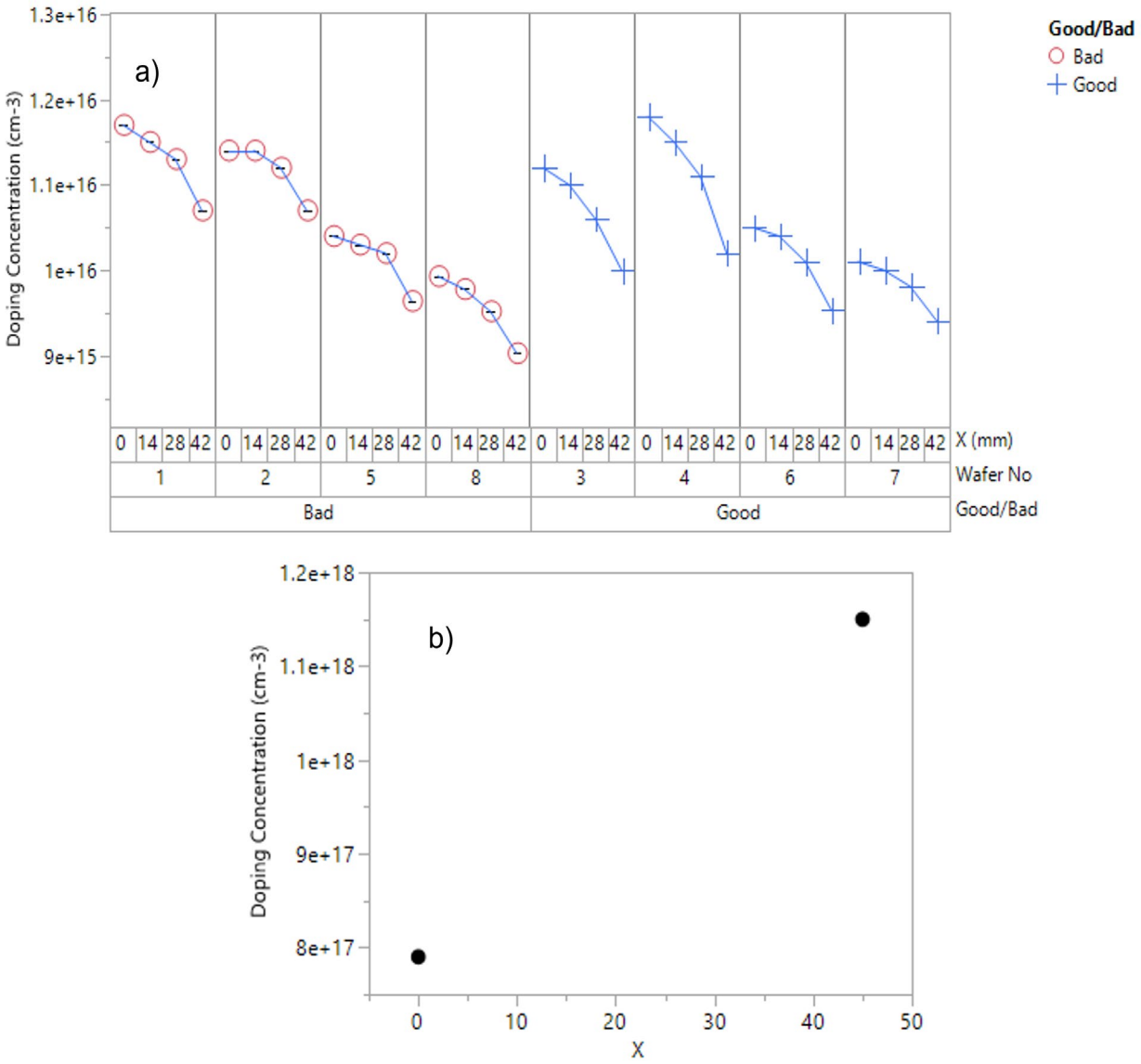

Fig. 4: Radial profile was compared for various values for good vs bad wafers for ID. No correlation was seen. a) radial profile of doping concentration of the epilayers b) typical buffer layer profile shown for a wafer.

Sammary

We conducted study the impact of temperature, doping concentration and substrate resistivty on the formation of interfacial dislocation in SiC epitaxy. Our results show that temperature profile plays a key role in generating interfacial dislocation, whereas doping profile did not show a good correlation in generating the interfacial dislocation.

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