Materials Science Forum
ISSN: 1662-9752, Vol. 1089, pp 15-22
doi:10.4028/p-i2s1cm

Submitted: 2022-08-30
Revised: 2022-11-18
Accepted: 2022-11-25
Online: 2023-05-26

Evaluation of Hysteresis Response in Achiral Edges of Graphene Nanoribbons on Semi-Insulating SiC

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Keywords: epitaxial graphene, graphene nanoribbons, field effect transistor, charge trapping, hysteresis.

Abstract. Hysteresis response of epitaxially grown graphene nanoribbons devices on semi-insulating 4H-SiC in the armchair and zigzag directions is evaluated and studied. The influence of the orientation of fabrication and dimensions of graphene nanoribbons on the hysteresis effect reveals the metallic and semiconducting nature graphene nanoribbons. The hysteresis response of armchair based graphene nanoribbon side gate and top gated devices implies the influence of gate field electric strength and the contribution of surface traps, adsorbents, and initial defects on graphene as the primary sources of hysteresis. Additionally, passivation with AlO_x and top gate modulation decreased the hysteresis and improved the current-voltage characteristics.

Introduction

Graphene has been widely discussed and gained significant attention in recent decades owing to its unique fundamental low-dimensional physical properties and potential applications [1, 2]. Nonetheless, the existence of the Dirac point, directed to a zero bandgap semiconductor [2], limits its integration into advanced digital electronic applications. However, it has been predicted to exhibit band gaps if the large area of graphene is constrained into a quasi-one-dimensional structure in sub-nanometer dimensions, making graphene suitable for many field-effect transistor applications at room temperature [3]. Many researchers stem from this significant property of graphene and are motivated to work on small constrictions like graphene nanoribbons (GNRs). In past decades these systems have been investigated at various levels of aspects. According to the studies, the properties of these systems can be tuned to form semiconductors to spin-polarized half metals [4, 5]. Generally, graphene has five edge structures: zigzag, armchair, cove, gulf, and fjord [6]. In contrast to the zigzag-edged graphene structure, which typically exhibits spin-polarized edge states with energy levels close to Fermi level, most other graphene edges show semiconducting properties [4, 6, 7]. Moreover, several studies have tried to experimentally prove the semiconducting properties of GNRs with field-effect devices [8, 9]. Both theoretical and experimental models revealed that the bandgap tunability is dependable on the width of GNRs [2, 3, 9]. However, the GNRs possess rough edges and widths along their ribbon length, which can further alter the bandgap depending upon the edge configurations (thus upon the chirality and number of carbon atoms) and doping [10, 11].

Furthermore, the field-effect studies on GNR based FETs show a hysteresis behavior in the conductance, which varies with sweeping voltage and sweep rate in ambient conditions [12, 13]. However, the hysteretic current-voltage (I-V) characteristics are not beneficial for transistors and integrated circuits. In contrast, the conductance hysteresis in graphene-related two-dimensional materials devices has significant possibilities and excellent potential in nonvolatile memory-based devices. Hence, many researchers have investigated and proposed various mechanisms and factors involved in graphene's origin of hysteresis behavior. However, most of the critical sources of hysteresis are charge transfer or trapping effects, mainly due to absorbates, interface traps, and bulk dielectric traps [12, 14, 15]. Moreover, considering the possible applications, making a systematic study of the physical mechanisms involved in the hysteresis properties of GNRs is a prerequisite for further device development. Therefore, insight into these fundamental properties and functionalities of GNRs is essential for developing GNR-based memory devices. Consequently, this study proposes a systematic evaluation of the hysteresis response of graphene nanoribbon structures in epitaxial graphene on semi-insulating SiC. The hysteresis response of GNRs on the armchair and zigzag directions of epitaxial graphene and dependent factors like width, measurement conditions, etc., were evaluated and studied. Moreover, the hysteresis response of armchair based side and top gated GNR FET devices were evaluated.

Experimental

Graphene has been prepared epitaxially with an orientation on-axis (0001) Si-face on semi-insulating 4H-SiC substrates at substrate temperatures between 1800 and 1900°C by thermal decomposition in an argon ambient [16-18]. The samples have a dimension of 10 x 11 mm^2. Initially, the samples were cleaned and spin-coated at 4000 rpm with a high-resolution negative resist, hydrogen-silsesquioxane (HSQ) (XR-1541-4%) and immediately baked on a hot plate at 90°C for structuring and fabrication of GNRs. The final resist thickness was about 30 nm. The GNRs were fabricated on epitaxial graphene by electron beam lithography in Raith 150 equipment. For high-resolution patterning and fabrication of nanoribbon structures on graphene, the electron beam lithography exposure was carried out at an acceleration voltage of 20 kV and an aperture of 7 μm. Subsequently, the exposed samples were developed with a two-step process in a solution of 3:1 (DI: TMAH) and 9:1(DI: TMAH) for 1 min at room temperature. Then the samples were etched in oxygen for 30 s using an inductively coupled plasma etching technique. The resist was removed by buffered oxide etching (BOE) for 1 min and rinsed in DI for another 1 min. The developed methodology allows the fabrication of GNRs down to sub 10 nm resolutions [8, 19]. The patterning of electrodes was defined by a positive tone electron beam resist PMMA (AR-P 617). The drain and source electrodes were metalized by an electron beam evaporation (Ti=10 nm/Au= 80 nm). In side-gate GNR-FET devices, both channel and side gates are made on graphene itself. For the top gate fabrication, initially a thin layer of Al (8 nm) is deposited using e-electron beam evaporation and oxidized thereafter. The top electrodes were metalized by an electron beam evaporation (Pd=10 nm/Au= 80 nm). The morphology and evaluation of critical dimensions and etching step heights of structured GNRs were measured using scanning electron microscopy (SEM) and atomic force microscopy (AFM) which uses active microcantilevers. The fabricated devices were characterized using SEM and measured using a Keithley 4200 system under a nitrogen environment at ambient conditions.

Results and Discussions

A non-contact AFM image of the surface morphology and profile obtained from pristine epitaxial graphene grown on Si-face of semi-insulating 4H-SiC is depicted in Fig. 1. As illustrated in Fig. 1, graphene is provided with wide micro-step structures. These micro steps like terraces are formed during the graphitization on the surface of SiC. These structures are spread along the edges of SiC due to the step bunching process and often cause inhomogeneity in graphene layer thickness [20, 21].

Terraces formed on the surface of graphene have an average width of 1 µm and a step height of 5 to10 nm. Fig. 2a shows a typical SEM image of the fabricated lateral device. All fabricated lateral devices have a channel length of 1 µm. As shown in the SEM image (see Fig. 2a), Ti/Au contacts were deposited above the GNRs from a two-terminal lateral device. Fig. 2b shows the AFM image of the device's active area with the profile obtained from the channel region. Since the channel region covers the terrace edges, the GNRs formed in such parts of the sample surface has varied graphene thickness. These inhomogeneities in the graphene layer thickness in the terraces and step region further change the electronic transport properties and result in mobility and channel conductance alterations of the graphene channel [22].

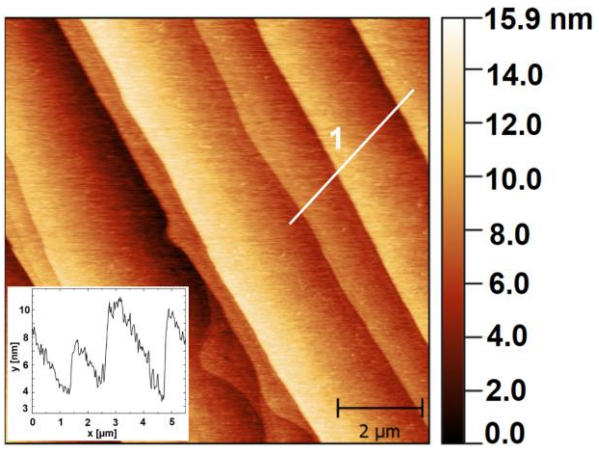

Fig. 1. Surface topography AFM images of epitaxial graphene on semi-insulating 4H-SiC and its respective height profile.

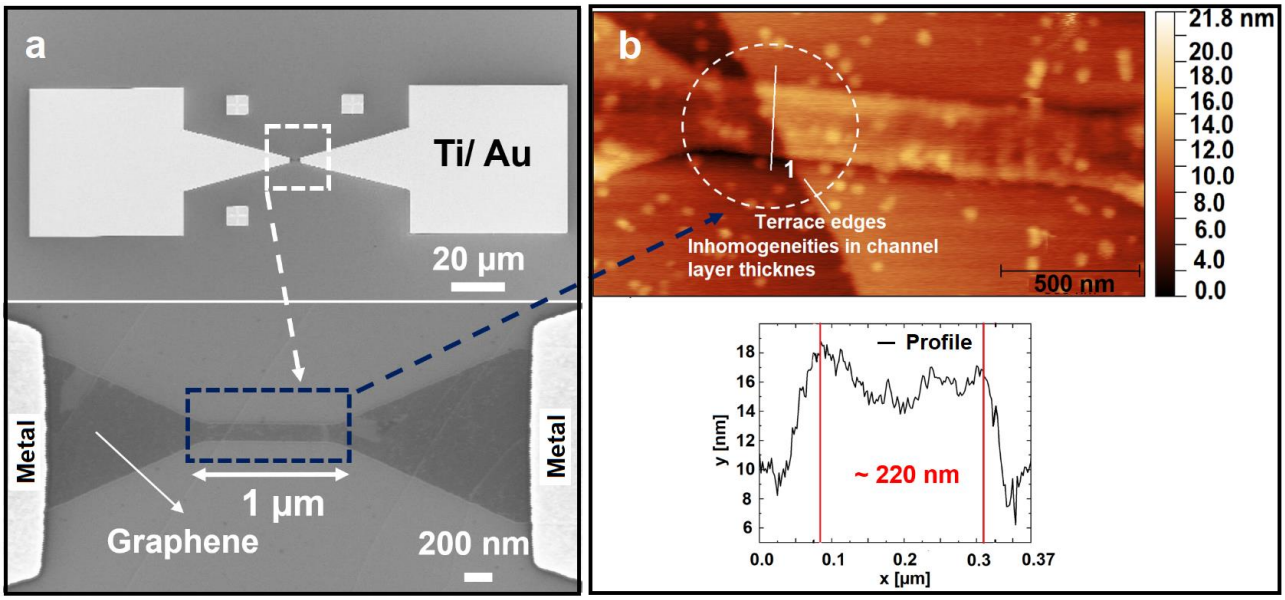

Fig. 2. SEM and AFM images of fabricated epitaxial GNR lateral device on semi-insulating 4H-SiC: (a) Single device overview of the lateral device, (b) AFM image of the channel region and height profile obtained across (white line 1) the channel.

Fig. 3a, 3b and 3c illustrates the AFM images of lateral devices with varying GNR widths, and their height profile obtained across the channel. The values obtained for the AFM profile channel dimensions nearly match the designed values. The channel region has an average step height of 4 to 5 nm. The developed technology could fabricate GNR with varying widths ranging from 20 to 250 nm. The fabricated devices were measured at ambient conditions under nitrogen flux. Fig. 4 (a) shows the DC hysteresis response obtained from a 20 nm GNR lateral device in the armchair direction, and the insets show the hysteresis response in the zigzag direction.

Furthermore, the hysteresis factor, the difference of the areas underneath the upper and lower branches of the hysteresis curves, was used here to quantify hysteresis using the Eq. 1 as follows:

$$Hysteresis\ area,\ H = \int_{V_{min}}^{V_{max}} I_d(V_d) dV_{d\,forward} - \int_{V_{min}}^{V_{max}} I_d(V_d) dV_{d\,backward} \quad (1)$$

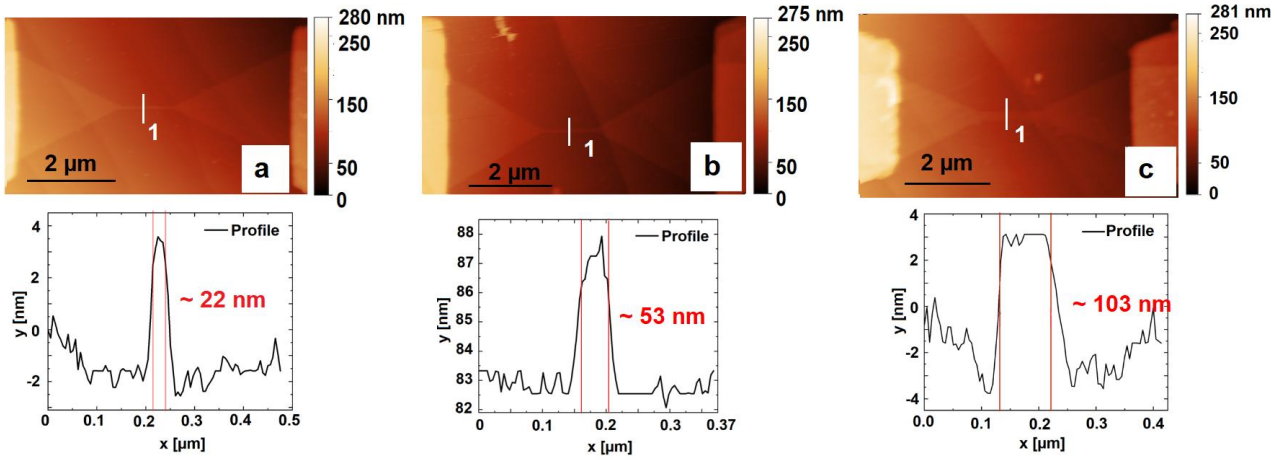

Fig. 3. AFM images of fabricated lateral devices with varying GNR widths. Lateral GNR devices with (a) 22, (b) 53 and (c) 103 nm constriction width and the profile obtained across (white line 1) of the channel region.

Fig. 4a illustrates the hysteresis obtained from both lateral devices on the armchair and zigzag directions. The drain to source voltage (U_{DS}) was applied by the voltage sweep from 0 V to 4 V, then from 4 V to -4 V, and back to 0 V. It is noted that the GNR in the armchair direction shows more pronounced hysteresis response with symmetric behaviour in both sweeping directions. In contrast, no significant hysteresis response of GNR devices in the zigzag direction was observed. Also, the area obtained for lateral devices in the zigzag direction is less when compared to the armchair (See Fig. 4a insets). This dependence in the hysteresis response might arise from the semiconducting and metallic nature of the armchair and zigzag edges of graphene nanoribbons, respectively [4, 5, 9]. Moreover, the hysteresis might be either attributed to the charge trapping and de-trapping into the surface or interface traps of the GNR device or the charge transfer from the absorbents like water molecules [12, 15].

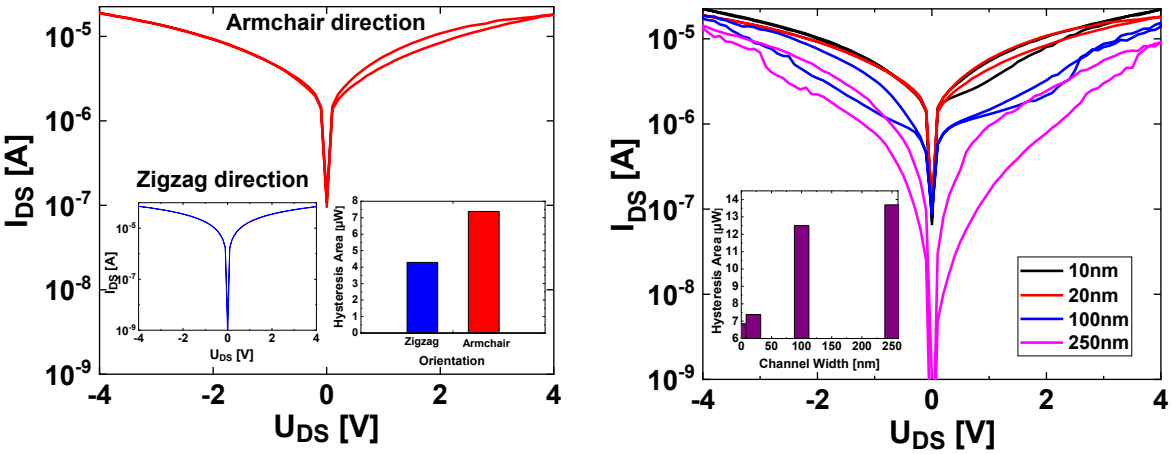

Fig. 4. (a) Hysteresis response of 20 nm GNR constriction in armchair direction (logarithmic scale) of epitaxial graphene, insets show the DC hysteresis response of GNR in zigzag direction (logarithmic scale) and hysteresis area obtained from lateral devices on both armchair and zigzag directions. (b) Hysteresis response of GNR in armchair direction with different strip widths, insets show corresponding hysteresis area obtained from the devices.

Furthermore, we have evaluated the hysteresis response dependence and the hysteresis factor on GNR strip width. Fig. 4b illustrates the dependence of the hysteresis response on the stripe width obtained from the GNRs in armchair direction for equal channel length. It is noted that with an increase in the strip width, we could observe a moderate increase of the hysteresis factor. This behaviour be attributed to an increase in the absolute value of traps with an increase in the surface

area of the channel [12, 15] when the trap density is assumed to be independent on the area. Moreover, due to the increase in the surface area, more additional terrace edges cover the channel region (See Fig. 2b), which further introduces more defect density in the channel [23]. These initial defect sites in the graphene channel promote the charge trapping process and may further influence the conductivity hysteresis of the GNR devices [23, 24].

We further evaluated the hysteresis response of the GNR channel by modulating the carrier density using a side gate. Similar methods of side gate engineering of graphene channels for graphene field-effect devices have already been reported and studied [25, 26]. Therefore, side gates could be an alternative to the top-gating scheme in graphene field effect transistors (GFETs) to modulate the graphene channel using a lower number of lithographic steps. However, this device type often experiences high leakage current caused by the current flow through the dielectric/air interface [27]. Fig. 5a and 5b illustrate SEM images of the general structure of side-gated armchair based GNR-FET. In these devices, graphene is used for both channel and side-gate. To understand the hysteresis behavior in these devices, measured in direct sweep conditions, (U_{DS} was varied from 0 V to 4 V, then from 4 V to -4 V and back to 0 V). The side gate voltage step was varied from 0 V up to 3 V with 1 V step.

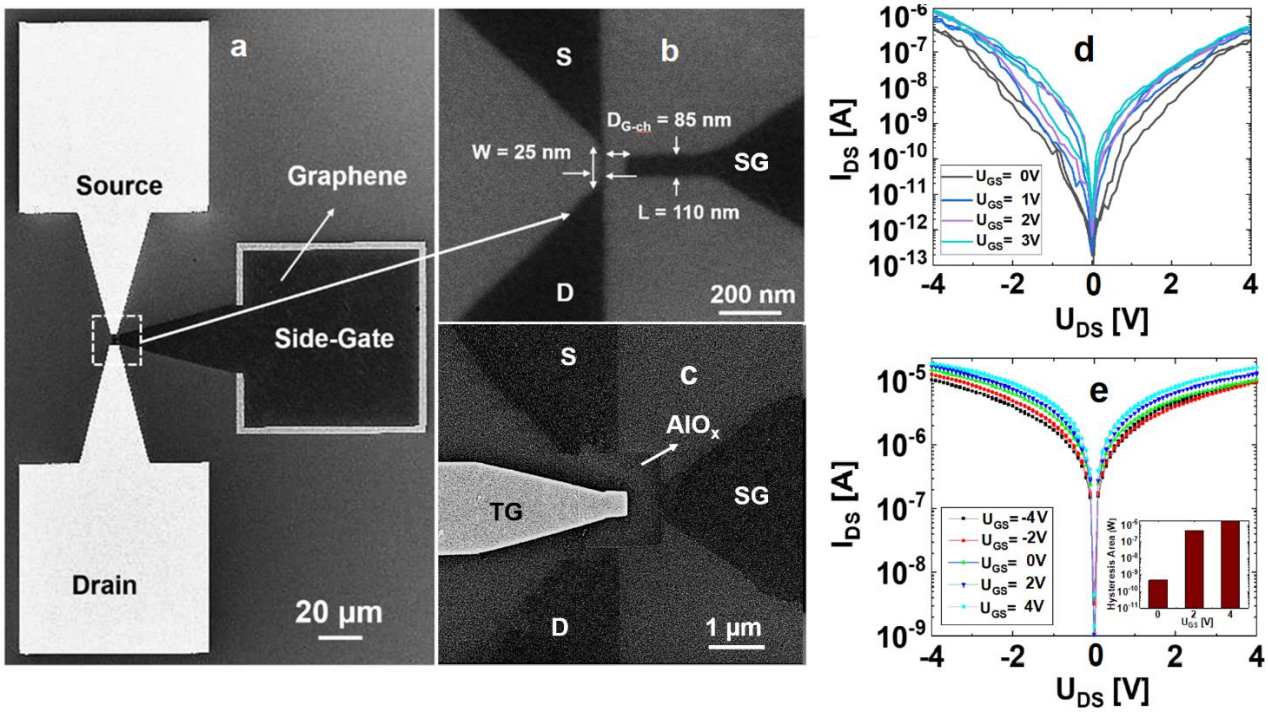

Fig. 5. (a and b) SEM image of single device overview of armchair based side gate GNR-FET. (c) SEM image of top gated GNR-FET. (d and e) Double sweep logarithmic scale output curve of GNR-FET under side gate and top gate modulation. Insets shows the dependency of hysteresis area upon different side gate to source (U_{GS}) voltage.

Typical output hysteresis response obtained from side gate GNR-FET is shown in Fig. 5d. The FET shows typical n-type behavior of graphene on SiC. In addition, it is noted that the U_{DS} sweep in GNR-FETs exhibits an increase in the hysteresis factor with increasing positive gate voltage. A similar behavior in GFETs has already been studied [12, 15]. These hysteresis responses possibly originate from the charge injection into the channel and side gate graphene substrate interface [14, 15]. Therefore, with the substantial influence of the side-gate voltage sweep, the hysteresis is triggered by a redistribution of charges at the interface and further causes charge transfer or trapping. As a second source of the conductivity hysteresis adsorbates and processing residues may act. The effect of the side gate-source voltage sweeping range (U_{GS}) and corresponding hysteresis area obtained from the GNR-FET is illustrated in Fig. 5e inset. Here, the U_{GS} voltage varies from 0 V to 3 V. A small hysteresis response was observed for U_{GS} at 0 V. However, a higher hysteresis response was observed when the U_{GS} increased. This behavior infers that the trapping of charges has increased

during the increase of side gate electric field strength sweeps which further contribute to the wider hysteresis.

We further investigated the effect of top gate modulation by passivating graphene channel with a high -k dielectric layer like AlO_x. The channel region is deposited with 20 nm of AlO_x. Subsequently, the top gate electrodes were deposited. Fig. 5b illustrates a SEM image of the top gated GNR-FET with 20 nm AlO_x. The devices were further measured with the side gate under ambient conditions. The U_{DS} voltage varied from 0 V to 4 V, then from 4 V to -4 V and back to 0 V. After each direct sweep measurement, the top gate voltage U_{GS} was increased by 2 V from -4 V to 4 V. Fig. 5e illustrates the hysteresis factor of the device under top gate modulation. It is noted that the current has been improved, and hysteresis response in the device was minimized with top gate modulation. This behavior further infers that deposition of a high-k dielectric material like AlO_x in the active device area of the GNR-FET modifies and passivates the contribution of hysteresis promoting sources like water molecules and other adsorbents [14, 28]. Moreover, it desorbs molecules from the surface of the graphene channel and retards the chemical reaction reducing the H_2O molecules at the interface of the channel [14, 29]. Another possible explanation for this behavior might be due to a limited supply of oxygen on the surface of the graphene channel, as it suppresses the surface reactions [28].

Summary

In conclusion, we have fabricated and evaluated the hysteresis response of GNR devices in both armchair and zigzag directions of epitaxial graphene on semi-insulating 4H-SiC. The difference of the area underneath the upper and lower branches of the hysteresis curves was used to quantify hysteresis. In addition, the influence of the orientation of fabrication of GNR in both armchair and zig directions and its dimensions on the hysteresis effect was examined and studied. Minimal hysteresis response in devices oriented in zigzag direction, possibly due to the metallic nature of the GNRs with zigzag edges was found. Moreover, the significant increase in the hysteresis factor with increasing channel width was observed stemming from an increase in the absolute value of traps with an increased surface area. Furthermore, the increase in the gate electric field strength substantially increases the hysteresis factor of armchair oriented GNR-FET devices. Additionally, passivation of the active device area with AlO_x as a high-k dielectric material and top gate device operation could reduce the defects, resulting in a lower hysteresis factor and enhancing the devices' current.

Acknowledgements

The authors acknowledge the financial support of this research by Carl Zeiss Foundation under contract P2018-01-002 and DAAD under grant 57435564.

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