

# Light Extraction from 4H Silicon Carbide by Nanostructuring the Surface with High Temperature Annealing

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**Abstract.** Nanostructuring of the surface occurs after annealing at high temperature of 4H-SiC samples. The surface morphology becomes needle-shaped like black silicon. The roughness of the surface also increases due to annealing and a slight etching of nanostructured zones occurs with an accentuated phenomenon at the boundaries. Electroluminescence is obtained by applied forward bias on fabricated PIN diode structures with localized nanostructured windows in surface. Light intensity seems to be more sensitive to the initial orientation of the substrate and less to the annealing temperature in the 1500°C-1700°C range.

## Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor with actual applications in power electronics and already commercialized SiC devices such as Schottky diodes and transistors (BJT, JFET, MOSFET). Due to its high thermal conductivity and stability, chemical inertness and high critical electrical field compared to other semi-conductor materials, SiC is ideal for applications in harsh environment. Because n and p-type doping of SiC are possible, multilayers devices with p/n junctions can be made [1]. However, SiC is also more and more studied today for its applications in optoelectronics and nanophotonics, becoming a strong competitor to conventional wavelength-conversion materials, such as phosphor/gallium nitride (GaN), for the fabrication of white light emitting sources (LED) [2]. Indeed, phosphor degrades quite fast with the time and is a rare-earth element which could lead to a strong increase of its price in the future [2]. In the case of fluorescent SiC (f-SiC), the material is co-doped with donor-acceptor pairs (DAP) like nitrogen – boron or nitrogen - aluminum, and presents a higher color rendering index and a longer lifetime compared to phosphor based GaN LED. Moreover, due to its high thermal stability, SiC needs little thermal management and it doesn't contain rare earth elements [3]. More recently, it has been shown that SiC can also emit near infrared (NIR) light due to the excitation of color centers such as silicon vacancies, divacancies and nitrogen-vacancy centers [4]. Comparing its different polytypes, cubic 3C-SiC seems particularly attractive for optoelectronic application due to its color emission center which better fits telecommunication wavelength [5].

However, one disadvantage of SiC for optoelectronic applications is its rather high refractive index (2.65 at 590 nm) compared to air. Due to that, the emitted light is totally reflected and stays trapped within the material which causes the low extraction efficiency of light of SiC [6]. To enhance the light extraction of SiC, nanostructuring of the material's surface has been done by various means such as e-beam lithography, nanosphere lithography, assembly of metal nanoparticles or reactive ion etching (RIE). The objective is to obtain an antireflection structure (ARS) array on the SiC surface [7]. However, these processes need time and several technological steps to be implemented and most of them are rather intended for local nanostructuring of the surface.

In this work, we look to improve the extraction of light in 4H-SiC by changing the nanostructure of the SiC surface with the help of high temperature annealing by controlling the sublimation of Si in surface. The objective is to increase the surface roughness of 4H-SiC in order to decrease the reflection of the emitted light within the material and to improve its transmission through the SiC

surface. This method could be used for fast nanostructuring of SiC surface on local zones or on large areas.

### Experimental Part

For this study commercialized 4H-SiC substrates are used with controlled doping epitaxial layers on Si surface for which the growth has been realized at Linköping University [8]. The samples have n-type 4H-SiC substrates. Three of them are grown 4° off-axis and one is grown on-axis. Except one off-axis substrate, the other samples have epitaxial layers. The structure of these samples is  $n^+/n^-/p^+/p^{++}$  (PIN diode structure). More information about the samples is given in the Table 1.

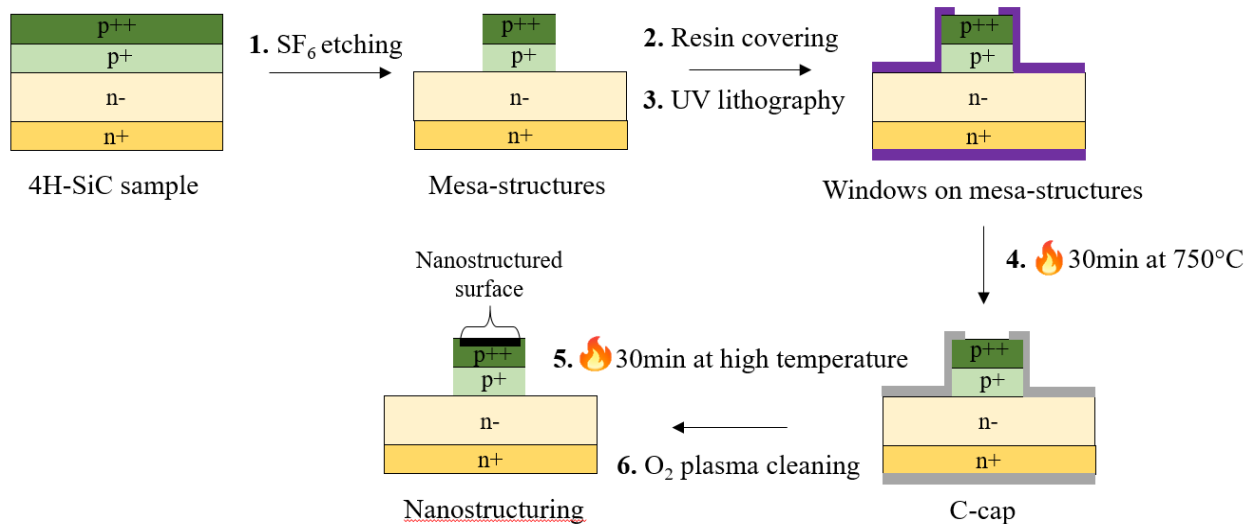
**Table 1.** Description of the samples used during this study.

	a	b	c	d
Orientation of the substrate	Off axis	On axis	Off axis	Off axis
Structure of the samples	n-type substrate	n-type substrate/ $n^+/n^-/p^+/p^{++}$		
Doping of the epitaxial layers [ $\text{cm}^{-3}$ ]	-	$3 \times 10^{18}/5 \times 10^{15}/1 \times 10^{18}/3 \times 10^{19}$		
Thickness of the epitaxial layers [ $\mu\text{m}$ ]	-	0.8/11/0.8/0.8	0.8/12/0.8/0.8	
Surface of the sample against the graphite susceptor in the AET/RTP furnace	Back (C-face)	Back (C-face)	Top (Si-face)	Back (C-face)

The objective of the study is to form PIN diodes with a nanostructured surface. To obtain electrically isolated PIN diodes on the 4H-SiC samples, fluorinated plasma etching is first used to etch the p-type epilayers and form p-type mesa-structures on the surface (Fig. 1). The patterned SiC substrates were etched using Inductively Coupled Plasma ICP – Reactive Ion Etching (ICP-RIE) Plassys MU400 reactor.

Nanostructuring of the surface of 4H-SiC occurs at high temperature annealing due to Si sublimation. However, we want to nanostructure only the surface of the p-type mesa-structures and to protect the rest of the samples surface. Therefore, the samples are covered by a thick layer of positive photoresist (AZ9260) and photolithography is performed with a mask to remove only the resin which is situated on the p-type mesa-structures surface. The patterned AZ9260 photoresist is first pyrolyzed at 750°C under Ar in a chamber (in quartz) of a dedicated AET furnace. This step leads to the formation of a protective graphite layer (C-cap) preventing Si sublimation on the surface of the samples [9]. High temperature annealing occurs then with a 30 minutes' plateau at a temperature of 1500, 1600 or 1700°C (Fig. 1). These high temperature annealings are performed under Ar in another chamber of the AET furnace provided with graphite resistors and susceptor. The geometry of this heating chamber has been designed to accomplish high temperature (up to 1900°C) rapid (2°C/s) temperature process (RTP) on SiC samples with a width up to 150 mm. The samples are disposed with their back face (C-face) against the graphite susceptor except one which has its front face (Si-face with mesa-structures in surface) against the susceptor (Table 1). Before each annealing, photolithography for C-cap patterning is performed, creating windows on a different zone of the sample.

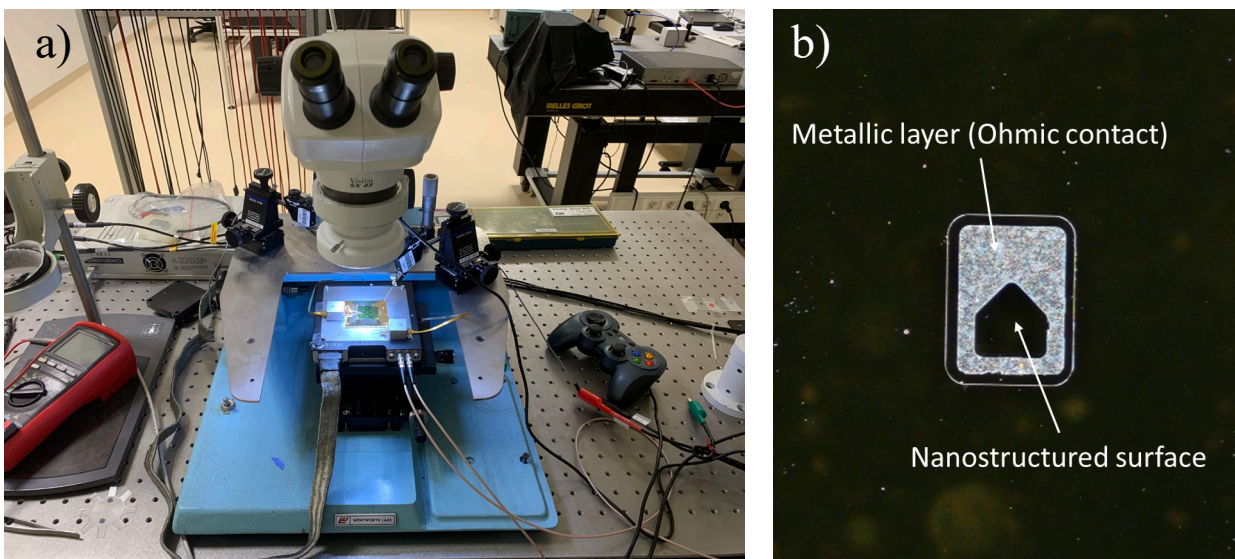
After SiC nanostructuring by high temperature in the created windows, the graphite cap formed by the AZ9260 photoresist is removed by oxygen plasma reactive ion etching (RIE) after each annealing. The samples are then cleaned with Piranha and diluted hydrofluoric solutions. Figure 1 shows a scheme of the process of the samples.



**Fig. 1.** Preparations of the SiC samples with a localized nanostructured surface by high temperature annealing.

After each annealing the surface of the samples have been analyzed by optical microscope Nikon Eclipse LV100, scanning electron microscopy (SEM) FEG SU8030 Hitachi and Bruker Dimension Icon AFM. The atomic force microscopy (AFM) measurements are performed with the Peak Force mode, with a scan rate of 0.702 Hz and a tip force of 700 pN. Roughness and height of etching are measured with the Nanoscope analysis software.

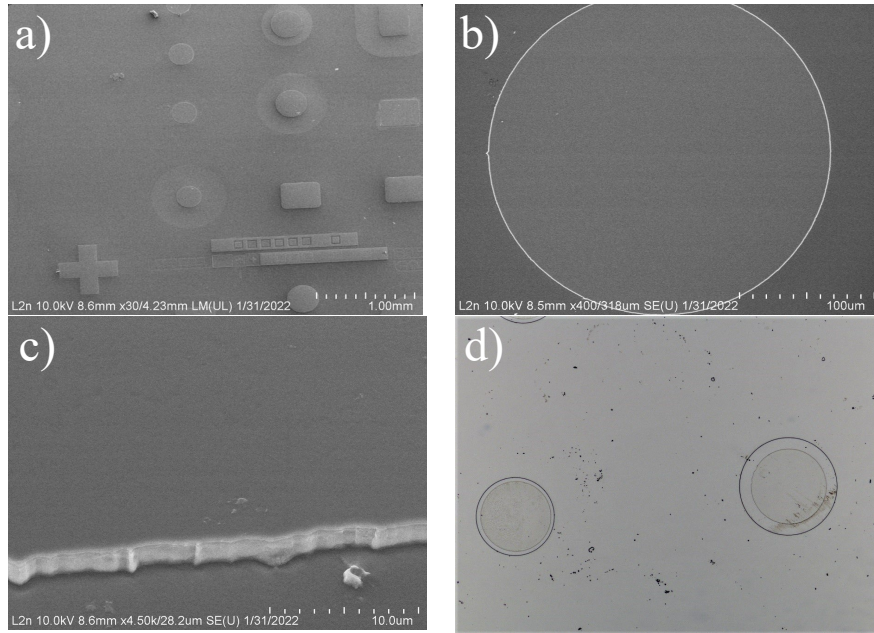
The electroluminescence of the PIN diodes is studied by two-point probe resistivity measurements with a bias of 8V applied on the mesa-structures. Figure 2.a shows a picture of the set-up. To obtain the ohmic contacts needed for the electrical measurements, metallic layers are realized by sputtered physical vapor deposition (PVD) on the back and front faces of the samples. On the substrate side of the samples, a 10nm titanium layer is first deposited followed by a 120nm nickel layer. On the front face of the samples, a metallic structure with Ni/Ti/Al/Ni layers is realized with respective thicknesses of 11/25/150/11nm. A lift off is then performed so only a part of the nanostructured mesa-structures is covered by the metal (Fig.2.b). Each deposition is done at low pressure, around  $5 \cdot 10^{-6}$  mbar. Annealing of the deposits is performed to create the ohmic contacts. The metallic layers on the back of the samples are annealed at 900°C and the ones on the front are annealed at 800°C.



**Fig. 2.** Set up of the two point probe measurements (a) and image under x50 microscope of a mesa with ohmic contacts.

## Results and Discussion

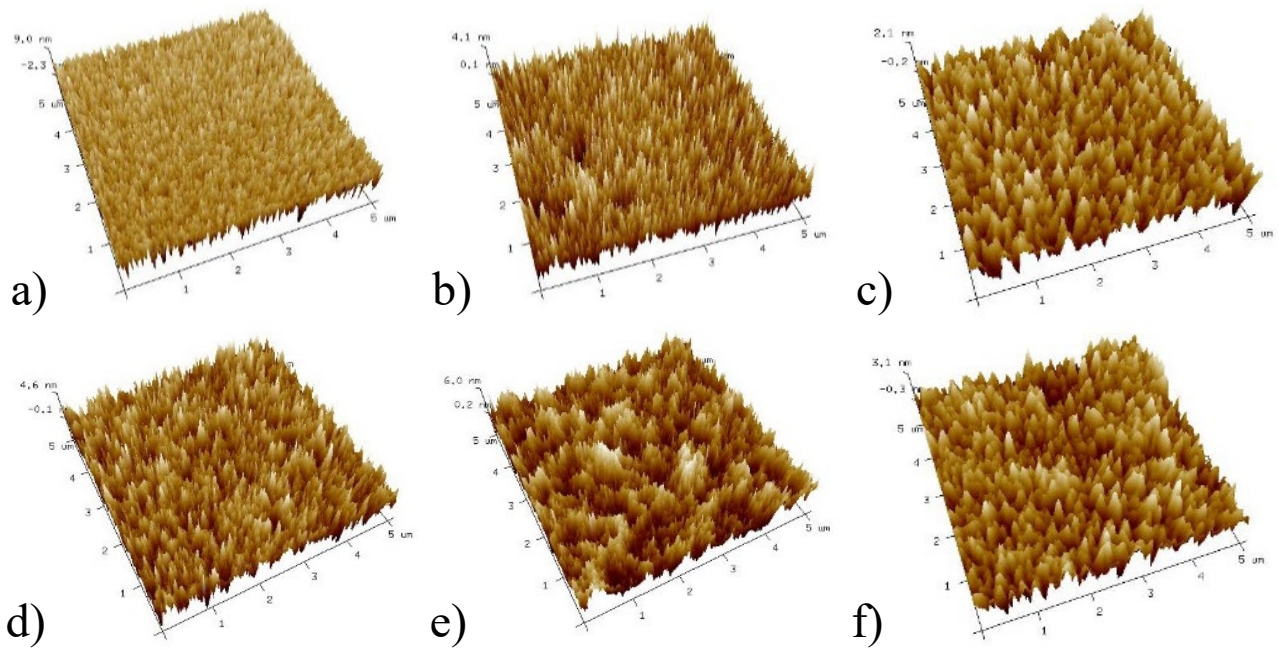
The SEM images obtained (Fig. 3) show the mesa-structures on the surface of a sample with a  $4^\circ$  off-axis substrate after annealing at  $1700^\circ\text{C}$ . However, it doesn't seem like there is a difference of structuration between the nanostructured mesas and the rest of the sample (smooth surface in both cases). An etching of the surface of the mesas is not seen either (Fig.2.b). However, with optical microscope observations on the same sample, a clear delimitation of the nanostructured surface in the center of the mesas is seen even at low magnification (x50). Therefore, a slight etch or surface morphology change seems to occur in the nanostructured zones but without an enough contrast to be observed under our scanning electron microscopy operation mode.



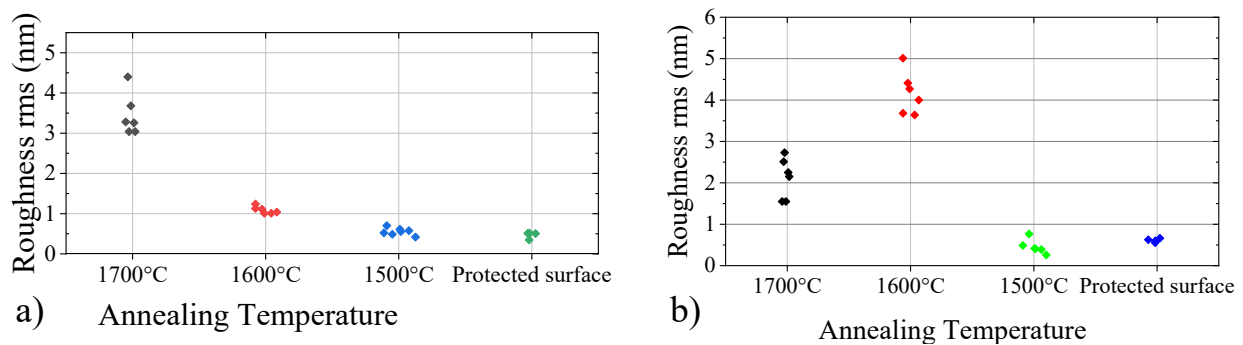
**Fig. 3.** SEM images of the sample d mesa-structures after annealing at  $1700^\circ\text{C}$  (a). Zoom on one mesa-structure is effected at normal incidence (b) and with a  $30^\circ$  tilt (c). Microscope image at x50 magnification of the d sample surface after annealing at  $1700^\circ\text{C}$  (d).

On the AFM images, a slight difference of surface morphology of the nanostructured part is seen depending on the temperature of annealing (Fig. 4). Indeed, after annealing at high temperature, the surface is needle-shaped. These needles seem to become larger when the temperature of annealing decreases and the needle-shape of the surface is more pronounced for the off-axis sample compared to the on-axis one. This surface morphology is due to the silicon sublimation (Si atoms are more volatile than C ones) which occurs during high temperature annealing (from  $\sim 1500^\circ\text{C}$ ), leading to the formation of carbonic layers (such as graphene) on the surface [10]. In this study, the carbonic layers are removed by  $\text{O}_2$  plasma RIE forming finally this needle-shaped structure similar to the surface aspect of black-silicon. This material has interesting optical properties due to its surface morphology, with very low reflectivity and high absorption of visible (and infrared) light [11]. Surface roughness of nanostructured mesas is also measured with AFM. Figure 5 shows that after annealing at  $1500^\circ\text{C}$ , the mean surface roughness (rms) of the nanostructured surface is similar to the one of the resin-covered zone during annealing. For samples with  $4^\circ$  off-axis substrate the surface roughness decreases with the temperature of annealing whereas for the sample with on-axis substrate the surface roughness is maximal after annealing at  $1600^\circ\text{C}$ .



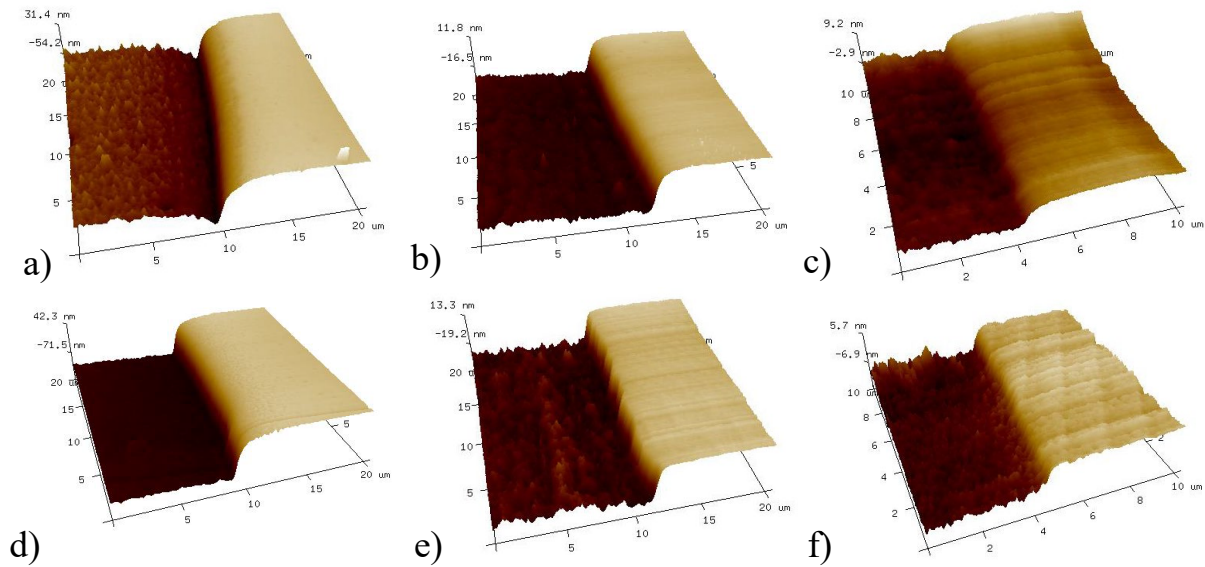


**Fig. 4.** Surface morphology of the nanostructured zones obtained after high temperature annealing at 1700, 1600 and 1500°C (from left to right) of 4° off-axis ((a) to (c)) and on-axis ((d) to (f)) 4H-SiC substrates with top epilayers.



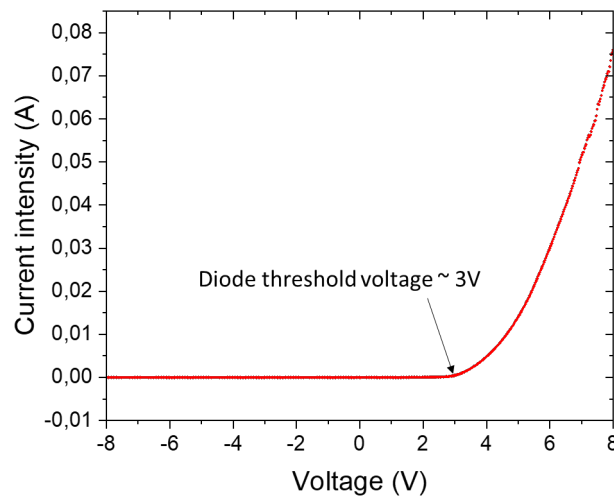
**Fig. 5.** Surface roughness (rms) of the nanostructured patterns after annealing at different temperatures (1500°C, 1600°C and 1700°C) and of the protected surface of 4° off-axis (a) and on-axis (b) 4H-SiC substrates with top epilayers. The protected surface is the surface covered by the pyrolysed resin during annealing.

Close to the limit of the nanostructured surface, a change of surface microstructure can also be observed as well as a light etching of the surface due to Si sublimation during annealing (Fig. 6). The etching depth tends to increase with the temperature of annealing. The surface is etched of around 10nm after annealing at 1500°C, around 35nm at 1600°C and around 80nm at 1700°C. When the temperature of annealing is too high (1700°C), the etching can also be strongly accentuated near from the limit of the opened windows for samples with 4° off-axis substrate.

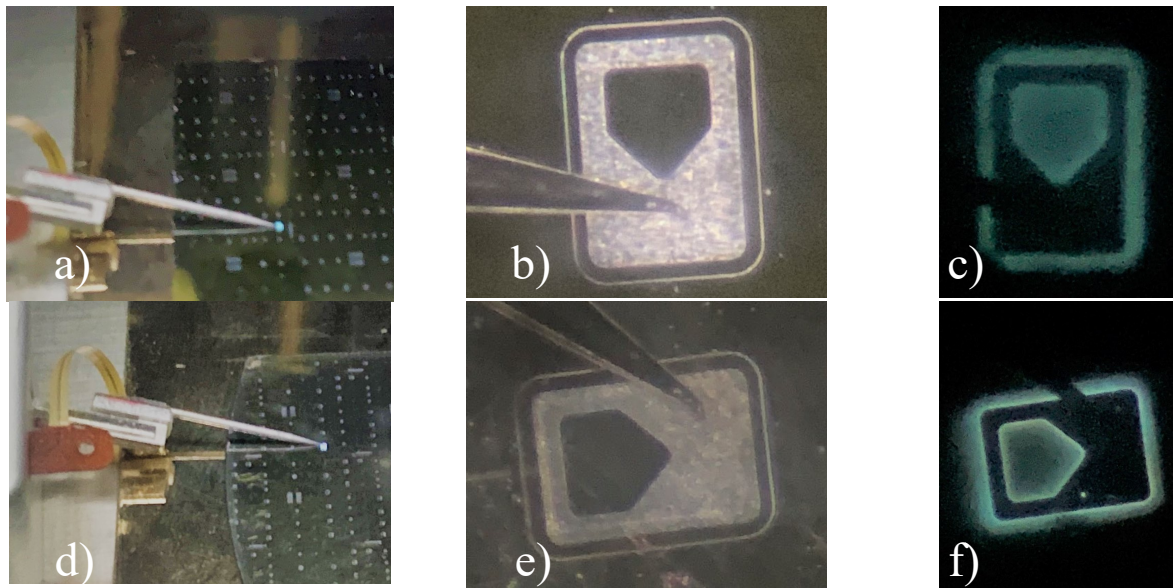


**Fig. 6.** AFM 3D profiles of 4° off-axis ((a) to (c)) and on-axis ((d) to (f)) surface, at the limit of the created etched nanostructured zone after annealing at 1700, 1600 and 1500°C (from left to right).

Electrical current measurements are also realized after metallization of the samples and formation of ohmic contacts on their back and front faces. A typical current-voltage characteristic of the formed diodes is presented in Figure 7. In forward bias the threshold is around 3V, it is also at this voltage that we begin to observe a luminescence of the samples. Under a forward bias of 8V, a blue light is seen on the surface of both oriented samples (Figure 8), with 4° off-axis and on-axis substrates. The observation under x20 binocular magnifier shows the electro-luminescence of a mesa annealed at 1600°C for both samples. The sample with off-axis substrate has a slightly more intense luminescence than the one with an on-axis substrate. The luminescence obtained confirms that the nanostructuration of the mesa surface allows a better extraction of light from 4H-SiC compared to a virgin smooth surface. However, a difference of luminescence depending on the temperature of annealing of the mesas is not visible by eye or binocular magnifier. The realization of spectral measurements is needed to complete our analysis of the samples and to find out if a slight intensity of light difference occurs when the annealed temperature of the mesas differs.



**Fig. 7.** I-V measurements of a p-n junction on a 4H-SiC off-axis substrate



**Fig. 8.** Electroluminescence measurements with two-point probe station of mesas for samples with off-axis ((a) to (c)) and on-axis ((d) to (f)) substrates. The observation of the mesas before ((b) and (e)) and after ((c) and (f)) forward bias application was realized with a x20 binocular magnifier.

### Summary

After annealing of the 4H-SiC samples, the zones which are not encapsulated by the pyrolysed resin are nanostructured and present a needle-shape surface morphology for annealing at higher temperatures (1700 and 1600°C). This morphology is similar to the one of black silicon. The nanostructured zones are slightly etched with a depth of etching from 10nm to 80nm depending on the temperature of annealing. Their surface roughness also increases with the temperature of annealing for samples with 4°-off-axis substrate whereas the surface roughness is maximal after annealing at 1600°C for the sample with an on-axis substrate. Therefore, to obtain a needle-shaped morphology of the surface and a higher roughness, it is better to use off-axis samples annealed at 1700°C. However, a stronger etching of the surface will occur at the edge of the created windows. Finally, two-point probe station measurements show an electro-luminescence of the mesas under a forward bias of 8V. Further analysis of this luminescence will be made in the future to determine if the luminescence varies depending on the temperature of annealing of the mesas.

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