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Controlled Macrostepping of Si-Face 4°off 4H-SiC over a Large Area via Liquid Si-Induced Reconstruction

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Abstract. The reconstruction of 4°off 4H-SiC surfaces was investigated using Si melting at 1550°C in a SiC/Si/SiC sandwich configuration. Despite systematically obtaining a macrostepped morphology over the entire areas in contact with the liquid Si, the steps were found wavy when using as-received 4H-SiC wafers. The regularity and straightness of the steps were significantly improved when the surface reconstruction was performed on processed surfaces: on re-polished surfaces the steps were found to be regular and straight in some cases, while this was constantly observed on as-grown epitaxial layers. After a reconstruction process of 2h, the best regularity of the steps was obtained with an average width of ~3-5 µm. Increasing the processed area from 1.44 to 4 cm^2 did not affect the results, which suggests good scalability of the process.

Introduction

While SiC MOSFETs are already being the most fostered switches to improve the efficiency in electric conversion systems, their full potential has not yet been reached. Indeed, high density of electrically active defects at the SiO_2/SiC interface drastically limits the channel mobility of these devices. Recent experimental studies suggest the localization of these defects at the step edges of the step-and-terrace morphology inherent to commonly used off-axially grown epitaxial surfaces [1]. By using few µm wide terraces, a decrease in the interface traps density of 10-15% on fabricated MOS capacitors was observed [2]. Such large terraces on 4° off 4H-SiC surfaces can be induced by the sole contact of SiC with liquid Si [3,4]. However, the sessile drop configuration used in these works does not allow the processing of surfaces > ~0.5 cm^2, hence this approach cannot be seriously considered as a device processing step. To solve this problem, a sandwich configuration allowing the processing of larger 4H-SiC areas is being investigated by the authors [5]. The preliminary results have shown a difficulty in obtaining regular and parallel macrosteps without uncontrolled mass transport inside the liquid. The present work reports significant improvements towards the development of this approach, regarding the obtained surface morphologies and homogeneity.

Experimental

The sandwich setup used in this work for liquid Si-induced surface structuring of 4H-SiC is schematized in Fig. 1. A piece of n-type Si wafer was melted between two 4H-SiC (0001) 4°off Si-face wafers from SK Siltron. Both Si faces of the top and bottom 4H-SiC wafers were thus in contact with the molten Si and underwent surface reconstruction. The top SiC wafer mainly had the role of homogeneously spreading the liquid by pressing and wetting. The lateral size of the bottom SiC wafer

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was larger than the top one (i.e. 2x2 cm^2 and 1.2x1.2 cm^2, respectively) to avoid any Si loss from the 4H-SiC wafers sides upon melting. The experiments were carried out inside an RF-heated vertical cold-wall chemical vapor deposition (CVD) reactor under 12 slm of H_2. The samples were heated with a ramp up rate of ~400°C/min up to 1550°C and kept at this temperature for 15-120 min. After the treatments, the samples were wet etched in concentrated HF/HNO_3 for removing the Si and thus separating both wafers. The reconstructed morphologies were then examined at different scales by SEM, AFM and optical microscopy. Regarding the latter technique, the entire reconstructed areas were characterized using Multiple Images Alignment (MIA) which involved the assembling of 20 to 40 images in each case.

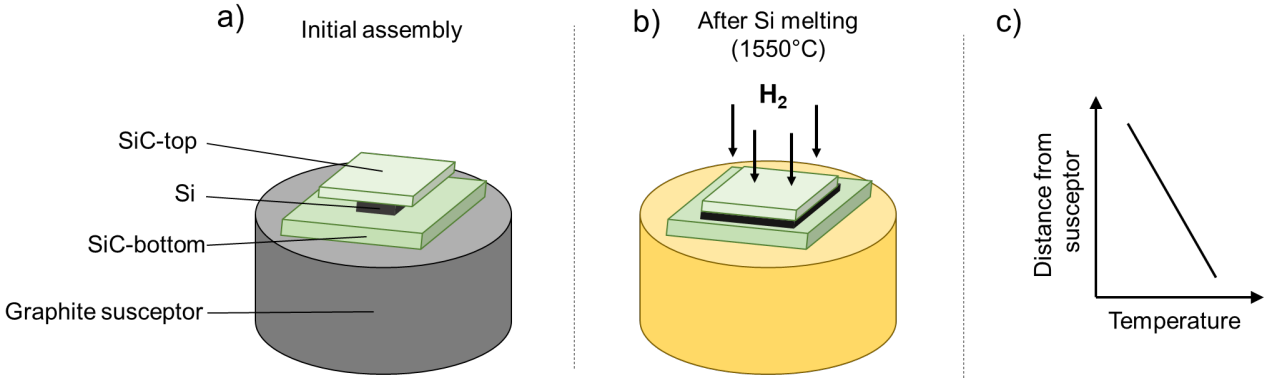

Figure 1. Schematic drawings of the investigated sandwich setup a) before and b) after Si melting; c) the presumed vertical thermal gradient inside the assembly using this configuration.

The amount (mass) of Si inside the sandwich was chosen as to form a film of ~30 µm thickness since this was found to be the best condition for controlling the mass transport inside the liquid and thus the homogeneity of the process (see ref [6,7] for calculation details). In these conditions, the natural vertical thermal gradient present within the stack generates a continuous carbon transport from the hotter bottom SiC wafer to the cooler top one: the bottom SiC is thus dissolved while the top SiC receives epitaxial deposition. Since the doping level of this epitaxial deposit on the top wafer is not controlled and since the control of the doping level at the MOS interface is essential, only the surface morphology of the bottom wafer, which was simply dissolved, will be considered. In this work, the use of different types of surfaces for the bottom SiC wafer is compared: as-received commercial n+ doped surface, re-polished surface (by Novasic company) and as-grown epitaxial surfaces (the epitaxial layers were grown in the same CVD reactor and using the conditions described in [8]).

Results and Discussion

Fig. 2 compares the morphology of the different surfaces, before (Fig. 2a) and after surface reconstruction (Fig. 2b) of the SiC-bottom wafer using the same experimental parameters (1550°C-2h). One can clearly see from the MIA that the steps are very parallel and continuously crossing the entire reconstructed area for both re-polished and epilayer surface cases. On the contrary, when using as-received wafers, no pattern is distinguishable from the MIA. When looking closer to the step morphology by AFM (inserts in Fig. 2b), step edges on the as-received wafer are wavy and intersect with each other, while they are much straighter and parallel in the two other cases. The same morphologies were observed by performing several AFM scans on different zones of each sample.

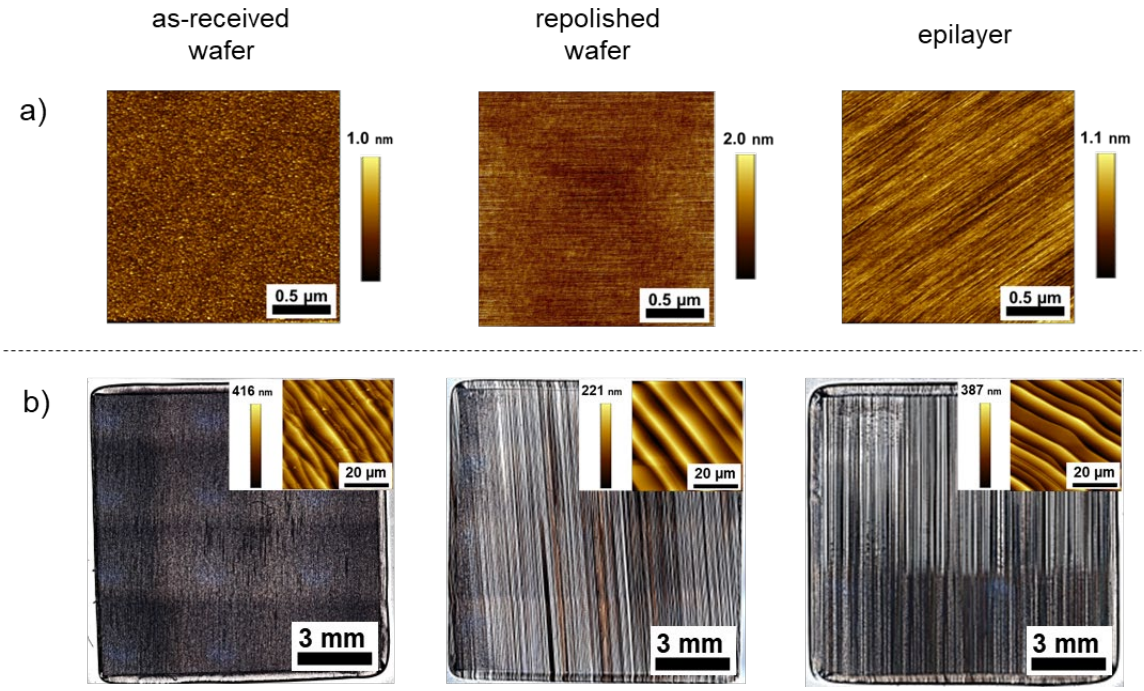

Figure 2. Morphology characterization of the different bottom SiC wafers of this study a) before Si interaction (AFM images, 2x2 µm scans), and b) after Si interaction for 2h at 1550°C (MIA of the reconstructed areas using optical microscopy with x25 objective). Inserts in b) show the corresponding AFM images (50x50 µm scans) obtained at the center of each reconstructed area.

The divergence in the obtained macrosteps reconstructions (using the same experimental conditions except for the type of surface) can thus be attributed to the initial morphology of these three different surfaces. As a matter of fact, the AFM images (Fig. 2a) of the epilayer and re-polished wafers both show an organized structure with microsteps at the nanometer scale though this structure is much fainter in the re-polished case. No specific microstructure is discernable in the case of the as-received wafer. Note that despite these morphological differences, these three starting surfaces display almost the same value of root mean square (RMS) roughness (~0.15 nm). These observations suggest that the Si-induced step-bunching mechanism may be strongly dependent on the initial surface morphology: disordered meandering of the step edges is obtained when the starting surface is undefined while a regular step and terrace structure is generated when starting from already formed microsteps.

Regarding the reproducibility of these results, it was experimentally observed that, whatever the liquid-Si interaction duration (up to 2h), using as-received wafers systematically led to step meandering, whereas only parallel macrosteps were observed when using epilayers. The case of the repolished wafers was less straightforward as only half of these samples presented parallel macrosteps without meandering after surface structuring. The other half was rather similar to the as-received wafer case with high meandering of the steps. These experimental occurrences are summarized in Table 1. It can be reasonably argued that the occurrence of parallel steps after surface structuring is linked to the presence of these steps before the structuring: a sharper initial step structure leads to straighter macrosteps after surface reconstruction. As seen from Fig. 2a, the step structure of the re-polished surfaces should be too faint to reproducibly generate the optimal step reconstruction after liquid Si interaction. We believe that a homogeneous and sharp microstepped surface is an essential prerequisite for obtaining a fully parallel and macrostepped reconstruction.

Table 1. Experimentally observed occurrences of parallel macrosteps on the SiC-bottom wafer using the sandwich Si-melting process on different initial surface types.

Starting surface	as-received wafer	repolished wafer	epilayer
Occurrence of parallel macrosteps	0%	50%	100%

Considering the better control of the macrostepping allowed with epilayers, the time dependency of the step-bunching mechanism was investigated using epilayers only as starting surface. At first glance, both the SEM images and the histograms of Fig. 3 suggest that increasing structuring time allows a reduction and homogenization of the mean step width. However, as shown in Fig. 4a, a closer inspection by AFM on the apparent large terraces (> 20 µm width) formed after 15 min of interaction shows that it is not smooth (unlike expected from a natural terrace) but composed of microsteps similar to the original morphology of the starting epilayer. Furthermore, the AFM cross-section profile (Fig. 4b) measured on such apparent large terraces does not follow the regular increase and decrease of the altitude expected in standard step bunching. Instead, the profile is flat when measured on these apparent large terraces, especially the larger ones. This is not observed in the case of the narrower (but more regular) steps formed after 2h of structuring, for which the cross-section profile corresponds to a standard step bunched morphology. It can thus be proposed that these large areas formed during short structuring time are in fact unreacted zones and thus cannot be considered as macrosteps. This leads us to suggest the structuring scenario illustrated in Fig. 5. Basically, it involves that the step bunching does not occur homogeneously over the entire surface but rather starts at specific step edges, by local dissolution of SiC into liquid Si. This dissolution continues laterally and along the basal plane. When the contact duration with liquid Si is increased, new dissolution starting points appear and propagate in the same manner.

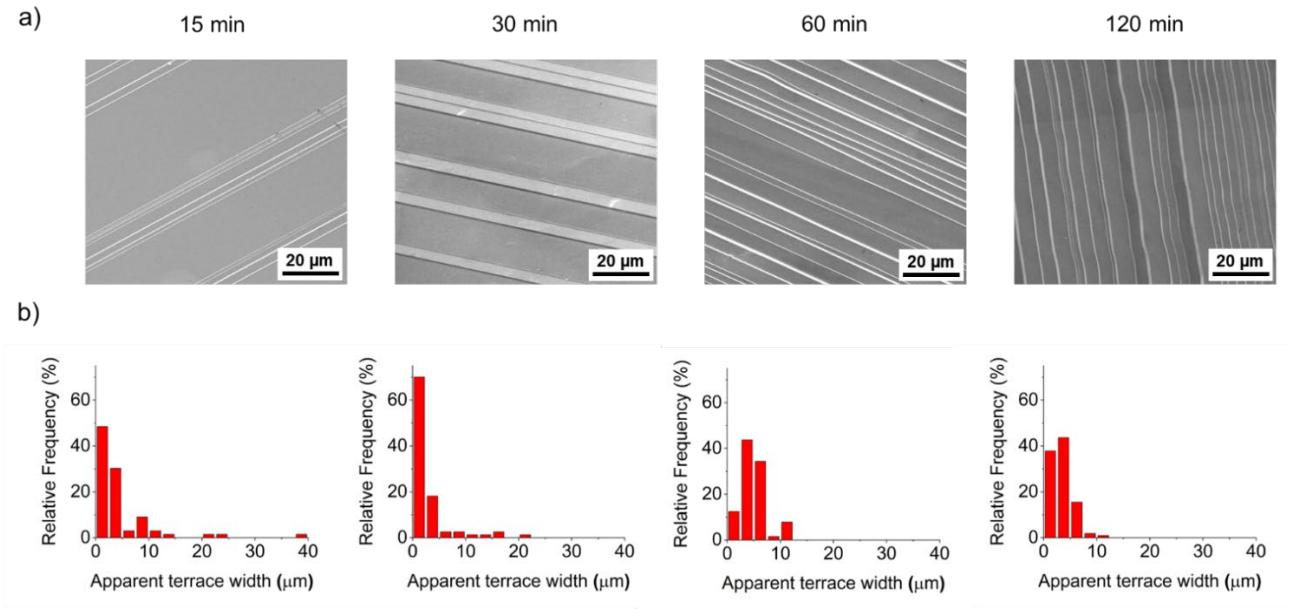

Figure 3. Effect of the structuring duration on a) the surface morphology as observed by SEM and b) the corresponding apparent step width distributions. These results were obtained using epilayer surfaces as bottom wafer of the stack.

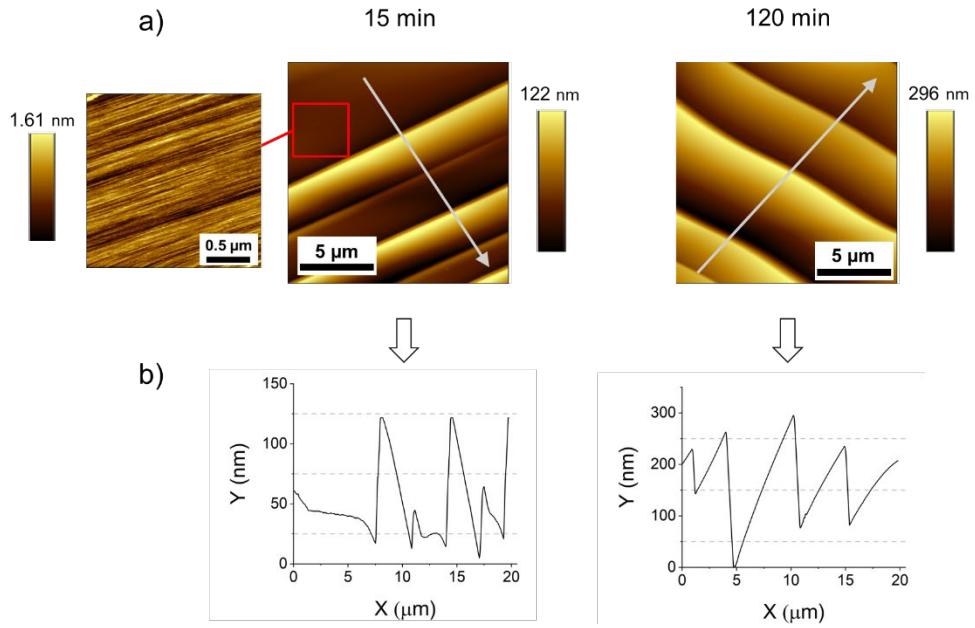

Figure 4. a) AFM images (15x15 µm scans, 2x2 µm scan on the left) of the surface morphology after 15 and 120 min of interaction with liquid Si and b) the corresponding cross section profiles along the grey arrows drawn in a).

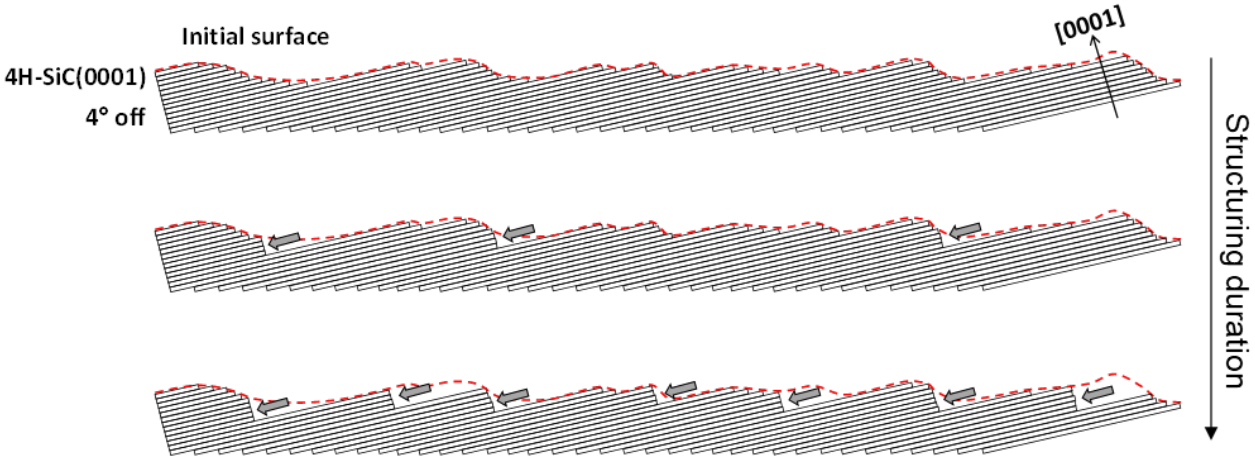

Figure 5. Schematic illustration of the proposed mechanism explaining the time dependence of the surface structuring evolution. The initial surface is drawn wavy to represent the microstepped structure of the starting epilayer.

Finally, as a first attempt to test the scalability of the sandwich set up studied here, the size of the 4H-SiC wafers was increased to 2x2 cm^2 and 2.5x2.5 cm^2 respectively for the SiC-top and -bottom wafers, which thus corresponds to a ~2.7 times increase of the reconstructed area. An epitaxial layer was grown on the SiC-bottom wafer beforehand. The results obtained using the same experimental conditions of surface structuring as previous (30 µm liquid Si thickness, 1550°C for 1h) are shown in Fig. 6. One can see that this size increase did not affect the Si wetting over the entire area fixed by the top-SiC wafer (Fig. 6a). The surface morphology, either observed by MIA or SEM (Fig. 6b), did not show significant difference with the previous sample elaborated with identical treatment time. These preliminary results did not evidence any difficulty in the scaling up of the sandwich set up towards higher dimensions. A transposition of the process to full 4-6 inches wafers would thus be an interesting perspective, though the author's experimental setup does not allow processing such dimensions.

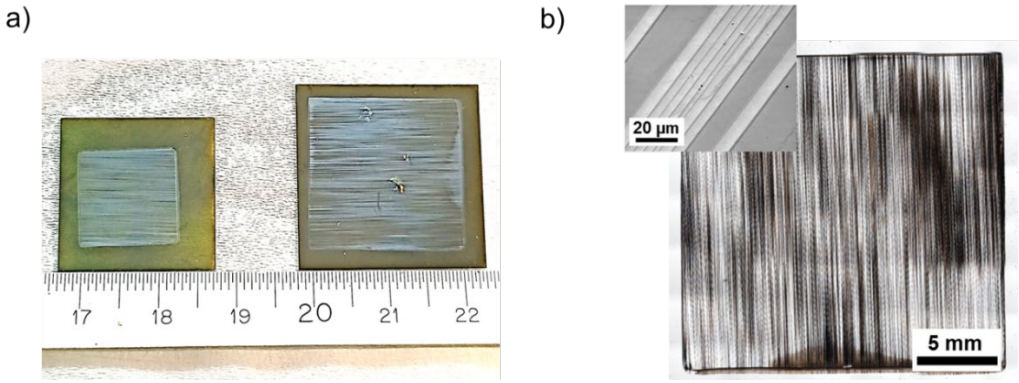

Figure 6. a) Photograph of processed SiC-bottom wafers (1550°C, 1h) with a reconstructed area of 1.2x1.2cm^2 (left) and 2x2cm^2 (right), and b) MIA of the 2x2cm^2 reconstructed area using optical microscopy (x25); in insert is a SEM image taken at the center of this area.

Summary

A process allowing the reproducible structuring of 4°off 4H-SiC surfaces into parallel macrosteps was successfully demonstrated. It involves the use of a SiC/Si/SiC sandwich set up with a 30 µm thick liquid Si interlayer and thermal treatment at 1550°C. The use of an as-grown epitaxial layer as starting surface was shown to be essential for reproducibility purpose. The obtained step bunched morphology was found to homogenize when increasing treatment time up to 2 h, leading to terraces width of ~3-5 µm. A first attempt at upscaling the setup size did not affect the results, which allows envisaging the processing of larger surfaces.

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