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Influence of Post-Ion-Implantation Annealing Temperature on the Characteristics of Gate Oxide on 4H Silicon Carbide

Li-Jung Lin[1 a] and Bing-Yue Tsui[2 b *]

[1]Master and Ph.D. Program for Science and Technology of Accelerator Light Source, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, R.O.C.

[2]Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, R.O.C.

[a] lin0851803.en08@nycu.edu.tw, [b *] bytsui@nycu.edu.tw

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Abstract. The effect of post-ion implantation annealing on the properties of the SiO_2/4H-SiC interface is examined in this paper. It is observed that the surface roughness degrades after the high-temperature Ar annealing, but the oxidation process after the high temperature annealing can improve the surface roughness. To better understand the effect of high-temperature annealing on the gate oxide, the reliability of gate oxide is further studied. The results show that although the surface roughness degrades after high-temperature annealing, the interface state density, tunneling barrier height, breakdown field, and critical electric field for the 10-year lifetime of the thermally grown gate oxide do not degrade.

Introduction

Silicon carbide (SiC) has been proved a suitable semiconductor material for high temperature and high voltage applications [1, 2]. Since high-temperature annealing (>1600 °C) is required to re-crystallize and activate dopants, all ion implantation and annealing processes must be performed before gate oxide formation [3]. Although carbon-cap can prevent Si from sublimation, the surface roughness may be degraded slightly [4]. In this work, we performed a thorough study on the influence of post-ion-implantation annealing (PIA) on the characteristics of gate oxide on 4H-SiC. Surface roughness, interface state density (D_{it}), time-zero dielectric breakdown (TZDB), and time-dependent dielectric breakdown (TDDB) are all investigated.

Experiments

Since the main SiC power MOSFET is n-channel MOSFET, the interface state near conduction band is the main factor affecting the performance of n-channel MOSFET. Therefore, n-type SiC wafer is used in this work and the interface state distribution is extracted by the high-low frequency method. Because the doping concentration of MOSFET is in the order of 10^{17} cm^{-3} in general, thus the doping type would not affect the surface roughness. Thus, it is believed that the results can be applied to the N-channel MOSFTE which is fabricated on p-type SiC.

The starting material was a nitrogen-doped 4° off-axis (0001) 4H-SiC substrate with a nitrogen-doped epi-layer. The thickness and doping concentration of the epi-layer are 5.5 μm and $1x10^{16}$ cm^{-3}, respectively. Samples experienced PIA in Ar ambient at 1600 ℃, 1650 ℃, and 1700 ℃ for 30 minutes with a carbon-cap. Sample without experiencing PIA was also prepared as reference. A 500-nm-thick oxide deposited by a PECVD system was used as field oxide (FOX). The circular device area was defined by typical photolithography and wet etching processes with a radius of 50 μm. Gate oxide was grown by wet oxidation at 1200 ℃ for 26 minutes followed by a 1200 ℃ NO annealing for 15 minutes. In-situ phosphorus doped poly-Si was deposited by a LPCVD system as gate material. After gate pattering, a 300-nm-thick Al was deposited and patterned to form probing pad. Fig. 1 shows the schematic cross-sectional structure of the MOS capacitor.

Atomic Force Microscope (AFM) was used to analyze the surface roughness of the samples. Interface state density was extracted by the high-low frequency method. TZDB and TDDB were evaluated by ramp voltage and contact voltage stress, respectively.

- RCA clean
- Carbon film
- Ar Annealing
  - Without
  - 1600 ℃
  - 1650 ℃
  - 1700 ℃
- Carbon film remove
- Field oxide deposition
- Lithography
- AA region formation (wet etching by BOE)
- Gate oxidation (1200℃ wet 26 min + 1200℃ NO 15 min)
- Poly-Si deposition
- Lithography
- Poly-Si etching (P5000E)
- Al deposition
- Lithography
- Al etching (wet etching)
- Backside etching (P5000E)
- Backside Al deposition
- Sintering (400 ℃,30min, N_2)

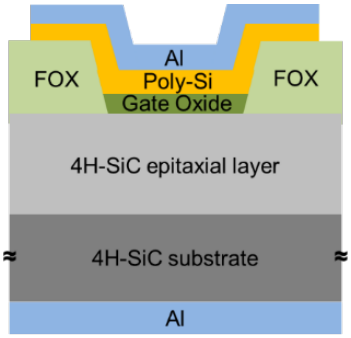


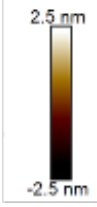
Fig. 1. Process flow and schematic cross-sectional structure of the MOS capacitor in this work.

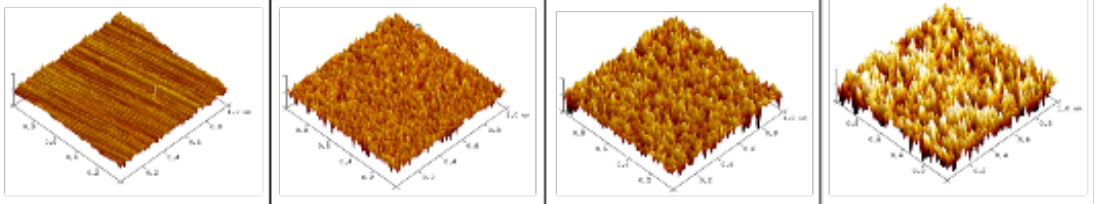
Results and Discussion

Fig. 2 shows the AFM images and the roughness average (R_a) values of the samples after removing the carbon-cap layer and after removing gate oxide. It is observed that higher PIA temperature results in larger R_a value. Gate oxidation can reduce the roughness but cannot fully recover it. Fig. 3 shows the energy distribution of the D_{it} of samples annealed at different temperatures. Although PIA degrades surface roughness, it does not affect the interface state density after NO passivation.

Fig. 4 shows the current-voltage (I-V) characteristics of all samples. The leakage current distributes tightly and the breakdown field (E_{BD}) of gate oxide grown on each sample is similar. The slight difference in E_{BD} has no PIA temperature dependence.

Process	Reference	PIA 1600 ℃	PIA 1650 ℃	PIA 1700 ℃
After removing C-cap	0.222 nm	0.263 nm	0.412 nm	0.764 nm
After removing gate oxide	0.138 nm	0.203 nm	0.299 nm	0.611 nm





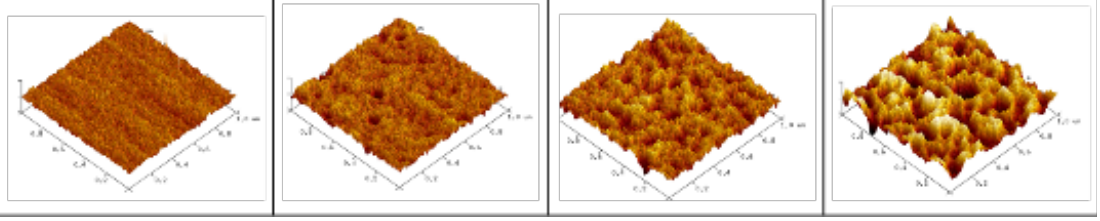


Fig. 2 Surface roughness (R_a) of the samples with different PIA temperatures after removing carbon-cap layer and after removing gate oxide.

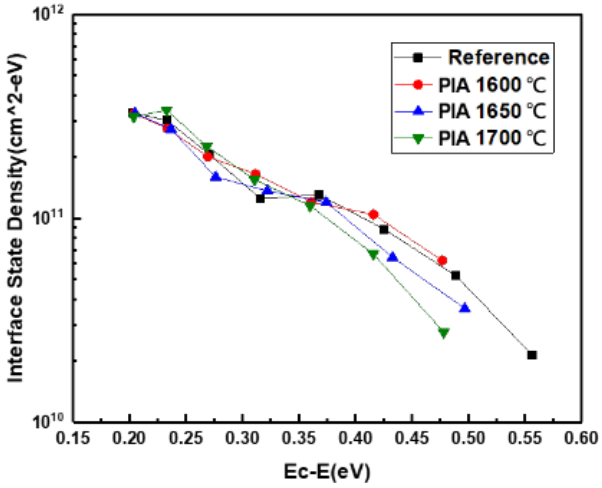


Fig. 3 Interface state density (D_{it}) of the samples with different PIA temperatures.

To further evaluated the gate oxide quality, constant voltage stress was performed and time-dependent dielectric breakdown (TDDB) was evaluated. Fig. 5 shows the gate current-time characteristics of all samples. The stress voltage was selected so that the initial electric field in oxide of each sample is similar. Very weak hole trapping phenomenon, i.e. gate current increases with time, is observed initially in the samples experienced PIA at 1600 and 1650 ℃. Apparent electron trap is observed on all samples and then the gate oxide breakdown. This is the typical phenomenon of the NO annealed gate oxide on SiC [5]. Fig. 6 shows the projection of the critical electric field for 10-year lifetime (E_{10y}) under 63% failure. Similar to the case of breakdown field, different but similar E_{10y} are extracted. There is no PIA temperature dependence.

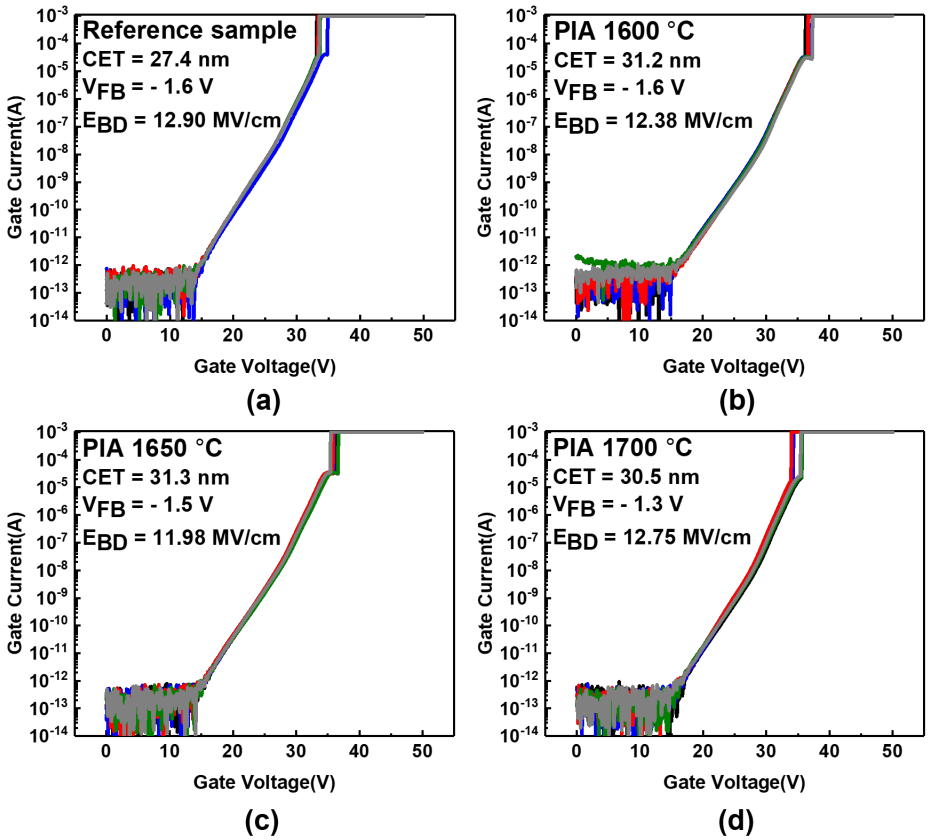


Fig. 4 Current-voltage (I-V) characteristics of (a) reference sample, (b) 1600 ℃ annealed sample, (c) 1650 ℃ annealed sample, and (d) 1700 ℃ annealed sample.

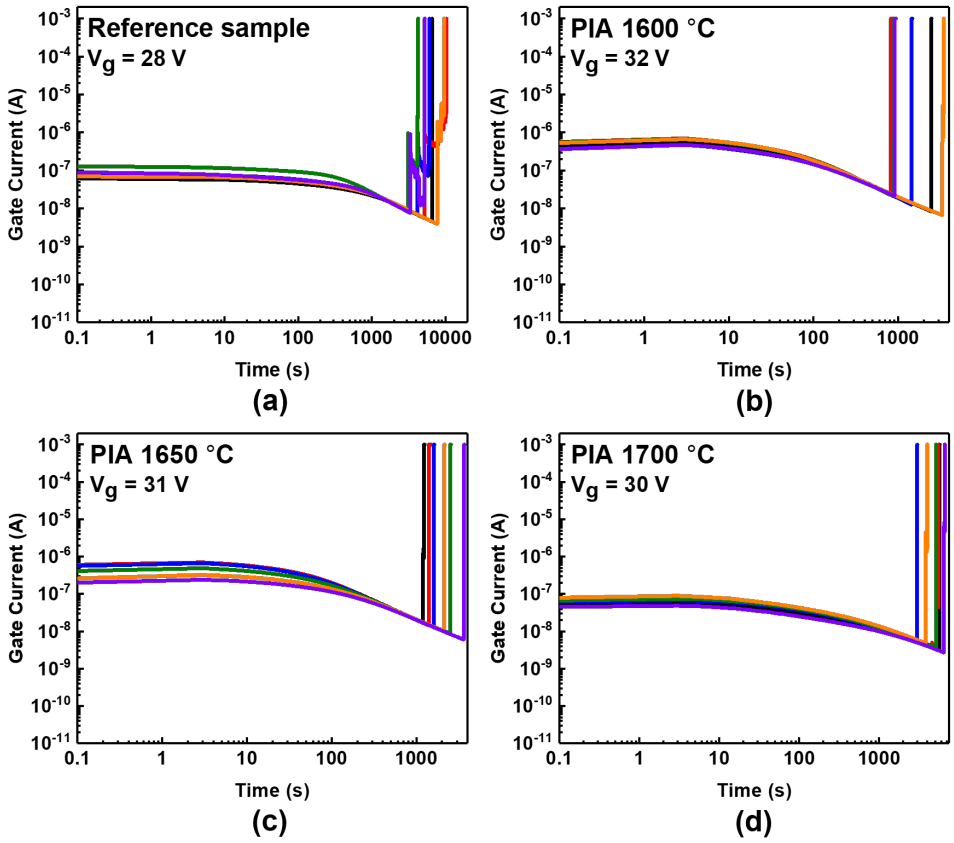


Fig. 5 Current-time (I-t) characteristics of (a) reference sample, (b) 1600 ℃ annealed sample, (c) 1650 ℃ annealed sample, and (d) 1700 ℃ annealed sample under constant voltage stress.

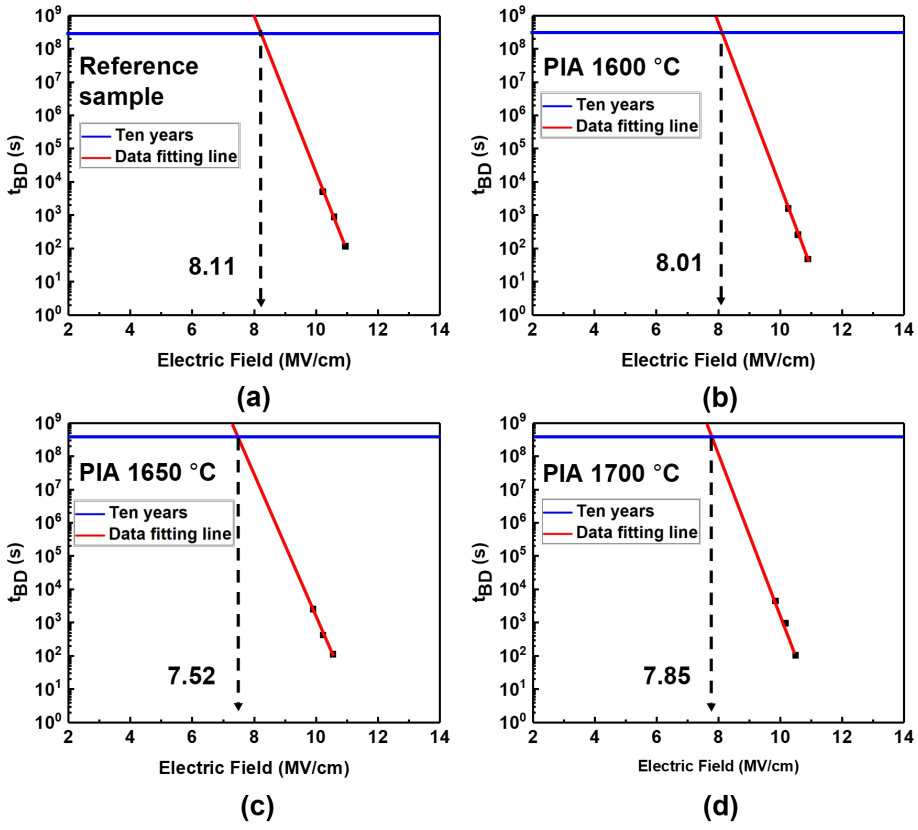


Fig. 6 Time-dependent dielectric breakdown (TDDB) performance of (a) reference sample, (b) 1600 ℃ annealed sample, (c) 1650 ℃ annealed sample, and (d) 1700 ℃ annealed sample.

Summary

According to the above results, although the surface roughness degrades after high temperature PIA, the interface state density, breakdown field, and the critical electric field for 10-year lifetime of the thermally grown gate oxide do not degrade. Furthermore, the interface roughness could be improved by the oxidation process. Therefore, it is suggested that the PIA condition can be determined independently, without considering the gate oxide characteristics. However, since the surface roughness degrades with the increase of the PIA temperature, the impact of surface roughness on channel mobility should be investigate.

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