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Evolution of Interface State Density and Near Interface Oxide Traps under Controlled Nitric Oxide Annealing in SiO_2/SiC Lateral MOSFETs

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Abstract. In this paper, the effect of different post oxide deposition nitridation processes in NO on n-channel lateral MOSFETs fabricated on implanted 4H-SiC were investigated. In particular, the electrical behavior of the MOSFETs was deeply investigated not only in terms of SiO_2/SiC interface state density and field effect mobility, but also considering the threshold voltage stability effect. The aim of this work was to explore to which extent post oxide deposition annealing in NO is beneficial for the MOS interface behavior and when their detrimental effects start to become predominant on the device performances. Here, the separation of the trapping states at the interface – either close to the conduction and valence band edges – and the near interface oxide traps are reported for the different duration of the post oxide deposition annealing. In fact, cyclic gate bias stress was employed in order to analyze the behavior of the trapping states and to correlate them with the variation of the benefits in terms of the channel mobility (that saturates at about 80 $cm^2V^{-1}s^{-1}$), and on the threshold voltage instability effect. In particular, prolonged PDAs may induce an increase of the amount of trapping states close to the valence band edge and inside the insulator of about 10% and 50 %, respectively.

Introduction

The conduction performances of 4H-SiC MOSFETs are strongly influenced by the processing of the SiO_2/4H-SiC interface [1]. In particular, the on-resistance and the field effect channel mobility (μ_{FE}) [2,3] can be improved by post-oxidation- or post-deposition-annealing (PDAs) in nitric oxide (NO) [4]. However, while the mobility is improved, the introduction of nitrogen during PDA can generate trapping states at the SiO_2/4H-SiC interface, which seems to introduce a detrimental impact on the threshold voltage (V_{th}) stability [5,6]. In this context, it is mandatory to explore the evolution of the interface state density not only close to 4H-SiC conduction band (D_{it}), but also close to the valence band. Moreover, it is relevant also to monitor the near interface oxide traps (NIOTs) that might be generated under prolonged PDAs in NO. This approach will elucidate if any detrimental effect occurs under prolonged PDAs in NO.

Experimental

In this paper, different n-channel lateral MOSFETs were fabricated on 4°-off-axis n-type (0001) 4H- SiC epitaxial layers (1×10^{16} cm^{-3}) an aluminum (Al) implanted body region ($N_A \sim 10^{17} cm^{-3}$). The gate oxide was a 55 nm thick deposited SiO_2 layer. Different duration PDAs were performed in a horizontal furnace in a sub-atmospheric pressure regime at 1175 °C in NO [7] in order to investigate the electrical evolution of both D_{it} and NIOTs at the SiO_2/4H-SiC system.

The MOSFETs were characterized acquiring the current voltage (I_D-V_G) transfer characteristics and capacitance–voltage (C-V) curves, in a CASCADE Microtech probe station equipped with a Keysight B1505A parameter analyzer.

Results and Discussion

Fig. 1 shows the field effect mobility μ_{FE} values measured on the MOSFETs subjected to PDAs in NO for 10, 20, 50, 90, and 120 min respectively. As can be noticed, the μ_{FE} values increased with increasing the PDA duration, but after 50 min the μ_{FE} values saturated (at about 80 $cm^2V^{-1}s^{-1}$). The peak mobility values are reported in Table I.

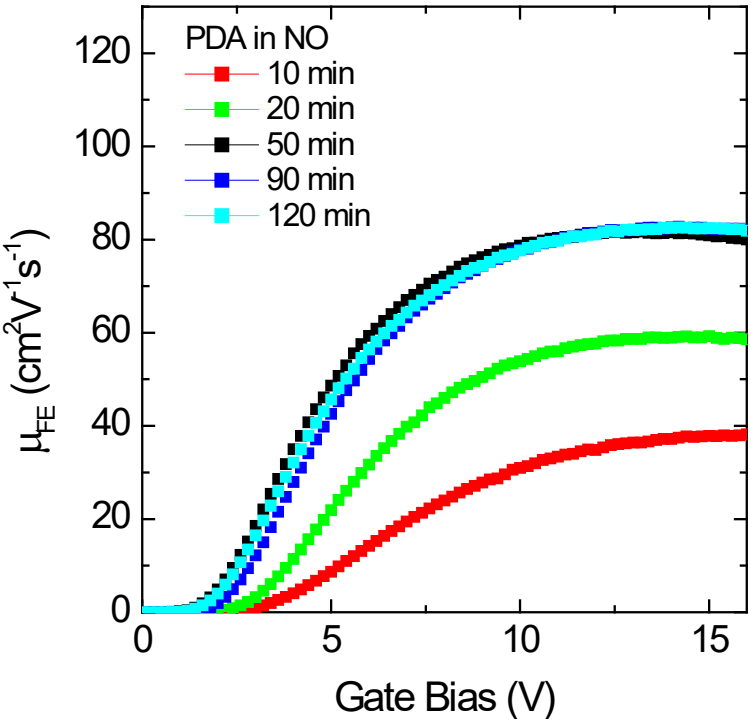

Fig.1: Field effect mobility values measured on 4H-SiC MOSFETs subjected to PDAs in NO of different duration.

Fig.2a shows the C-V curves collected at 100 kHz from negative toward positive gate bias (V_G) values and backwards (hysteresis not visible at a sweep rate of 0.1V/s). From the accumulation capacitance values measured in the positive V_G range, no significant oxide thickness variation is observed for PDA with times longer than 20 min. Hence, in our experimental conditions, the NO annealing duration did not change the oxide thickness, thus indicating that only a limited substrate re-oxidation occurred (< 3 nm). However, as can be noticed in Fig.2a, the slope of the C-V curves increases with increasing the NO annealing duration. This behavior is confirmed by the D_{it} profile – calculated by the Terman method that used the TCAD simulated curve as reference – shown in Fig. 2b, where the clear decrease of D_{it} can be correlated to the NO annealing duration. Table I shows the D_{it} data collected at 0.1 eV below the 4H-SiC conduction band, which decrease with increasing the NO annealing duration with a saturation at about 4×10^{11} $cm^{-2}eV^{-1}$.

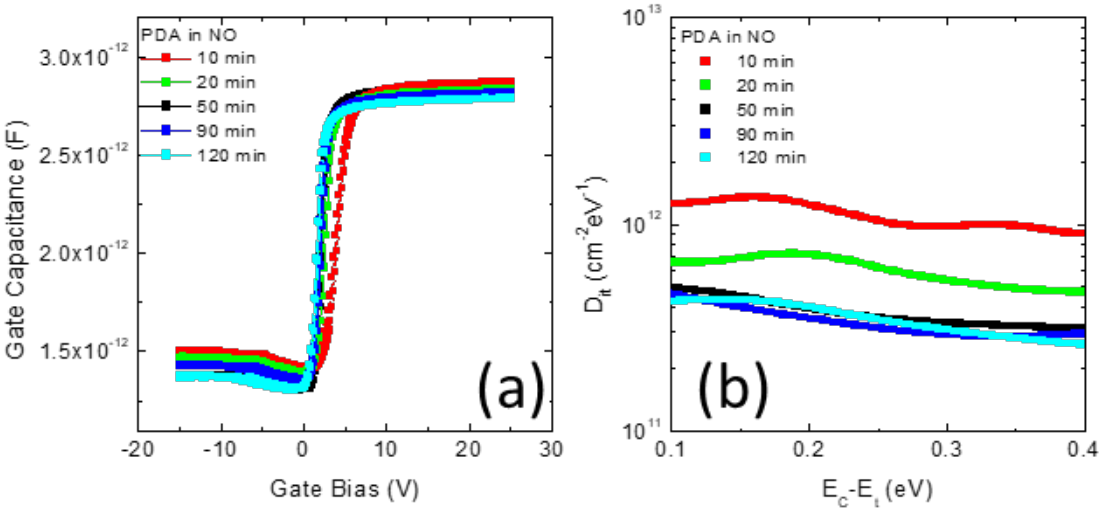

Fig.2: (a) C-V curves (with no Hysteresis) measured on the different MOSFETs subjected to different PDAs in NO. (b) D_{it} values obtained on the different MOSFETs subjected to different PDAs in NO.

The eventual detrimental role of a prolonged NO annealing duration can be assessed by monitoring the V_{th} stability (Fig.3). In fact, it has been observed that a prolonged exposure to oxidizing species (such as the NO) may increase the interfacial disorder correlated to the formation of sub-stoichiometric oxide layer and/or the formation of carbon-related defects [7].

In our case, by applying the non-relaxing stressing method to study the MOSFET V_{th} stability described in Ref. [4], it was possible to separate the different trapping contributions, affecting the SiO_2/4H-SiC systems under investigation. The threshold voltage variation ΔV_{th} (Fig.3) were converted into the amount of trapped charge (N_{Trap}) at the conduction (E_C) and valence (E_V) band edges and in near interface oxide region (NIOTs) as shown in Fig.4. The relevant data reported in Fig.4 are also summarized in Table I.

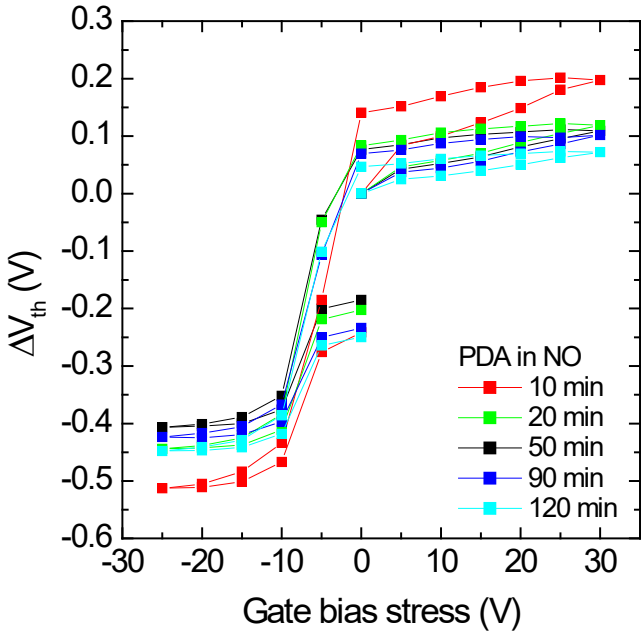

Fig.3: ΔV_{th} values obtained on the MOSFETs subjected to PDAs in NO of different duration.

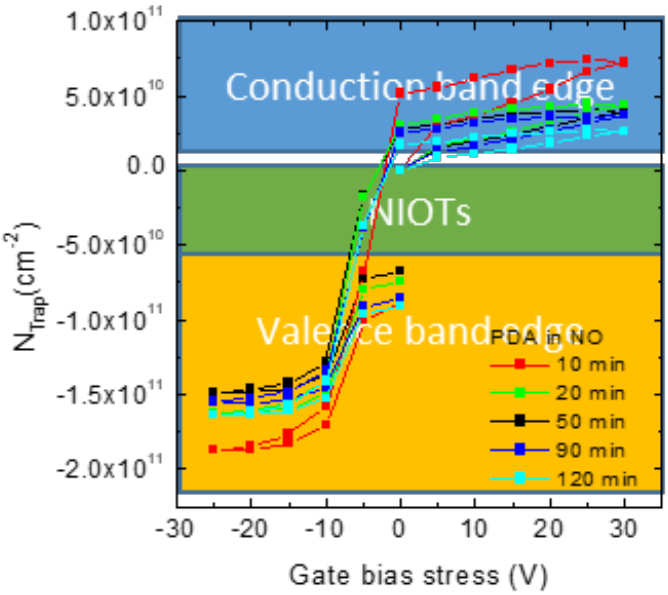

Fig.4: N_{Trap} values (calculated from data shown in Fig.3) obtained on the MOSFETs subjected to PDAs in NO of different duration.

Table I: Survey of the electrical data collected on the investigated MOSFETs.

Sample	μ_{FE} ($cm^2V^{-1}s^{-1}$)	D_{it} ($\times10^{11}cm^{-2}eV^{-1}$)	N_t at E_C ($\times10^{10}cm^{-2}$)	N_t at E_V ($\times10^{11}cm^{-2}$)	NIOTs ($\times10^{10}cm^{-2}$)
10min NO	38.2	12.48	7.22	1.88	8.84
20min NO	59.2	6.51	4.35	1.62	7.40
50min NO	81.7	4.21	3.98	1.49	6.77
90min NO	82.7	4.56	3.72	1.55	8.55
120min NO	82.6	4.21	2.63	1.64	9.13

As can be noticed, the increase of the PDAs duration results an increase of the field effect mobility and a reduction of the D_{it}. However, the amount of traps close to the valence band edge has a non-monotonic behavior – first it decreases with increasing the PDAs duration (from 1.88 down to 1.49 $\times10^{11}$ cm^{-2}), then it increases again (up to 1.64 $\times10^{11}$ cm^{-2}). Similarly the NIOTs suffers a non-monotonic behavior by long PDAs duration (from 8.88 $\times10^{10}$ cm^{-2} down to 6.77 $\times10^{10}$ cm^{-2} then up to 9.13 $\times10^{10}$ cm^{-2}). By a cross-comparison of all the electrical data summarized in Table I, it is possible to conclude that prolonged NO PDAs may induce detrimental effects. In particular, despite the improved μ_{FE} and D_{it} values, the amount of trapping states close to the valence band edge and inside the insulator are increased of about 10% and 50 %, respectively. Those increased trapping states increased the V_{th} instability for the prolonged NO PDAs devices.

Summary

In this paper, n-channel lateral MOSFETs fabricated on implanted 4H-SiC were investigated after PDAs in NO of different duration, by means of cyclic gate bias stress in order to analyze the behavior of the trapping states at the edges of the conduction and valence band of the semiconductor and in the near-interface region of the insulator. Alongside the benefits in terms of the channel mobility (that saturates at about 80 $cm^2V^{-1}s^{-1}$), a detrimental effect of a prolonged PDAs was observed. In particular, prolonged PDAs may induce an increase of the amount of trapping states close to the valence band edge and inside the insulator of about 10% and 50 %, respectively. Hence, a fine control of the NO PDA is required to improve the MOSFET interfacial transport and mitigating the threshold voltage instability.

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