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Oxide and Interface Defect Analysis of Lateral 4H-SiC MOSFETs Through CV Characterization and TCAD Simulations

A. Vasilev[1,a*], M. W. Feil[2,5,b], C. Schleich[1,c], B. Stampfer[1,d], G. Rzepa[4,e], G. Pobegen[3,f], T. Grasser[2,j], and M. Waltl[1,h*]

[1]Christian Doppler Laboratory for Single Defect Spectroscopy at the Institute for Microelectronics, TU Wien, Austria

[2]Institute for Microelectronics, TU Wien, Austria

[3]KAI GmbH, Villach, Austria

[4]Global TCAD Solutions GmbH, Vienna, Austria

[5]Infineon Technologies AG, Neubiberg, Germany

[a]vasilev@iue.tuwien.ac.at, [b]Maximilian.Feil@infineon.com, [c]schleich@iue.tuwien.ac.at, [d]stampfer@iue.tuwien.ac.at, [e]g.rzepa@globaltcad.com, [f]gregor.pobegen@k-ai.at, [j]grasser@iue.tuwien.ac.at, [h]waltl@iue.tuwien.ac.at

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Abstract. We investigated oxide and interface defects of lateral 4H-SiC MOSFETs through capacitance-voltage (C-V) and conductance-voltage (G-V) characterization at various frequencies and temperatures. By employing consecutive up and down sweeps of the gate voltage at three different temperatures, we experimentally characterized the hysteresis width as the difference between up and down sweeps in the depletion to accumulation (d-a) and depletion to inversion (d-i) regions. We observed an increase in the hysteresis width with decreasing temperature. Although the hysteresis width is not affected by the small-signal frequency, at the same time, increasing the frequency leads to a strong stretch-out effect, especially in the d-i region. Our measurement results indicate that the hysteresis deformation of the C-V curves is dominated by three different trap types. First, interface acceptor-like defects located close to the conduction band can follow the small-signal frequency. Slower acceptor-like border traps with trap levels both close to the conduction band and in the middle of the band gap are however responsible for the increase of trapped negative charge with increasing gate voltage. Finally, we assume the presence of a fixed positive charge.

Introduction

4H-SiC MOSFETs are a promising technology for high power electronics [1]. However, silicon dioxide (SiO_2) on a Si-face SiC surface still remains a major research topic due to the high defect density compared to the SiO_2/Si interface [2–13]. This is of particular concern because electrically active border and interface defects can not only affect the reliability of the device itself but also the operation of the application circuit [14]. Understanding the origin and influence of these different types of defects will help to reduce the defect density and increase device reliability. In this context, technology computer aided design (TCAD) can be a powerful tool to analyze the data from characterization measurements. Recently, some researchers have evaluated the influence of the interface traps on capacitance-voltage (C-V) curves by using Shockley-Read-Hall (SRH) theory [15–19]. In [15], the trapping behavior of interface and near-interface traps was simulated for MOS capacitors by employing SRH, trap-assisted tunneling and Frenkel-Poole models. The authors implemented both deep and shallow oxide traps to describe the hysteresis and the flat-band voltage shift increase with temperature. Furthermore, Marescra *et al.* [17] have not only shown that fixed positive charge influences the C-V curve, they also investigated the impact of variations in the capture cross section on the hysteresis effect. It was demonstrated that traps close to the valence or conduction bands are fast, while those close

to the mid bandgap are slow. Despite all these efforts to improve the understanding of C-V measurements in SiC devices, a complete simulation of a lateral 4H-SiC MOSFET calibrated and validated with measurement data at different small-signal frequencies and temperatures has not been performed yet.

In this work, we present such a TCAD [20] model including Shockley-Read-Hall (SRH) theory and the non-radiative multi-phonon (NMP) theory [21] for the description of charge transfer reactions associated with defects at the interface and in the oxide, respectively. The resulting model has been calibrated with C-V curves from impedance measurements at different temperatures and frequencies.

Devices and Experiment

We used lateral 4H-SiC nMOSFETs with a n^+ poly silicon gate. We assume an oxide thickness of $68\,\mathrm{nm}$ and a gate length of $7.5\,\mu\mathrm{m}$, see Fig.1, left. This oxide layer was formed on the Si-face substrate by chemical vapor deposition. For C-V and conductance-voltage (G-V) curve measurements, the small-signal method was used. For equivalent circuit capacitance and conductance were connected in parallel mode. Both the sinusoidal small-signal for each bias step and the gate voltage up and down sweeps were implemented for investigating the trapping dynamics, see Fig. 1, right [17,24]. The gate voltage V_{gs} is swept up and down within the range of $-30\,\mathrm{V}$ to $30\,\mathrm{V}$ at a sweep rate of $2.0\,\mathrm{V\,s^{-1}}$, see Fig. 1, right. The amplitude of the small-signal was $50\,\mathrm{mV}$ with a frequency between $4\,\mathrm{kHz}$ and $1024\,\mathrm{kHz}$. The time step for each gate bias was $0.13\,\mathrm{s}$ and the delay between up and down sweep was $12\,\mathrm{ms}$. The hysteresis width was extracted for operating temperatures of $300\,\mathrm{K}$, $373\,\mathrm{K}$, and $448\,\mathrm{K}$.

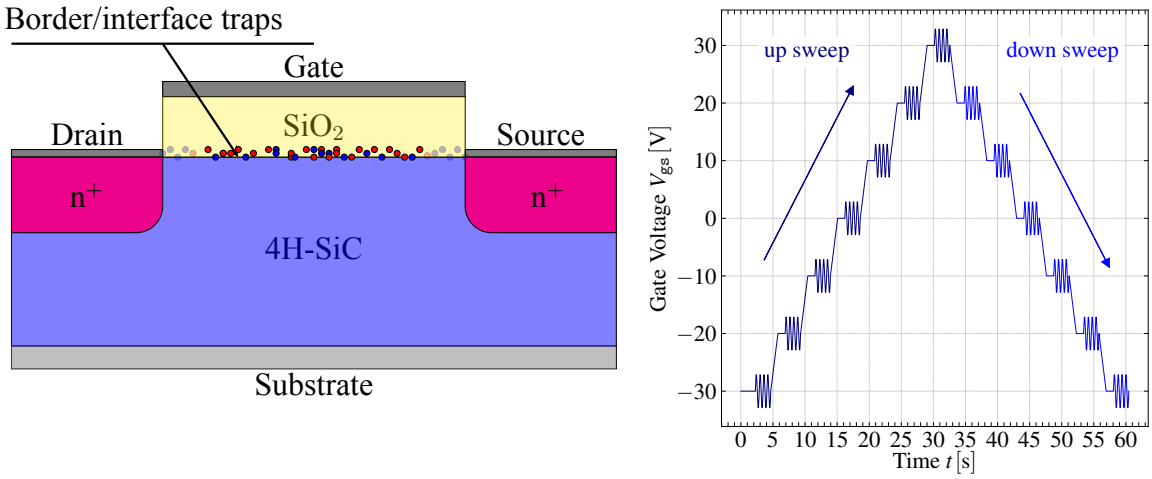

Fig. 1: Left: The used lateral 4H-SiC transistor. The possible defects leading to the distortion of the C-V curves are shown. Right: Schematic of the applied gate voltage during the impedance measurement. Both the small-signal and the gate voltage sweep are used in the transient analysis to investigate traps dynamics.

Measurement Results

Fig. 2 shows C-V and G-V curves measured at various temperatures and frequencies. The measured impedance has been corrected for parasitic impedances [6]. The horizontal line indicates the reference capacitance ($C_{\mathrm{cut}} = 4.3 \times 10^{-12}\,\mathrm{F}$) at which we define the hysteresis widths $\Delta V_{\mathrm{H}}^{\mathrm{d-a}}$ and $\Delta V_{\mathrm{H}}^{\mathrm{d-i}}$ between the up and down sweeps respectively. One can see in Fig. 2a the C-V curves are shifted by ΔV towards lower V_{gs} with increasing temperatures. The peak of conductance shifts towards lower gate voltage by $3\,\mathrm{V}$ with increasing temperature, see Fig. 2b, and the hysteresis width in the depletion to accumulation region $\Delta V_{\mathrm{H}}^{\mathrm{d-a}}$ is wider than in the depletion to inversion region $\Delta V_{\mathrm{H}}^{\mathrm{d-i}}$, whereby they slightly decrease with increasing temperature. We attribute this behavior to slow and border traps which are located within a few nanometers away from the SiC/SiO_2 interface [22, 23], see Fig.2, left. Fig.2c shows that the C-V curves are shifted towards higher V_{gs} when the frequency

is increasing. A frequency-dependent peak in the conductance around 2–8 V indicates the presence of interface states, see Fig.2d. Two reference capacitances are used for extracting the capacitance swing ($CS = \partial V_{\mathrm{gs}}/\partial C$).

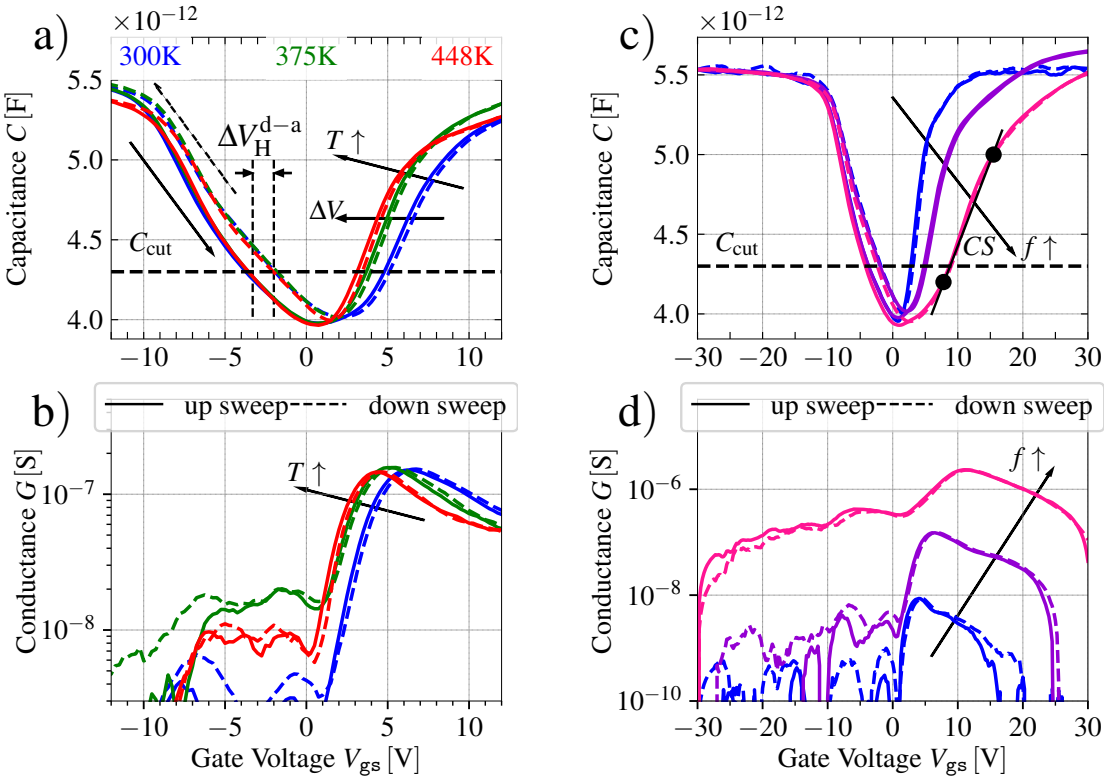

Fig. 2: a) C-V characteristics and b) conductance of a lateral 4H-SiC MOSFET at 64 kHz and 300 K, 373 K, and 448 K. c) C-V characteristics and d) conductance of a lateral 4H-SiC MOSFET at 300 K and frequency 4 kHz, 64 kHz, and 1024 kHz. The horizontal line indicates the reference capacitance ($C_{\mathrm{cut}} = 4.3 \times 10^{-12}$ F) at which we define the hysteresis widths $\Delta V_{\mathrm{H}}^{\mathrm{d-a}}$ and $\Delta V_{\mathrm{H}}^{\mathrm{d-i}}$ between the up and down sweeps respectively. Two reference capacitances are used for extracting the capacitance swing (CS).

The Modeling Framework

To explain the C-V curves at various frequencies from Fig.2a,c we used an exponential distribution of fast acceptor-like interface defects located close to the conduction band (see Fig. 3) [15–19]. Due to their small capture (τ_{c}) and emission (τ_{e}) time constants over a large bias range, charge trapping and detrapping can follow the small-signal modulation. The interface traps that capture electrons become electrically active and are directly integrated with the mobility degradation model. In a simplified way the effective mobility is proportional to $\mu_{\mathrm{C}} \propto \mu_0\,[(T/300\,\mathrm{K})^{\alpha}/(D_{\mathrm{it}}/10^{11}\,\mathrm{cm}^{-2})]$, where μ_{C} is the Coulomb component of mobility model. By fitting the measured and simulated curves we extract these parameters, which can reproduce the measured C-V curves with high accuracy. In our work we used $\mu_0 = 18\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, $\alpha = -9.2$, and $D_{\mathrm{it}}(T)$ is the temperature-dependent interface charge density [20]. The capture cross section for electrons and holes was $\sigma = 10^{-15}\,\mathrm{cm}^{-2}$ [20]. Our measurements show a negligible influence of donor-like traps which are located close to the valence band and which are hence not considered in the simulation, see Fig.2. Furthermore, we introduced a Gaussian distribution of slower acceptor-like border traps D_{ox}^2 close to the SiO_2/SiC interface, which turned out to be located around the middle of the 4H-SiC band gap. We further calculated the capture and emission times of the involved border traps by using the NMP model [21]. In this model, the asymmetry of barriers for the forward and backward processes leads to differences in charge capture and emission times. These barriers are determined by the relaxation energy $S = 4.0 \pm 0.1$ eV and

the parabolic curvature ratio $R = 2.0 \pm 0.1$. The bias dependent asymmetry of capture and emission times influences the hysteresis width from the depletion to the accumulation region. Also, we assume a second Gaussian distribution of slow acceptor-like border traps D^1_{ox} with a lower concentration which is energetically located close to the 4H-SiC conduction band. The relaxation energy of D^1_{ox} is $S = 0.1 \pm 0.01$ eV, and the parabolic curvature ratio is $R = 1.0 \pm 0.01$. These defects affect the hysteresis width of the depletion to the inversion region [25]. The high concentration of acceptor-like traps results in a severe positive voltage shift towards higher V_{gs}. Hence, we introduced fixed positive traps $N^{\text{fix}}_{\text{it}}$ to compensate for such a large ΔV shift. The parameters for the models are summarized in Table 1. The effective gate voltage shift for the up and down sweeps was calculated by using Eq. 1.

$$V_{\text{eff}}(f, \text{SR}, T) = V_{\text{ideal}}(T) + \Delta V_{\text{it}}(f, T) + \Delta V^1_{\text{ox}}(\text{SR}, T) + \Delta V^2_{\text{ox}}(\text{SR}, T) + \Delta V_{\text{fix}}(T) \tag{1}$$

Where V_{ideal} is the ideal C-V curve without any defects, ΔV_{it} is a shift caused by the interface traps, ΔV^1_{ox} is shift caused by slow traps which are located close to the conduction band and depending on sweep rate (SR) and temperature, ΔV^2_{ox} is shift caused by slow traps which are located close to mid gap and V_{fix} is fixed positive traps.

Table 1: Parameters for Traps.

Parameter	**Value**
Interface trap concentration D_{it}, $\text{eV}^{-1}\text{cm}^{-2}$	9.6×10^{13}
Exponential energy distribution σ^{it}_E, eV	0.1
Acceptor-like defect density D^1_{ox}, cm^{-2}	0.5×10^{12}
Acceptor-like defect density D^2_{ox}, cm^{-2}	2.0×10^{12}
Positive interface trap concentration $N^{\text{fix}}_{\text{it}}$, cm^{-2}	7.0×10^{11}
Exponential energy distribution $\sigma^{1,2}_{E\ \text{ox}}$, eV	0.1

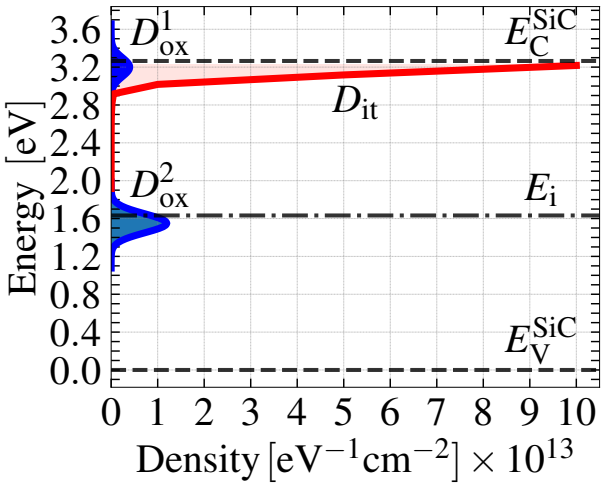

Fig. 3: The DOS for the D_{it} (red), D^1_{ox} and D^2_{ox} (blue).

Results and Discussions

Based on our measurement results and the modeling framework we investigated the behavior of the C-V curves at various temperatures and frequencies. Fig.4, right shows the comparison of the hysteresis width between measured and simulated C-V at $4\,\text{kHz}$ and $300\,\text{K}$. By increasing the gate voltage we scan the 4H-SiC band gap and see how traps with different energies influence the C-V curve.

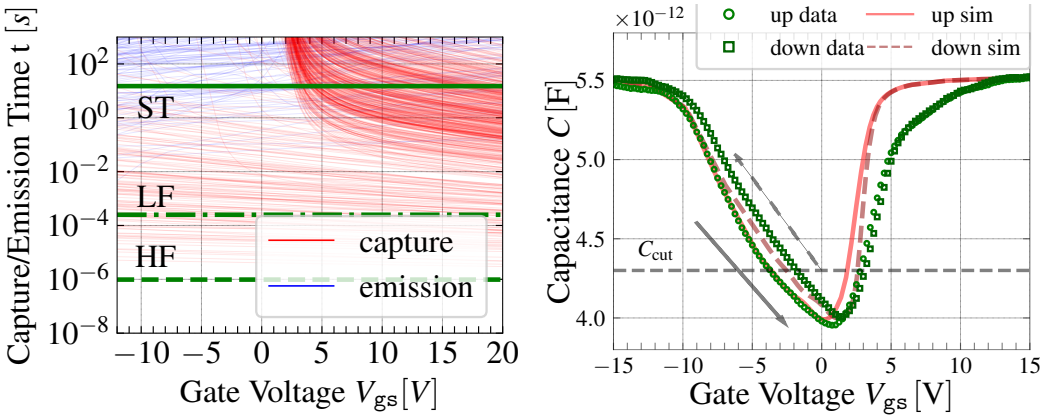

Fig. 4: Left: Simulated capture (red) and emission (blue) times of D^2_{ox}. The HF and LF lines refer to high and low frequency respectively, and ST is the sweep time. Right: Comparison of the hysteresis width with measured (green) and simulated C-V (red) at 4 kHz and 300 K.

Depending on their energy position relative to the Fermi level traps capture electrons and store them at different gate biases, thus two different hysteresis widths at the d-i and d-a regions occurred. In detail, the time evaluation of the slow acceptor-like traps D^2_{ox} indicates that by increasing the gate voltage, the emission times become longer than the capture times and partly even exceed the sweep time (ST), which means that some of the defects keep their charge state during the entire bias sweep, see at Fig. 4, left. Therefore, these slow defects appear to be responsible for the hysteresis width ΔV_H^{d-a}. Nevertheless, an increasing temperature decreases the hysteresis width, and ΔV_H from depletion to accumulation (d-a) is 10 times higher than from depletion to inversion (d-i). However, in case the emission time remains higher than the ST, we do not observe a strong temperature dependence of ΔV_H^{d-i}. This is because the down sweep time is enough to release electrons due to their fast time constants. Otherwise, at low temperature, during the up voltage sweep electrons are captured due to the emission time being larger than the capture time $\tau_e \geq \tau_c$, and traps become negatively charged. As a result, ΔV is shifted towards positive gate voltages, see Fig. 2a. When the gate voltage sweeps down, electrons tend to be emitted back to the channel but due to the large emission time distribution, some of the traps keep their charge state. The high temperature reduces both capture and emission times, thus, most of the traps become neutralized, and both the ΔV_H^{d-a} and the ΔV_H^{d-i} are small, see Fig. 2a. In contrast to the slow border traps, the fast interface traps have τ_c (τ_c =10^{-10}–10^{-13} s) even below $1/f_{HF}$ (high frequency, HF), see Fig. 4, left, thus they can follow the small-signal frequency.

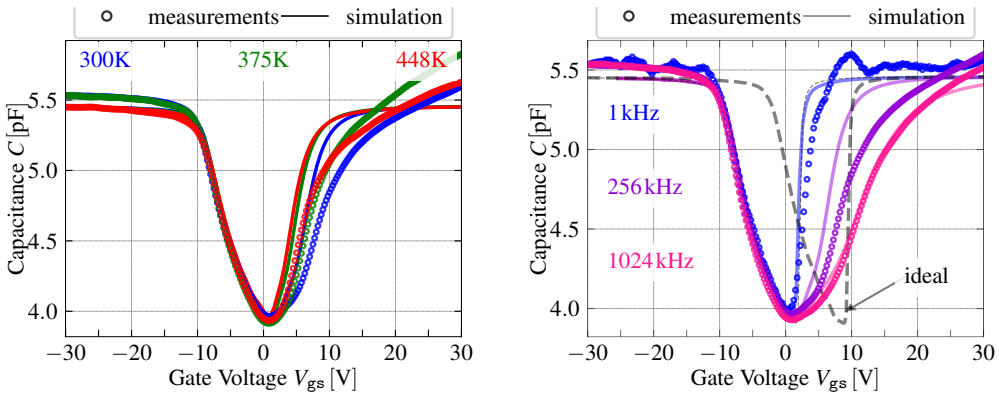

Fig. 5: Left: Measured and simulated C-V curves at 256 kHz and T=300 K, 373 K, and 448 K. Right: Measured and simulated C-V at 300 K and frequencies of f=1 kHz, 256 kHz, and 1024 kHz, compared to the ideal (defect-free) curve (black dashed lines).

Fig. 5 shows a comparison between measurements and simulation results. The difference in the capacitance values in the strong inversion regime at high frequencies indicates a residual parasitic impedance. The voltage shift ΔV strongly depends on temperature and frequency, especially from depletion to the inversion region, see Fig. 5, left. With the increasing temperature, the capture and emission rates increase as well (or at the same time $\tau_e < \tau_c$) which leads to defect neutralization and thus a decreasing voltage shift. The frequency dependence of C-V curve distortion indicates interface traps. Fig. 5, right shows that the fixed positive defects deviate the C-V measurement from ideal, and shift it towards lower gate voltages by 6 V at all frequencies (ΔV_{fix}). At the same time, the shape of the ideal C-V curve is close to the measurement at low frequency and is not affected by sweep rates and higher frequencies. The fast interface traps D_{it} can follow the small-signal frequency due to capture time being smaller than emission time.

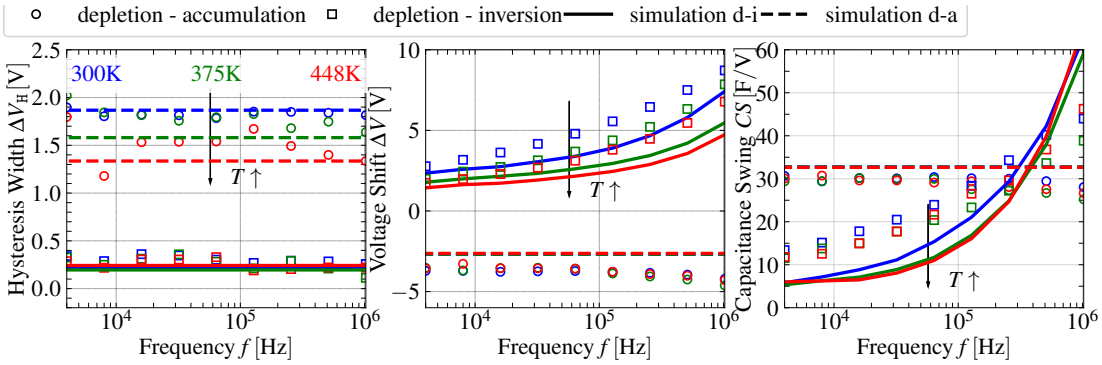

Fig. 6: Left: The hysteresis width at measured (circles and squares) and simulated C-V (solid and dashed lines). Middle: The voltage shift at C_{cut} at measured and simulated C-V. Right: The capacitance swing at C_{cut} at measured and simulated C-V.

Therefore, a lot of interface traps are charged and we observed the distortion at C-V curves under high frequency, see Fig.5, right. In addition, Fig. 6 depicts the extracted measured and simulated dependencies of the hysteresis widths, voltage shifts, and capacitance swings. The strong frequency and temperature dependence from depletion to inversion confirms the presence of interface defects, see Fig. 6, middle, right. The hysteresis width in the depletion to inversion region is narrow due to low trap concentration D^1_{ox}.

Summary

In this work, we have presented a physical-based modeling approach to calculate the temperature activation of the hysteresis width and voltage shift of C-V curves of lateral 4H-SiC MOSFETs. We show that these behaviors are due to the charging and discharging kinetics of slow border traps in the oxide. The hysteresis widths of depletion to accumulation and from depletion to inversion region are caused by an asymmetry of the capture and emission times. These widths depend on temperature and sweep parameters but do not depend on the frequencies. In addition to slow border traps, the fast interface traps are responsible for the distortion of the C-V curves at various frequencies. Although the distribution of defect states is probably more complex than the used distribution in our simulation, our approach can explain the charge trapping dynamics and the general behavior of lateral 4H-SiC MOSFETs.

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