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The Influence of Extended Defects in 4H-SiC Epitaxial Layers on Gate Oxide Performance and Reliability

Holger Schlichting[1,a*], Minwho Lim[1,b], Tom Becker[1,c], Birgit Kallinger[1,d] and Tobias Erlbacher[1,2,e]

[1]Fraunhofer Institute for Integrated Systems and Device Technology IISB, Schottkystr. 10, 91058 Erlangen, Germany

[2]Chair of Electron Devices, University Erlangen-Nuremberg, Cauerstr. 6, 91058 Erlangen, Germany

[a]holger.schlichting@iisb.fraunhofer.de, [b]minwho.lim@iisb.fraunhofer.de, [c]tom.becker@iisb.fraunhofer.de, [d]birgit.kallinger@iisb.fraunhofer.de [e]tobias.erlbacher@iisb.fraunhofer.de

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Abstract. For the ongoing commercialization of power devices based on 4H-SiC, increasing the yield and improving the reliability of these devices is becoming more and more important. In this investigation, gate oxide on 4H-SiC was examined by time-zero dielectric breakdown (TZDB) and constant current stress (CCS) time-dependent dielectric breakdown (TDDB) method in order to get insights into the influence of the epitaxial defects on the gate oxide performance and reliability.

For that purpose, MOS capacitors with different gate oxides have been fabricated. Crystal defects in the epitaxial layers have been detected and mapped by ultraviolet photoluminescence (UVPL) and interference contrast (DIC) imaging. The results of the comparison of electrical data and surface mapping data indicate a negative influence on the leakage current behavior for some extended epitaxial defects. Results from TDDB measurement indicated numerous extrinsic defects, which can be traced back to gate oxide processing conditions and defect densities.

Introduction

More and more, silicon carbide (SiC) devices are replacing silicon devices in power electronics [1]. This is due to numerous advantages of SiC compared to silicon. These properties make the devices more suitable for high voltage, high frequency, and high temperature applications.

The natural oxide of SiC is SiO_2, which makes it more compatible with silicon technology [2]. Despite all these benefits, there are still some issues that are problematic for mass-production of SiC based devices. For one, there is a relatively high number of substrate and epitaxial defects evident in the SiC crystal structure compared to silicon [3]. Moreover, the higher critical field strength, as a result of the wide band gap, leads to a higher field strength at the gate oxide semiconductor interface [4]. These two circumstances may lead to a decrease in yield and to reduced reliability of SiC devices. Since there was even a relationship between yield and reliability in semiconductor technology proposed [5], this topic is now further investigated for SiC technology.

In this study, gate oxide on 4H-SiC is investigated with time zero dielectric breakdown (TZDB) and constant current stress (CCS) time dependent dielectric breakdown (TDDB) measurements in order to get insights into the influence of the epitaxial defects and processing on the gate oxide performance and reliability.

Experiment

Processing. For this study, metal–oxide–semiconductor (MOS) capacitors in repeating units of different sizes were fabricated on two 4H-SiC wafers (“sample 1” and “sample 2”). The wafers used in this study are 150 mm n-type 4° off-axis 4H-SiC (0001) epitaxial wafers with an epilayer thickness of 11.5 µm and an epilayer nitrogen-doping concentration of 7E15 cm^{-3}.

These MOS capacitors were fabricated in our research SiC-CMOS processing line. The processing of the MOS capacitors included etching of alignment marks, high temperature annealing with carbon cap and sacrificial oxide process in order to condition the SiC-surface. Afterwards, the gate oxide process with subsequent deposition of an in-situ n-doped polysilicon layer (1200 nm) was performed. Two types of oxides were investigated. Sample 1 was processed with dry oxidation at 1300 °C and NO-annealing at 1300 °C (oxide thickness tox ~55 nm), while for sample 2 the oxide was deposited by LPCVD (TEOS), with subsequent NO-annealing at 1250 °C (tox ~60 nm). The polysilicon layer was structured using a photo resist mask and reactive ion etching. The oxide layer outside of the polysilicon pads is remaining at its initial thickness after the etching process on the whole wafer. This way it is ensured that the leakage current and breakdown will be located under the polysilicon electrode and not over a peripheral leakage current path outside the capacitor area.

Defect Detection. After etching of alignment marks, the epitaxial layers were examined and mapped with the surface scanning tool AQUILA by Intego for 150 mm 4H-SiC wafers. The methods used for defect detection were ultraviolet photoluminescence imaging (UVPL) and differential interference contrast imaging (DIC). The stimulation wavelength for UVPL was 305 nm. The single images of the UVPL as well as the optical surface images were automatically stitched together. A defect detection algorithm detected, classified, and counted the extended defects in the epilayers, such as triangular shaped stacking faults and particles/downfalls and growth pits. The locations and densities of extended defects can be exported from the software for further comparison with the electrical characteristics of MOS capacitors.

Electrical Characterization. After processing, the MOS capacitors on the samples were investigated by electrical characterization in a two-step investigation.

First, the MOS capacitors have been characterized by TZDB-measurement on a wafer prober to get a first statistic on their electrical performance. The electrical characteristics of the MOS capacitors of larger size (0.0133 cm^2), with a total number of capacitors per sample of 936, have been directly compared to the defect mapping of the wafer-mapping tool. Electrical measurements (IV) have been performed on an automatic wafer prober for TZDB.

In the second step, TDDB measurements were performed. Due to benefits, like more easily obtained charge-to-breakdown and sharper TDDB characteristics, CCS method was chosen for these measurements [6, 7]. For this investigation, smaller capacitors (0.0707 mm^2) have been selected, and the results were compared to the statistical results of epitaxial defect maps. In the measurement, a fixed current is applied between the electrodes. An abrupt decrease in the measured voltage indicates the dielectric breakdown. The time until this point is measured.

Results

Epitaxial Defects. Prominent epitaxial defects have been selected for the investigation. These defects are known from literature and previous investigations for influencing device performance and appearing in relevant densities [8, 9].

The investigated extended defects are shown in fig. 1a). Included are three types of triangle defects, named after their appearance in UVPL imaging. Triangle defects are known to be different types of stacking faults or poly type inclusions [10, 11]. While “dark triangles” and “mixed triangles” have a visible surface structure (shown in DIC images), “bright triangles” do not show this effect. The other defect types are downfalls and surface pits. Downfalls are ingrown particles from the epitaxial process, visible both in UVPL and DIC. Surface pits, which originate from threading screw and threading edge dislocation [12], are only visible in DIC. The densities of selected extended epitaxial defects are depicted in fig. 1b) for both samples. The density of mixed triangle defects and downfalls in approximately similar for both samples. For dark and bright triangle defects, the densities on sample 2 are around 5 times and 3.5 times higher compared to sample 1, respectively. Pits are by far the most common defect in the two epilayers. The density of pits is significantly higher than for the other investigated defects. Here as well, the density on sample 2 is twice as high as on sample 1.

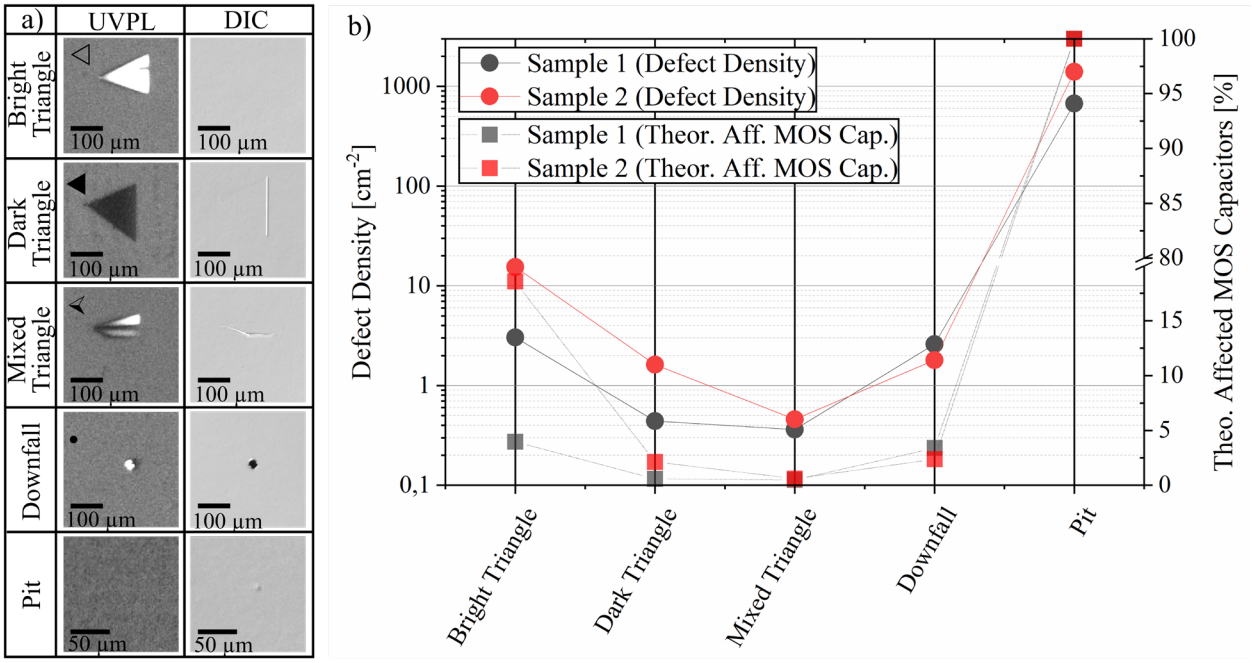

Figure 1. a) Investigated epitaxial defects in UVPL and DIC image. In b) the densities of extended epitaxial defects are depicted on a logarithmic scale (round symbols). The second pair of curves (square symbols) show the percentage of MOS capacitors, that are theoretically affected by one of the epitaxial defects.

In addition to the defect densities, the theoretical affected MOS capacitors for each examined defect type are depicted in the graph. These theoretical proportions of affected MOS capacitors were calculated with the Poisson yield model, making the simplified assumption of a homogeneous, random population of defects [13]. This leads to a rather high number of defect-affected devices, compared to other yield models, which account also for cluster or edge effects [14]. For this model, all capacitors have at least one pit below the oxide (100 % affected devices). For the rest of the examined defect types, the values are well below 5 %, except for bright triangles on sample 2.

TZDB Evaluation. Two examples for typical I/E characteristics extracted from TZDB measurement for each sample are shown in Fig. 2. The behavior for both types of oxide in logarithmic scale is quite similar for both samples. Up to a certain value, where the curves intersect at around 8.3 MV/cm, the leakage current for the thermally grown oxide on sample 1 is higher. After that point, this relationship is inversed and the thermally grown oxide from sample 1 reaches slightly higher electric fields at lower leakage current values until breakdown is reached. The blue line marks the field strength (8 MV/cm) that was selected for leakage current investigation on wafer level for the selected capacitors.

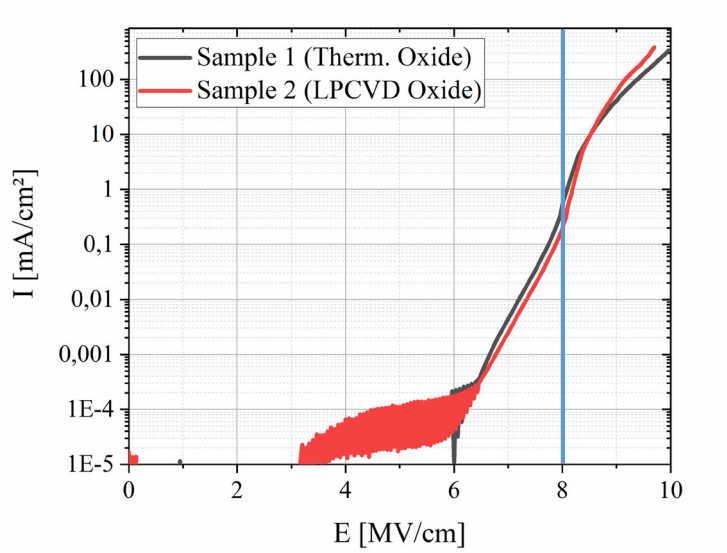

Figure 2: Current density over electric field in the oxide characteristic for two capacitors from both samples. The blue lines mark the point of investigation.

In Fig. 3, wafer maps of the current densities at a chosen electric field strength in the oxide are depicted. Each field represents one measured capacitor. The value in the cells of the wafer map is the measured leakage current at an electric field of 8 MV/cm in mA/cm². The relative value of the leakage current is also indicted by the color of the field, using a green-yellow-red scale (green = lowest leakage current, red = highest leakage current). For certain areas of the wafer, the leakage current for this electric field strength is up to seven times higher for sample 1 compared to sample 2. There is also a stronger deviation of leakage current over the wafer for the thermally grown oxide from sample 1 in contrast to the LPCVD oxide from sample 2.

Chips with significantly higher leakage current than the typical values are marked red. The value that was selected for this yield criteria was a leakage current over 800 mA/cm² and indicates a dielectric breakdown. The marked capacitors were compared with defects found on the defect maps from the previous surface investigation. Fig. 3 a) show results from sample 1 and fig. b) from sample 2.

Pits were excluded from this investigation, due to the high defect density in combination with the large capacitor area, which leads to the fact that statistically every capacitor for this is affected by at least one pit, assuming a homogeneous distribution.

The number of capacitors with strongly increased leakage current (defective criteria) is much higher (~ six times) for sample 2. Especially epitaxial defects with surface morphology (Mixed Triangles, Downfalls) are present on some of the capacitors with strong increase of leakage current.

More than half (63.6 % and 57.4%) of the samples with increased leakage current could not be traced back to any visible extended epitaxial defect. As mentioned before, pits may still be present on all devices.

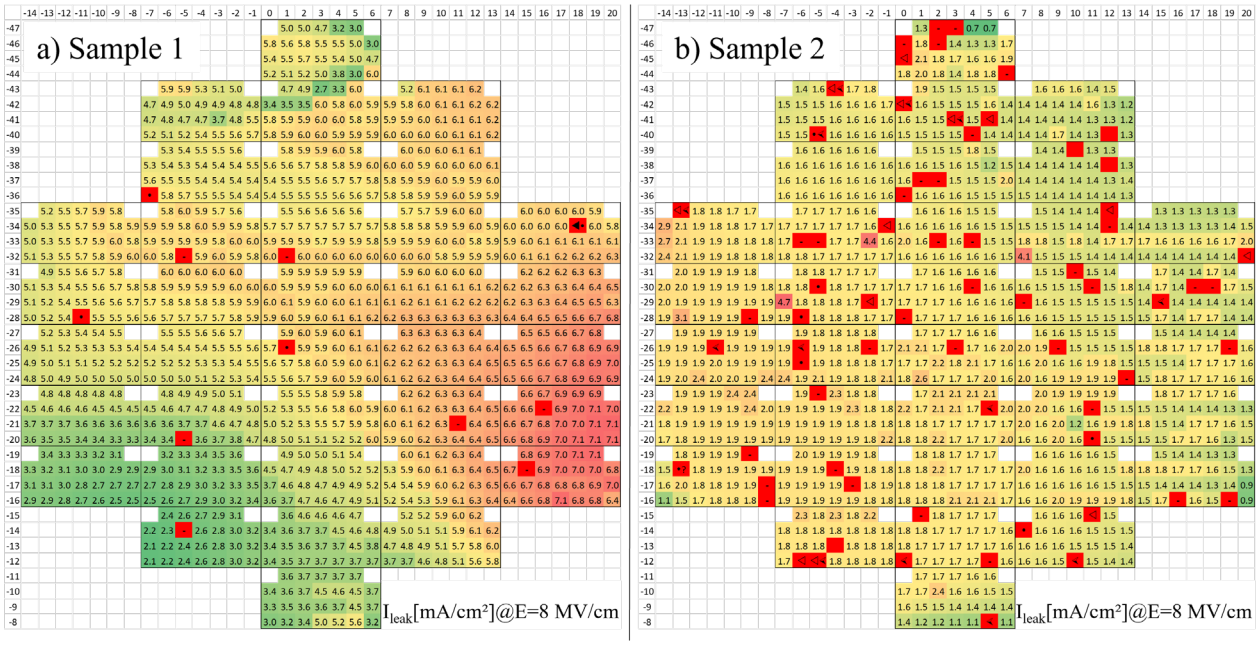

Figure 3: Wafer maps of current densities at 8 MV/cm for both samples. Devices with strong increase of leakage current at certain electric field are marked red with symbols of the corresponding epitaxial defects (see figure 1a)).

In Fig. 4, the statistics of the detected defects on the devices with a strong increase of leakage current are depicted. Some of the devices are affected by multiple defects, which is also accounted for in these charts.

If the values from this investigation are compared to the values from the theoretical calculation from Fig. 1 b), it can be seen that an extraordinary high proportion of devices with high leakage current are located on an extended epitaxial defect. However, many devices show higher leakage current at 8 MV/cm that are not affected by detected defects. Oxide defects or higher pit densities might be the reason for this observation. For defective devices with epitaxial defects, downfalls and mixed triangles appear to play a major role, if the total defect density is compared to number of conspicuous capacitors affected by said defects. The increased number of defective capacitors with extended epitaxial defects on sample 2 could be explained by the higher defect density.

The increase of defective capacitors without extended epitaxial defects on the other hand cannot explained by this. The reason might either the increased pit density, in combination with clusters of pits, or a higher oxide defect rate for LPCVD oxide.

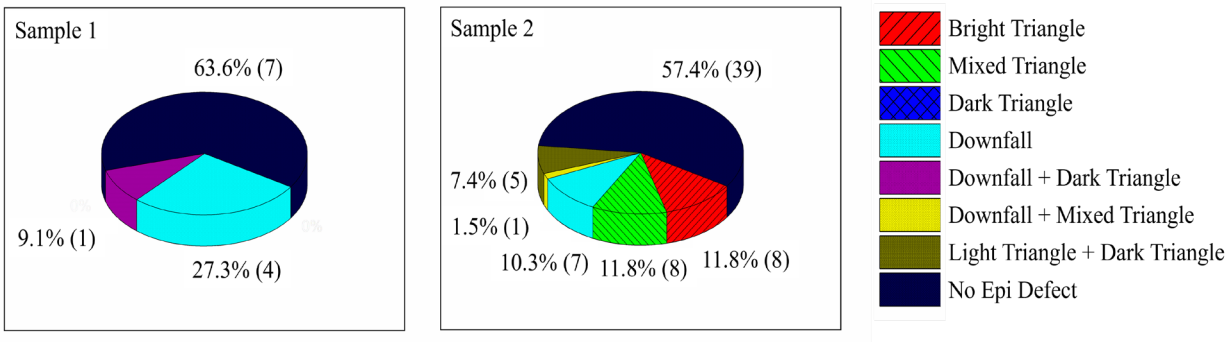

Figure 4: Statistic distribution of detected defects on capacitors with strong increase of leakage current for both samples at 8 MV/cm each.

TDDB Evaluation. In order to get further information on the impact of the different processing conditions and defect densities for these samples, reliability tests were performed.

Chips with direct voltage drop after application of the current were excluded from the measurement. These measurements were performed at room temperature. Three different current densities were chosen for this investigation, 50 mA/cm², 100 mA/cm² and 120 mA/cm². The time until dielectric breakdown is reached for each capacitor (t_{BD}) is plotted in a Weibull-distribution. In Fig. 5, the Weibull distributions for the CCS TDDB measurement of the MOS capacitors on selected samples are shown.

For all current densities, the different parts of the curves with intrinsic and extrinsic defects can be distinguished. There is a change of slope between the clearly extrinsic part of the curve and the intrinsic part. This can be explained by an overlap of extrinsic and intrinsic failure mechanisms. What is noticeable for these samples is a higher number of extrinsic defects for sample 2 at 120 mA/cm². Despite the two different types of oxides used for these samples, there is no major difference in the intrinsic distribution, except the slight change in curve progression for sample 2 at 50 mA/cm², which could be explained by some systematic defects.

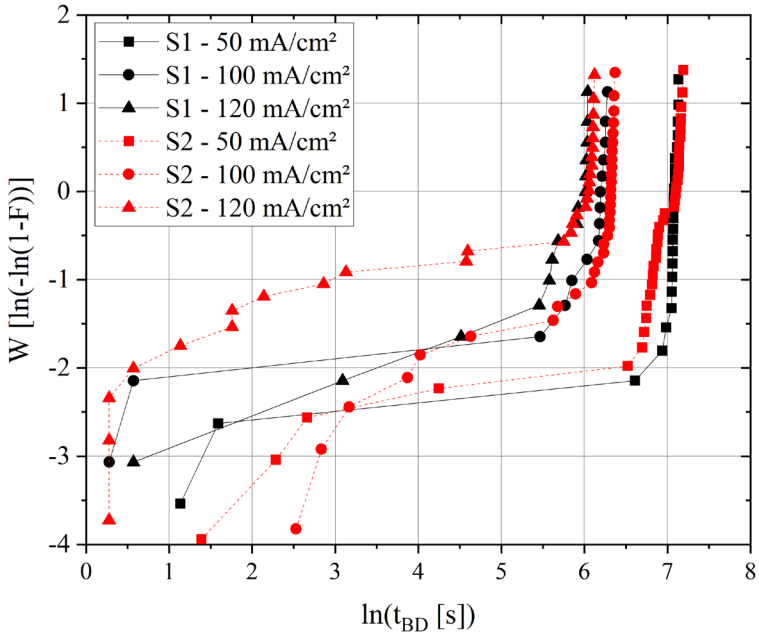

Figure 5. Weibull plots for the results of CCS TDDB measurements on sample 1 (S1) and sample 2 (S2) for different current densities.

While epitaxial defects may have stronger influence on the first pass yield and the extrinsic gate oxide failures, oxide processing including pre- and post-treatment may mainly influence the intrinsic part of the curve. However, the results also indicate a higher rate of extrinsic defects in the LPCVD oxide. Influence of surface pits on the reliability of oxides grown on 4H-SiC were already shown [15]. This defect may be the reason for an increase in extrinsic failures for sample 2. To distinguish the influence of surface pits and LPCVD oxide defects, further investigations on this topic must be made.

Summary

Two samples with different types of oxide and different defect densities have been investigated for gate oxide performance by TZBD and TDDB measurement. Especially epitaxial defects known for impacting substrate surface (mixed triangles, downfalls) are present on some of the tested capacitors with strong increase of leakage current. However, many devices show higher leakage current that are not affected by detected defects. The oxidation process and correlated oxide defects or higher pit density may be the reason for that.

The comparison of the theoretical number of capacitors affected by epitaxial defects and the actual defective and affected devices indicated, that there is a strong statistic influence of epitaxial defects on the leakage current behavior of the MOS capacitors. Especially the MOS capacitors with LPCVD oxide show a high number of dielectric breakdowns without being located on an epitaxial defect. Furthermore, the results from TDDB measurements show a clear extrinsic part of the characteristics, that are more prominent (higher number of extrinsic defects) for the sample with higher number of surface pits and with LPCVD oxide.

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