Materials Science Forum
ISSN: 1662-9752, Vol. 1090, pp 141-145
doi:10.4028/p-v0j9jt

Submitted: 2022-09-04
Revised: 2022-12-06
Accepted: 2022-12-06
Online: 2023-05-31

Improvement of Interface Properties for Thermally Oxidized SiC/SiO_2 MOS Capacitor by Post Oxidation Annealing Treatment

U. Chand[a], L.K. Bera[b]*, N. Singh[c], K.M. Han[d], V.Q.G. Roth[e], C.H.M. Chua[f], S. Chung[g]

Institute of Microelectronics, Agency for Science, Technology, and Research (A*STAR), Singapore 138634,

[a]chand_umesh@ime.a-star.edu.sg, [b]*beralk@ime.a-star.edu.sg, [c]navab@ime.a-star.edu.sg, [d]mhan@ieee.org, [e]roth_voo@ime.a-star.edu.sg, [f]chuahm@ime.a-star.edu.sg, [g]surasit_chung@ime.a-star.edu.sg,

Keywords: 4H-SiC MOS Capacitor, Post Oxidation Annealing, Interface trap density, Gate leakage current

Abstract. In this work, we report an innovative approach to improve the interface properties of SiC/SiO_2 metal oxide semiconductor (MOS) capacitors. High temperature (1350ºC) oxidation under different ambient is followed by a combination of post-oxidation annealing (POA) treatments using N_2, N_2O and NO gases. TOF-SIMS analysis shows silicon and nitrogen peaks near the SiC/SiO_2 interface. The silicon peak is attributed to the emission of silicon and carbon atoms during high temperature oxidation. The accumulation of nitrogen is caused by the presence of nitrogen during oxidation or POA. One of the lowest interface-trap densities along with good dielectric strength has been demonstrated with the N_2 and NO gas POA treatment.

Introduction

Silicon Carbide (SiC), in particular 4H-SiC polytype, is one of the most promising semiconductor materials for high-power devices due to its' wide bandgap, high breakdown electric field, and large thermal conductivity [1, 2]. Although SiC MOSFETs are commercially available, the on-resistance of medium voltage class SiC MOSFETs (~1 kV) is much higher than expected from the physical properties of bulk SiC due to the low channel mobility. This is attributable to the high interface state density (D_{it}) in SiC/SiO_2 structure [3-5]. Although, the exact origin of the high D_{it} for SiC/SiO_2 structure has not yet been identified, it is widely considered that carbon atoms that remain at the interface are plausible candidates. The key to obtain a high-quality SiC/SiO_2 interface may be the formation of SiO_2 on SiC without the creation of carbon-related defects and crystalline disorder [6].

To enhance the performance of SiC devices further for enabling applications in high-power and high-performance electronics, the improvement in mobility is very critical. To achieve that, a reduction of D_{it} is strongly required. Post-oxidation annealing (POA) is widely used as a passivation method [7,8] to improve channel mobility to some extent without substantial degradation of the dielectric properties of the gate oxide. However, till date, there are very few reports on the physical and chemical effects of the oxidation and annealing ambient on SiC/SiO_2 interface properties and channel mobility of SiC MOSFET.

In this work, we report on the engineering of the SiC/SiO_2 interface using different oxidation and post oxidation annealing (POA) treatments to improve the SiC/SiO_2 MOS interface. C-V results show that the interface trap density (D_{it}) was significantly reduced to $3\times10^{10}/eV^{-1}cm^{-2}$.

Results and Discussion

The SiC/SiO_2 MOS capacitors were fabricated on a 4º off-cut (0001) Si-face of 4H-SiC with a 10µm thick N-doped homo-epilayer deposited on a highly doped n-type substrate. The key process flow is described in Fig.1. Pre-gate surface cleaning was performed via RCA method followed by diluted hydrofluoric acid (DHF) dip. SiO_2 layers with a thickness of 50 nm were grown via thermal oxidation at 1350ºC in O_2 for 18 minutes, followed by post-oxidation annealing at 1300ºC in N_2, N_2O and NO gas for 30 min. The detailed thermal oxidation conditions are described in Fig.1. After each oxidation, the grown oxides were characterized by cross-sectional transmission electron microscopy (TEM) and time-of-flight secondary-ion mass spectrometry (ToF-SIMS) measurements. A 200 nm thick aluminum metal was evaporated on the front side using a shadow mask to create top electrode of the MOS capacitor while blanket metal was deposited on the back surface of substrate to form back contact. In the following electrical characterizations of the devices, a B1500A semiconductor parameter analyzer is used.

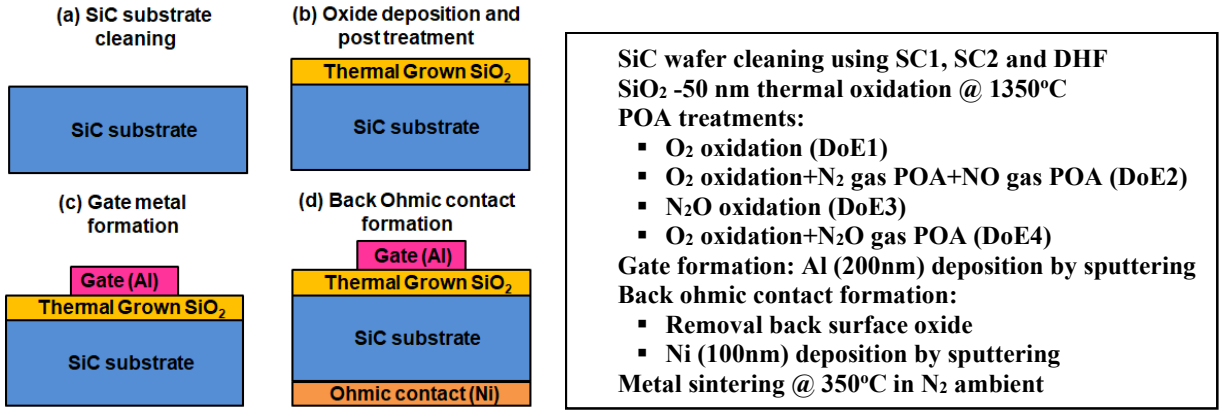

Fig. 1 (a-d) Illustration of fabricated SiC/SiO_2 MOS capacitors and key process flow of SiC/SiO_2 MOS capacitors fabrication.

To confirm the influence of annealing on SiC/SiO_2 interface, ToF-SIMS data of the SiO_2 layer is analyzed (Fig.2). The devices treated with N_2 and NO gas shows the presence of nitrogen at the SiO_2 interface as observed on the peak location inside the SiO_2, implying that annealing process only affects the interface and not the physical morphology. Si peak was also observed at the interface due to the migration of Si and C during the thermal oxidation process [11]. The migrated C interstitials into the oxide diffused toward the oxide surface, which react with O_2 to form CO_2 and evaporated. Fairly Si-rich interfacial layer exists at high-temperature oxidation process as observed from TOF-SIMS.

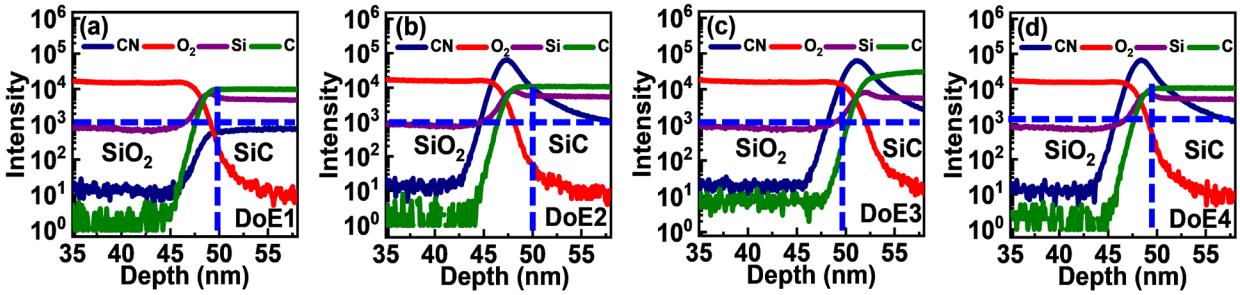

Fig. 2. ToF-SIMS depth profiles of CN, O_2, Si, and C of the SiC/SiO_2 MOS capacitors: (a) O_2 oxidation, (b) O_2 oxidation + N_2 gas POA + NO gas POA, (c) N_2O oxidation, and (d) O_2 oxidation + N_2O POA.

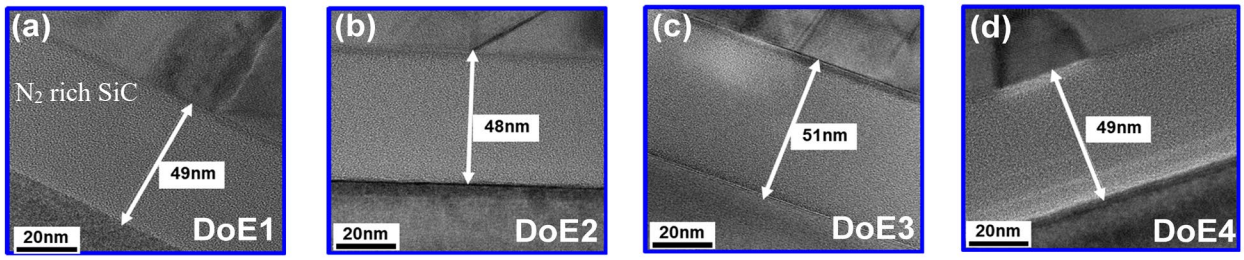

Fig. 3 Cross-sectional TEM of the SiC/SiO_2 interface: (a) O_2 oxidation, (b) O_2 oxidation +N_2 gas POA+ NO gas POA, (c) N_2O oxidation, and (d) O_2 oxidation + N_2O POA.

Moreover, we have carried out high resolution cross-sectional TEM imaging of our samples to examine the existence of any other additional layer at SiC/SiO_2 interface after POA treatment as shown in Fig. 3. Observation of no additional layer implies that the POA treatment process only affects the gate dielectric and interface trap charges, and not the physical morphology. The nitrogen profiling was carried out using EDX of HRTEM as shown in Fig.4. Nitrogen rich layer thickness in SiC near SiO_2/SiC interface clearly observed.

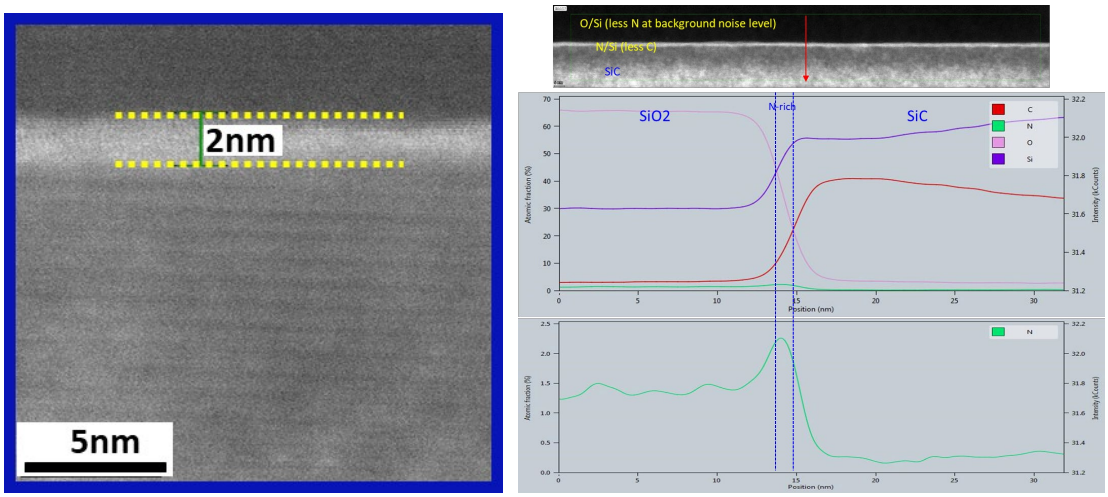

Fig. 4. HRSTEM SiO_2/SiC interface and EDX line scan of elemental analysis

Gate leakage current density (J_G) is plotted as a function of V_G as shown in Fig. 5(a), to examine the film quality of the SiO_2 gate dielectric. The extrapolated gate leakage current density (J_G) is 10^{-10} A/cm^2 in the range of the applied V_G from 0V to 25V for 50nm SiO_2 and this suggests superior film quality of the SiO_2 gate dielectric.

Furthermore, a capacitance-voltage (C-V) test under forward and reverse sweep of gate bias is performed to further investigate the effect of POA at the SiC/SiO_2 interface. Fig. 5(b) shows the measured C-V characteristics of all the fabricated SiC/SiO_2 MOS capacitors at a high frequency of 1MHz. It is found that the device with SiO_2 treated by N_2 and NO POA exhibits the smallest clockwise hysteresis. Such small hysteresis window indicates that the presence of least number of traps at the SiC/SiO_2 interface.
The interface state density is extracted using Hill–the Coleman conductance method [2]

$$D_{it} = \frac{2}{qA}\frac{G_{m,max}/\omega}{\left(\frac{G_{m,max}}{\omega C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2}$$

where $G_{m,\,max}$ and C_m are the corresponding peak conductance capacitance respectively at the same gate bias, C_{ox} is oxide capacitance at accumulation, obtained using single frequency C_{ox}-V_G techniques. Fig. 5(d) benchmarks the D_{it} of SiC/SiO_2 MOS capacitors and other reported SiC based MOS capacitors [9,10]. It is clear that the device with N_2 gas POA+NO gas POA treatment in this work achieves lowest D_{it} (3×10^{10}/eV^{-1}c m^{-2}) among all SiC-based capacitors. However, DoE-2 resulted in the highest density of net positive charge in SiO_2 film. These 4 DoE results suggested that channel mobility, V_{th} and J_G leakage can be trade-off and optimized to meet a wide range of applications using SiC-based devices.

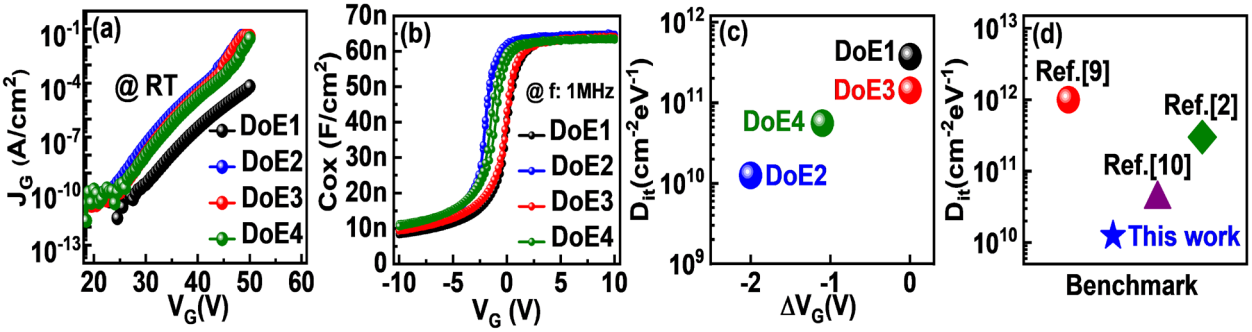

Fig. 5 (a) J_G -V_G for the SiC/SiO_2 MOS capacitors measured at room temperature. (b) Typical C_{ox}-V_G curves of the SiC/SiO_2 MOS capacitors measured at 1MHz. (c) Comparison of D_{it} and ΔV_G (measured at flat band voltage with normalization with the DoE1) with different annealing conditions. and (d) Benchmark plot of D_{it} showing the lowest D_{it} among all reported SiC based MOS capacitors.

Summary

In summary, we have presented the effect of high temperature oxidation and post oxidation annealing on the SiC/SiO_2 MOS capacitors. Interestingly, it is found that the SiC/SiO_2 interface are effectively influenced by POA treatment on the SiO_2 layer. It is noticed that N_2 gas POA+NO gas POA treatment improves the SiC/SiO_2 interface quality. The lowest D_{it}, almost hysteresis-free, and decent gate leakage current density among other post-oxidation annealing conditions have been experimentally demonstrated.

Acknowledgement

This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research) Singapore, under Grant No. A20H9a0242.

References

[1] N. S. Saks, S. S. Mani, and A. K. Agarwal, Appl. Phys. Lett. 76, 2250 (2000).

[2] L. K. Bera, N. Singh, Z. Chen, C. M. Chua, K.J. Chui, R. Singh, S. Chung, K. M. Han, K. Chong, and D. L. Kwong, ECSCRM, 2021.

[3] E. Arnold and D. Alok, IEEE Trans. Electron Devices 48, 1870 (2001).

[4] S. Harada, R. Kosugi, J. Senzaki, W. J. Cho, K. Fukuda, K. Arai, and S. Suzuki, J. Appl. Phys. 91, 1568 (2002).

[5] T. Kimoto and H. Watanabe, Appl. Phys. Express 13, 120101 (2020).

[6] T. Kobayashi and Y. Matsushita, J. Appl. Phys. 126, 145302 (2019).

[7] L. Huang, Y. Liu, C. Xiao, Y. Ding, X. Peng, Y. Onozawa, T. Tsuji, N. Fujishima, and J. Sin, IEEE Trans Elect. Dev. 68, 2133 (2021).

[8] C. Wanb, H. Xub, J. Xiaa, and J.-P. Ao, Journal of Crystal Growth 530,125250, (2020)

[9] M. Noborio, J. Suda, and T. Kimoto, Applied Physics Letter, 93, 193510 (2008).

[10] K. Tachiki , M. Kaneko, and T. Kimoto, Applied Physics Express 14, 031001 (2021).

[11] Y. Hijikata, R. Asafuji, R. Konno, Y. Akasaka, and R. Shinoda, AIP Advances 5, 067128 (2015)