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High Mobility Silicon Dioxide Layers on 4H-SiC Deposited by Means of Atomic Layer Deposition

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Abstract. A study on the impact of different growth and deposition techniques on the reliability of silicon dioxide (SiO_2) layers on silicon carbide (SiC) metal-oxide-semiconductor capacitors (MOSCAPs) is presented and compared to channel mobilities that were extracted from lateral metal-oxide-semiconductor field-effect transistors (LMOSFETs). Oxide layers were formed using atomic layer deposition (ALD), low pressure chemical vapour deposition (LPCVD) and direct thermal growth, including post-deposition anneals (PDAs) in nitrious oxide and forming gas (FG) for the ALD- and LPCVD-deposited oxides. Electrical characterisation results at elevated temperatures show that a PDA in FG leads to the highest average breakdown electric field of 10.08 MV/cm, outperforming all other device splits. Time-dependent dielectric breakdown (TDDB) results showed that the time to failure of 63% of the investigated samples at 9MV/cm in the FG-annealed samples was about 50% higher than in LPCVD-deposited oxides that had undergone an N_2O PDA. Channel mobilities of the FG-treated samples averaged about three to four times higher than in other datasets, showing excellent peak field-effect mobilities of 60 $cm^2/V.s$ and 108 $cm^2/V.s$ at room temperature and 175°C, respectively.

Introduction

The successful implementation of silicon carbide into commercial power electronics conversion stages is in no small part due to its readily available native oxide, silicon dioxide (SiO_2). This can be thermally grown with reasonable interface quality at temperatures between 1200°C-1400°C [1], making SiO_2 the ubiquitous gate oxide in any commercially available SiC metal-oxide-semiconductor field effect transistor (MOSFET).

However, interface defect densities are much more prevalent in SiC/SiO_2 systems than in their Si/SiO_2 metal-oxide-semiconductor (MOS) counterparts [2], and most of these defects originate from the thermal oxidation process, which ends up forming carbon-rich interfaces containing carbon clusters, hydrogen (H) and oxygen (O) vacancies. These defects enhance scattering, increase leakage currents and hence reduce channel mobilities in MOSFETs. This is a major technological issue, leading to specific on-resistances ($R_{ON,SP}$) that are much higher than their theoretical limits, hampering the further uptake of SiC MOS technology.

Unlike with thermal oxidation, deposition techniques such as atomic layer deposition (ALD) or low-pressure chemical vapour deposition (LPCVD) offer a lower deposition temperature, excellent thickness control and suitability for conformal deposition of gate oxides in trench power device structures. They also do not consume any of the SiC material, meaning that the interface is less likely to be carbon-rich after deposition [3]. However, the electrical properties of as-deposited SiO_2 layers are poor [3, 4], and, after their deposition on SiC, a post-deposition anneal (PDA) typically follows in a nitrogen-containing ambient, such as nitric (NO) or nitrous oxide (N_2O) at temperatures above 1,100°C [5]. In this work, we present the improvement brought about by deploying ALD-deposited

SiO2 layers which were post-deposition annealed in forming gas (FG) and N_2O ambient. This is analysed by observing time-dependent dielectric breakdown (TDDB), capacitance-voltage (C-V), current-voltage (I-V) and channel mobility results.

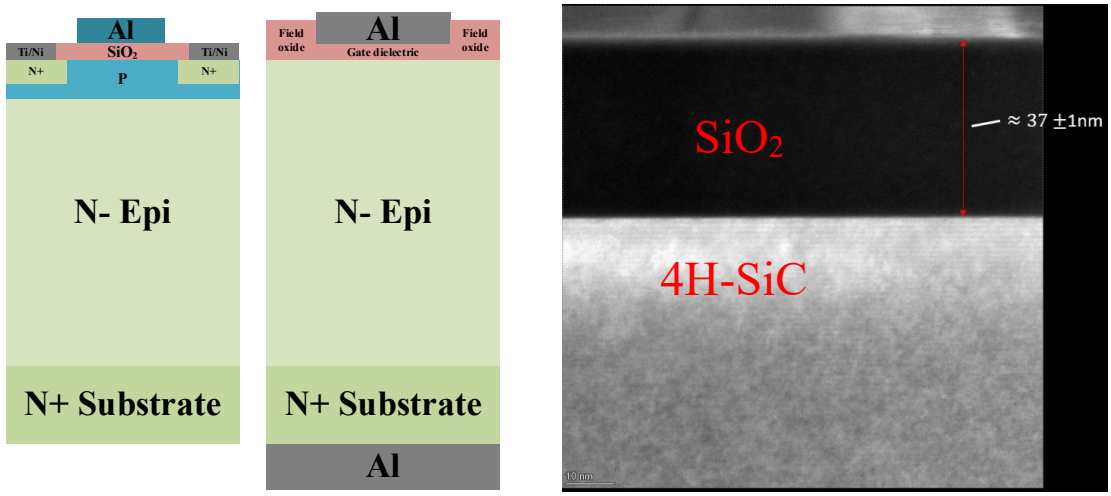
Experimental

Devices were fabricated on 10 µm thick, intentionally nitrogen-doped (4 x 10^{15} cm^{-3}) epilayers on a highly nitrogen-doped SiC substrate. Lateral MOSFET samples underwent a conventional implantation schedule for the p-base and n+-source and drain implant, both carried out at 500°C, with the post-implantation anneal carried out at 1,700°C for 45 minutes in Ar (5 slm).

Once the samples had undergone an initial RCA1/HF(10%)/RCA2/HF(10%) clean procedure, a 1 µm thick field oxide was deposited on the samples through LPCVD, details of which are outlined below. The process window was opened by means of photolithography and the deposited oxide was thinned to approximately 30 nm in the gate area through reactive ion etching (RIE). The final 30 nm were removed using a wet etch in diluted 10% buffered oxide etch (BOE). The gate oxides were then deposited or grown using one of the following oxidation routines:

1. **ALD** deposition of SiO_2 using bis(diethylamino)silane (BDEAS) and an oxygen plasma at 200°C (750 cycles) or
2. **ALD** deposition of SiO2 using bis(diethylamino)silane (BDEAS) and an oxygen plasma at 200°C (750 cycles) plus a **PDA in FG** ambient (5 slm, 5%H_2) at 1,100°C for 1 h.
3. **LPCVD** using tetraethyl orthosilicate (TEOS) as a Si precursor.
4. **Direct thermal growth** at 1300°C for 5 hrs in diluted **N_2O** (4 slm Ar: 1 slm N2O) ambient.

Since samples that had undergone routines 1 and 3 usually show a poor as-deposited oxide quality, a post-deposition anneal was performed on these samples in an oxidation furnace in N_2O ambient at 1300°C for 2 hrs. All N2O treated samples (1,3 and 4) an oxide thickness of approx. 60 nm, with the FG-treated sample showing a lower thickness of approx. 35 nm. This process has shown to result in excellent SiO_2/SiC interfaces and was reported previously by the authors [3]. The oxide growth/deposition of all samples was then followed by the contact formation to finalise the device structures.



(a) (b) (c)

Fig. 1: Schematic cross section of the fabricated lateral metal-oxide-semiconductor field-effect transistor (LMOSFET) (a) and MOSCAP (b) as well as a cross-sectional TEM image to verify the oxide thickness of a ALD FG-annealed SiO_2 MOSCAP (c).

For MOSCAPs, 500 nm thick aluminium (Al) top- and bottomside contacts were e-beam evaporated.

LMOSFET structures used a 30 nm Ti/ 100 nm Ni e-beam evaporation followed by a RTA at 1,000°C for 2 minutes in Ar (5 slm ambient) to form source and drain contacts. This was then followed by a 500 nm Al gate contact deposition. A cross-section of the fabricated MOSCAP and LMOSFETs can be seen in Fig. 1 (a) and (b), respectively. To verify the oxide thickness, cross-sectional transmission electron microscopy (TEM) scans were carried out, that can be seen in Fig. 1 (c).

Room temperature vertical C-V measurements were performed on at least 20 MOSCAPs using an Agilent E4980A LCR meter to extract flatband voltage, hysteresis and frequency dispersion values, which are not going to be separately reported here. The results of these measurements can be found in [6]. Furthermore, vertical I-V as well as constant-voltage TDDB measurements were performed at 175°C using a Semiprobe semi-automatic probe station with a Keysight B1505A parameter analyser. Lateral MOSFET measurements were done at the same semi-automatic probe station rig at room temperature.

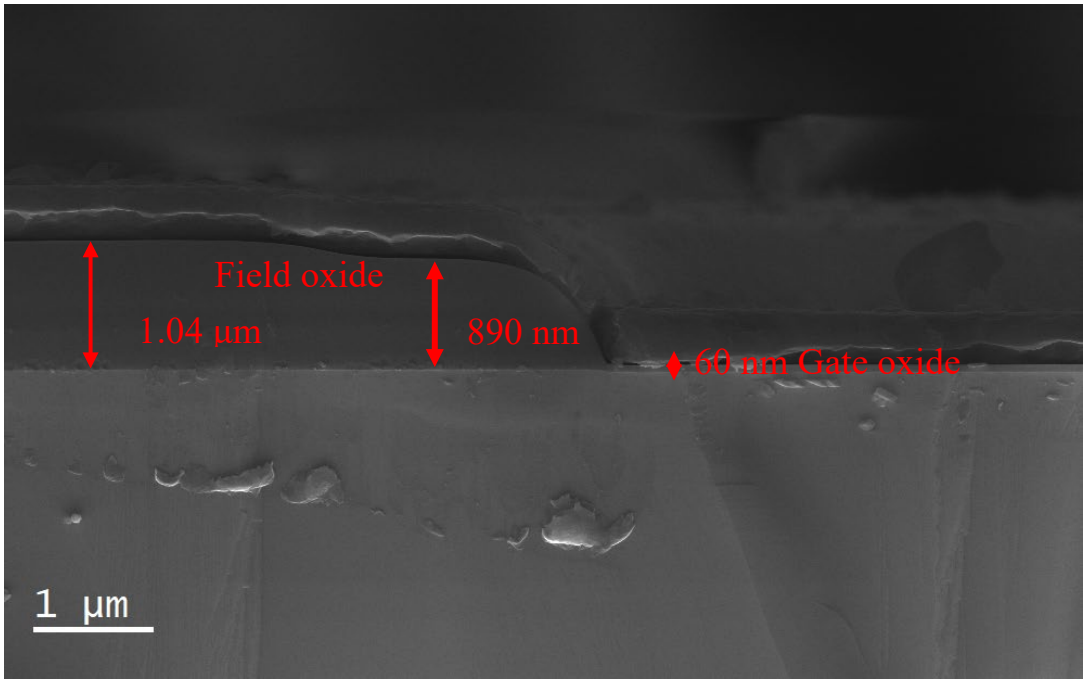
Results

An overview of the constant voltage TDDB as well as average breakdown fields of the investigated vertical device structures (Fig. 2 (a)) at 175°C can be found in Table 1 below.

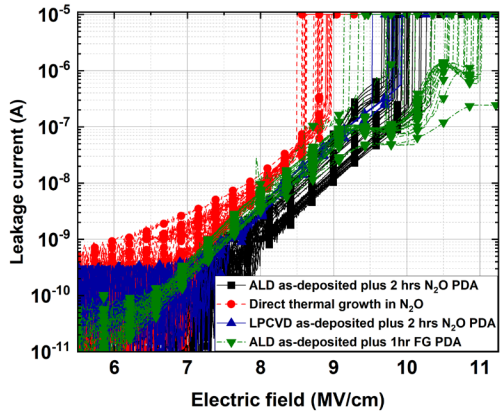
Table 1: Breakdown electric field, fail time as well as breakdown charge 9.6, 9, 8.5 and 8 MV/cm. For this analysis, at least 50 each devices were measured at 175°C. Device area was 7.86×10^{-5} cm^2.

Sample	BV Field (MV/cm)	8 MV/cm	8.5 MV/cm	9 MV/cm	9.6 MV/cm
		$T_{fail,63\%}$ (s)	$T_{fail,63\%}$ (s)	$T_{fail,63\%}$ (s)	$T_{fail,63\%}$ (s)
ALD As-dep. SiO_2	8.58 ± 0.87	-	-	-	-
ALD SiO_2 plus FG-anneal	10.08 ± 0.57	-	-	5,623	1,202
ALD SiO_2 plus N_2O	9.84 ± 0.60	11,220	13,183	4,786	120
LPCVD SiO_2 plus N_2O	8.81 ± 0.14	7,413	8,511	3,715	65
Direct thermal growth	9.50 ± 1.11	5,012	3,981	3,020	75

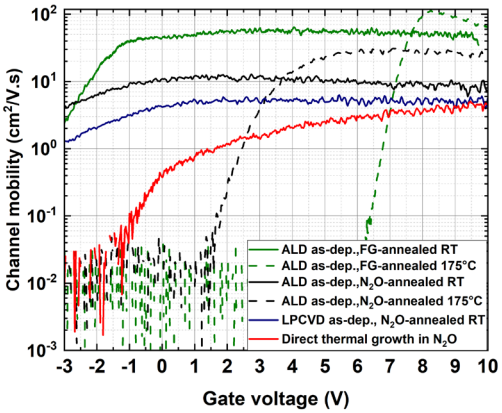
All investigated samples achieve average breakdown fields around 10 MV/cm at 175°C, which demonstrates the excellent oxide quality across the entire dataset, as can be observed in Fig. 2 (a). Here, the FG-treated samples achieve the highest electric breakdown field across the entire dataset,



(a)



(b)



(c)

Fig. 2: Schematic cross section of the fabricated vertical MOSCAP structure (a) using scanning electron microscopy (SEM). The I-V measurements of the investigated samples at 175°C (b) as well as extracted channel mobilities from LMOSFET structures at room temperature and 175°C (c).

once again proving the excellent suitability of this treatment compared to conventional thermal oxidation treatments, which has previously been established to be related to the creation of an oxygen-rich environment near the SiO_2/SiC interface after ALD deposition of SiO_2, in which Si complexes are then broken down into Si dangling bonds by the FG treatment, creating dangling bonds that can then be passivated better [3].

In fact, both ALD oxides that were investigated in this study showed the most promising TDDB performance across the entire dataset, too. Both FG-treated and N_2O-annealed ALD-deposited SiO_2 layers outperform the other two oxides consistently, averaging 5623 s and 4786 s 63% fail time at 9 MV/cm, respectively. For the FG-treatment, this is the equivalent of a 50% improvement when compared to LPCVD-deposited samples. This trend is also true at lower stress levels.

For further analysis of the conduction mechanisms within the oxide layers, the LMOSFET structures were then investigated at room temperature and 175°C, too. Channel lengths were varied

from 150 μm to 15 μm, with representative channel mobility curves being depicted in Fig. 2 (c). The previously established improvement brought about in the ALD-deposited layers can be confirmed in this dataset,too, with the FG-treated LMOSFET structures showing peak field effective mobilities of 65 cm^2/V.s and 108 cm^2/V.s at room temperature and 175°C, respectively. This is an improvement of at least 300-400 percent, compared to all other oxidised device splits, where samples averaged between 10-20 cm^2/V.s, confirming reports about channel mobilities in similarly oxidised structures [7, 8]. The huge improvement brought about by the low-temperature deposition seems to be coming at the expense of an increase in threshold voltage instability at elevated temperatures for the FG-treated samples, an effect which will require further investigation.

Summary

Improvements to ALD as-deposited SiO_2 layers, in terms of breakdown electric field (10.08 MV/cm), TDDB performance (highest $t_{fail,63\%}$ at all investigated electric fields) and channel mobility (60 cm2/V.s and 108 cm2/V.s at room temperature and 175°C, respectively) have been achieved by carrying out a post-deposition anneal in FG-ambient at 1100°C for 1 hour. Even when carrying out a PDA in N2O ambient, reasonable improvements could be achieved when compared to samples which utilized oxides that had been formed in direct oxide growth.

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