Materials Science Forum
ISSN: 1662-9752, Vol. 1090, pp 159-164
doi:10.4028/p-bt3i95

Submitted: 2022-09-03
Revised: 2022-12-16
Accepted: 2022-12-28
Online: 2023-05-31

Hypothesis to Explain Threshold Drift Due to Dynamic Bipolar Gate Stress

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Keywords: 4H-SiC MOSFET, threshold voltage, Vth-drift, Vth-shift, interface traps, ACBTI, GSI.

Abstract. We supply a hypothesis that explains threshold voltage (V_{th}) drift under dynamic bipolar gate stress in SiC-MOSFETs, postulating that ionized donor-like interface traps in the lower half of the bandgap, give rise to an increased internal electric field at each rising edge of a gate voltage pulse. The enhancement of the internal electric field may be viewed as a V_{th} -reduction, and we devised different experiments to assess this V_{th} -reduction. Comparing V_{th} -drift rate using different pulse shapes in dynamic bipolar gate stress tests, we estimated a temporary V_{th} -reduction in the order of 15 V within 200 ns after the rising edge. Measuring the drain-source current peak 200 ns after the rising edge of a rectangular pulse, gives an estimate for the V_{th} -reduction of 5.5 V. To resolve this discrepancy, we postulate that in inversion, positive traps are effectively screened such that the impact on the channel is spatially restricted and smaller than the channel length. Channel current will only flow where positive charges induce a percolation path between drain and source, reducing the apparent V_{th} -reduction in the current based measurement.

Introduction

Dynamic bipolar gate stress for $>10^8$ cycles, typically causes a positive threshold voltage (V_{th}) drift in 4H-SiC MOSFETs beyond the expected drift due to the accumulated total stress time at the positive voltage level [1-4]. For guidelines to measure this form of Vth -drift, see [5]. For applications that require a high number of cycles, it is important to understand the mechanisms behind the V_{th} -drift due to bipolar dynamic gate stress.

An adequate hypothesis for dynamic bipolar gate stress should explain the power law behavior of the V_{th} -drift

$$\Delta V_{th} \propto N_{cyc}^{n} \tag{1}$$

Where N_{cyc} is the number of switching cycles and the exponent n is an experimentally derived value. The graphs in the references [1-3] show that Eq. 1 describes the V_{th} -drift quite well in the range 10^8 - 10^{11} cycles with an exponent in the range between 0.25 and 0.5.

Note that, there are several other names for dynamic bipolar gate stress found in literature e.g., AC-Bias Temperature Instability (AC-BTI), AC gate stress or Gate Switching Instability (GSI). In this paper we denote V_{th} -shift to describe short term changes of V_{th} as seen in hysteresis, due to short-term trapping of electrons and holes, when sweeping gate voltage in a transfer curve in positive and negative direction. We use the term V_{th} -drift to denote the quasi-permanent V_{th} change due to long-term trapping of electrons or holes in the interface or bulk of the gate oxide upon gate voltage stress.

In this paper we will supply a hypothesis that may explain the typical observations and we will try to support the hypothesis using different measurements inspired by this hypothesis.

Experimental Setup

For experimental investigation, we use 0.5 mm² trench-MOSFET's with a 60 nm thick gate insulator made with a process known to be prone to V_{th} -drifting. Measurement of the threshold voltage was done using a Keithley model 2636 source meter to supply a drain voltage of 100 mV

while applying a staircase ramp to the gate electrode to determine the gate source voltage at which the drain source current reaches 1 µA. Bipolar dynamic gate stress was applied using an Agilent function generator model 33220 with the output signal amplified using a Texas Instruments LM7171 operational amplifier on a development board. To determine the drain-source current during bipolar dynamic gate stress we used a small shunt resistor of 10 Ω to convert the current into a voltage signal. Readings of applied gate voltage and shunt voltage drop were done using a Tektronix oscilloscope model TDS3014B and high impedance measurement probes. All measurements shown in this paper were performed at 175 °C.

Hypothesis

Our hypothesis is best understood by considering Fig. 1. Negative gate bias causes hole capturing, or equivalently electron emission from donor like traps at the SiO_2/SiC-interface. As the emission of holes takes time, some holes will remain after switching to positive gate bias. Note that, using the Poisson equation, the electric field profile perpendicular to the interface may be obtained by integrating over the charge distribution. The hole charge will cause a peaking in the electric field at the interface. This will increase both the trapping rate at the interface and the Fowler-Nordheim tunneling probability and subsequent electron trapping in the bulk. At each rising edge and as long as a significant number of holes are not yet emitted, we thus expect an increased V_{th}-drift rate.

As the increased V_{th}-drift rate is effectively based on an increased internal electric field after each rising edge of the pulse, it is now clear how the power law behavior in Eq. 1 may the explained. If we assume that the duration of the excess V_{th}-drift rate is, for example, <500 ns, then the number of rising edges N_{cyc} times the duration of the excess drift rate will result in an effective stress time that scales with N_{cyc} rather than pulse width up to pulses frequencies of 1 MHz, assuming 50% duty cycle.

Another way to view the effect of the increased electric field at the interface after turning the MOSFET on, is to consider that positive interface charge lowers the V_{th}, thereby increasing the overdrive voltage i.e., the difference between V_{th} and the on-state gate voltage.

Note that, as positive charges are effectively screened during inversion, the impact on the electric field or V_{th} is spatially restricted by the Debye length.

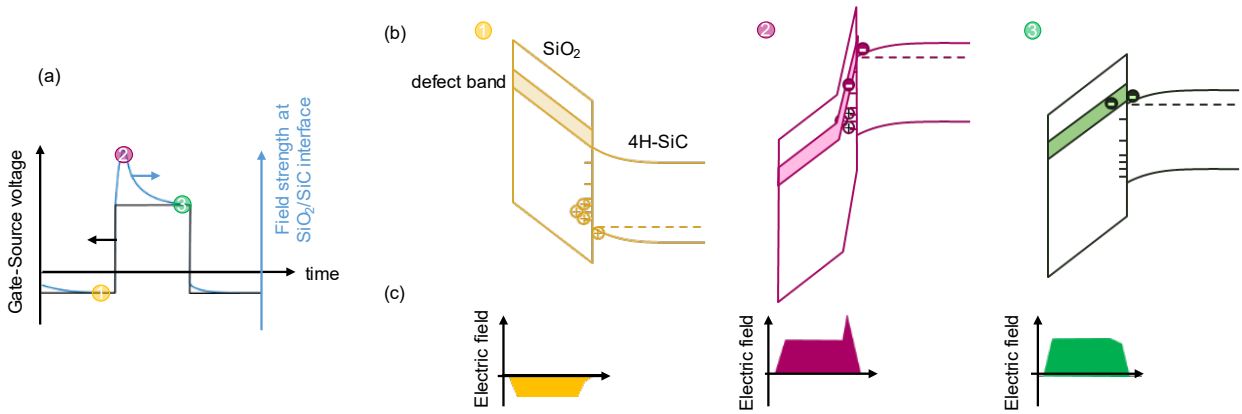

Fig. 1. Schematic representation to show the hypothesis to explain V_{th}-drift due to bipolar dynamic gate stress. (a) Pulse train and estimated electric field strength at the SiO_2/SiC-interface. (b) Band diagrams during different phases (just before the rising edge, just after the falling edge, just before the falling edge) of the pulse. (c) Schematic electric field distributions corresponding to each band diagram.

Maintaining constant trapping rate during high-level phase of the pulse

To test the hypothesis, we devised an experiment with the goal to maintain a constant internal electric field at the interface i.e., constant trapping rate during the high-level of the pulse. We used multi-step pulses, as shown in Fig. 2a for different sets of fresh devices. Preconditioning for each

pulse was -15 V for 1.5 µs. The number of pulses was calculated for each pulse type to obtain 1 h of accumulated high-level duration. Thus, for the measurement using the shortest pulse of ~180 ns, we used 2×10^{10} pulses. Determining V_{th} before and after dynamic bipolar stress resulted in a V_{th}-drift of +200mV for the shortest pulse type. Using another fresh device, we applied two-step pulses with a total width of ~350ns, where the first part of the pulse was identical to the first part of the 180 ns pulse. The second part of the pulse was adjusted in high-level to obtain the same V_{th}-drift of +200 mV after 1h of accumulated high-level time. We found good agreement, when taking a high-level voltage of +27 V for the second part of the two-step pulse. Using yet another set of fresh devices, we designed a three-step pulse in the same manner, giving a third part of the pulse with a high level of +35 V. Finally, we used a 3-step pulse with total width of 10µs and cross-checked that it resulted in roughly similar V_{th}-drift as for the short 3-step pulse. The evolution of the V_{th}-drift due to gate stress using these four different pulse shapes roughly follows a power law with exponent 0.34 when plotted against cumulative high-level time as shown in Fig. 2b.

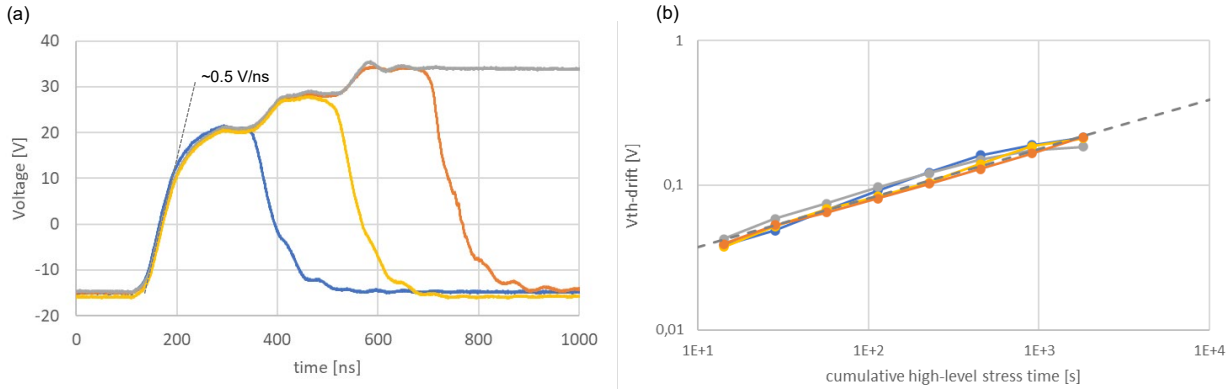

Fig. 2. (a) Pulse shapes adapted to ensure a roughly similar internal electric field during the pulse high level. (b) Threshold voltage drift versus cumulative high-level stress time for dynamic bipolar gate stress using the pulse shapes with corresponding colors shown in figure 2a. The dashed line is a power law with exponent 0.34 used as guide for the eye.

Fig. 3 shows the combination of pulse width and pulse peaks required to obtain the +200 mV V_{th}-drift. Apparently, the average V_{th}-drift rate during the high level of +20 V pulses with ~180 ns pulse width is similar to the V_{th}-drift rate during constant voltage gate stress of +35 V.

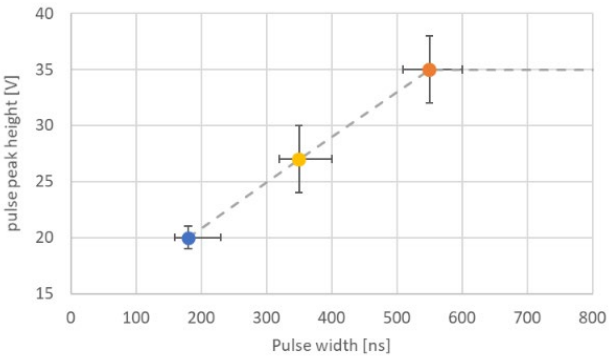

Fig. 3. Gate pulse peak voltage required to obtain a V_{th}-drift of +200 mV after an accumulated stress time of 1h for different pulse widths at 175 °C. Colors correspond to Fig 2. Preconditioning for each pulse was -15 V, 1.5 µs.

V_{th}-shift after negative voltage gate stress

The enhancement of the electric field just after switching to high level should give rise to a temporary reduced V_{th}. We recorded the drain-source current during dynamic bipolar gate stress, with a setup described in the experimental section, to estimate the V_{th} reduction. Fig. 4a shows the recordings for the case where we switched the gate only partially on. With a gate source voltage of +2 V, we obtain a current peak of ~55 mA within the first microsecond. We then increased the pulse high level voltage such to obtain 55 mA of drain-source current after 1ms. We found a high-level voltage of 7.5 V, as shown in Fig. 4b.

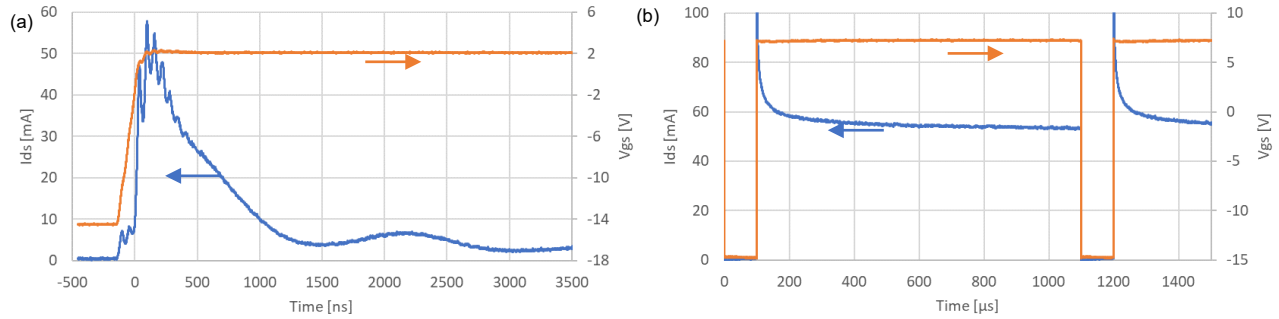

Fig. 4. Measurement of drain-source current at 175 °C after switching the gate partially on. Drain-source current is on the left axis and gate source voltage on the right axis. (a) shows a current peak ~200 ns after switching the gate source voltage from -15 V to +2 V and (b) shows similar drain-source current of 55 mA after 1 ms after switching the gate to 7.5 V.

Assuming that the same drain-source current in each case indicates similar electric field at the interface, we may roughly estimate that the Vth was temporarily reduced by 5.5 V at 200 ns after the start of the high level. We repeated this experiment for different negative gate stress voltages to obtain the Graph in Fig. 5.

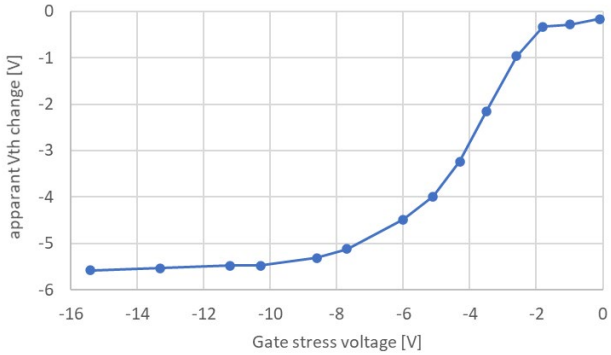

Fig. 5. Measurement of apparent temporary V_{th}-reduction 200 ns after the rising edge of a gate voltage pulse for different applied negative gate voltage stress levels. The high level of the pulse was set at +2 V and preconditioning for each pulse was -15 V for 100 µs.

Discussion

The distance between positive trapped charges at the interface and the inversion layer charge is assumed to be a few nm and therefore only a few percent of the oxide thickness of 60 nm. Neglecting this difference and assuming homogeneously distributed charge across the interface, we may calculate the net interface charge with the equation for a parallel plate capacitor using known gate capacitance and the applied gate voltage.

Fig. 3. showed that the V_{th}-drift rate during high-level at +20V of the 180ns pulses is similar to the V_{th}-drift rate during high-level at +35V of 10µs pulses, suggesting that the electric field perpendicular at the SiO_2/SiC-interface is similar in both cases. Following the hypothesis presented

and assuming we may describe the gate as a parallel plate capacitor, we thus need positive interface charge during the high level of the 180ns pulses corresponding to 15V, to explain the difference in required high-level voltages.

Assuming, that the same amount of positive charge remains after switching to a lower high level, we would expect a temporary V_{th}-reduction of 15V during the first 180ns after switching. V_{th} -measurements using a setup with function generation and oscilloscope showed a much lower V_{th} -reduction of 5.5 V. How to resolve this discrepancy?

Let us consider the screening of positively charged traps during inversion. With typical values for inversion charge density, the Debye length is in the range of nm's and thus much smaller than typical gate lengths. Therefore, the drain-source current is not significantly affected in full inversion. It looks different at depletion/very weak inversion. The electron density is much lower and the charge sheet width much thicker. The positive charges have a much larger radius of impact and may now cause percolation paths or a charge sheet for the drain-source current. Fig. 4a, indicates that during the first 1µs after the rising edge such current path is formed and subsequently destroyed when the traps are neutralized by channel electrons. The long tail of the current peak might be explained by electron trapping and reduction of the inversion layer density due to the V_{th} -increase during the high-level phase.

As said, in full inversion the drain-source current is not significantly affected by the positively charged traps. But positively charged traps will temporary cause a high local electric field or equivalently a low local V_{th} significantly enhancing electron trapping. The electric field from the trapped electrons is not significantly screened in inversion and thus each trapped electron may have a significant radius of impact on the channel current causing an increase of V_{th}. Note, that a typical V_{th} -measurement takes several milliseconds and thus allows inversion layer electrons to neutralize at least a part of the positively charged interface traps.

The aforementioned discrepancy may thus be resolved by considering the spatial distribution of the temporary V_{th} -reduction over the area of the inversion channel. An apparent V_{th} in electron trapping experiments, like in dynamic bipolar gate stress test, is thus a weighted area average of the V_{th} distribution. For experiments based on drain-source current, the apparent V_{th}, is a weighted area average of the percolation paths. As the total area of percolation paths due to positive charges is always smaller than the total area affected by the positive charges, we expect lower apparent V_{th} -reduction in measurements based on drain-source current.

The presented hypothesis helps to design further experiments to better understand V_{th} -drift due to dynamic bipolar gate stress. For example, it is now straightforward to understand that Eq. 1 will not be valid for high frequencies beyond a few MHz because the positively charged interface traps will not be neutralized at the end of the high-level phase. Furthermore, we would expect a strong dependence on switching slope of the rising edge rather than the falling edge. Also, we would expect similar drift rates in additional standard PBTI when using devices pre-stressed to the same V_{th} -drift using different pulse shapes according to the method presented in this paper.

Summary

We presented a hypothesis to explain V_{th} -drift due to dynamic bipolar gate stress in SiC-MOSFETs and devised two different experiments to test the hypothesis.

According to our hypothesis, the root cause for this V_{th} -drift are holes trapped at the SiO_2/SiC-interface, when the gate voltage is negative. After switching the gate into inversion these positively charged traps give rise to an enhanced electric field at the interface causing an increased V_{th} -drift rate. Roughly 200ns after switching into inversion, the trapped holes recombine with the inversion layer electrons eliminating the electric field enhancement.

In a first experiment, we constructed gate voltage pulse shapes of different high-level time that aim to keep the enhanced electric field at the SiO_2/SiC-interface constant during the full duration of the pulse high-level phase. To compensate for the recombination of the trapped holes, the gate voltage is increased accordingly during the course of the high-level phase. We could show that pulses with different high-level time give rise to the same V_{th} -drift if the total cumulative high-level time remains

constant, thus proving that the average V_{th}-drift rate is constant for the constructed gate voltage pulse shapes. To fully compensate for the enhanced electric field due to the trapped holes in this experiment, we required 15 V ± 2 V additional gate voltage, during the first 180ns after switching to high level.

In a second measurement, we recorded with high temporal resolution, the apparent V_{th}-reduction due to the positive trapped interface charge after switching to high-level. We used a high-level voltage of only +2V to avoid a high concentration of inversion layer electrons. This is necessary to keep the screening length such that the impact radius of the trapped positive charges overlap to form a percolation path. The V_{th}-reduction derived from this current-based measurement is -5.5V and much higher than the -15V from the drift-based measurement. This discrepancy is resolved by assuming that even at a gate voltage of +2V, the screening length of the positive charges is much smaller than the channel length, resulting in a reduced source-drain current and thus less V_{th}-reduction.

The basic learning that the paper is suggesting, is that there is no need to make a difference between drift due to constant voltage gate stress and drift due to dynamic bipolar gate stress if one considers the local internal electric field at the SiO_2/SiC-interface, which we believe to be the driving force of the positive V_{th}-drift under dynamic and static gate voltage stress. Dynamic bipolar gate stress is thus more or less equivalent to constant voltage gate stress with a higher gate voltage during the first few 100ns after the rising edge. Or phrased differently, we may 'convert' the switching-based gate stress into a time-based gate stress, where we account for the enhanced internal electrical field due to temporary remaining positive charges after switching to high-level.

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