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Gate Dielectric Current Transport Mechanisms in n-SiC Metal Oxide Semiconductor Capacitor

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Abstract. In this work, the voltage and temperature behavior of gate leakage current transport in SiC/SiO_2 metal oxide semiconductor (MOS) capacitor was investigated. The wide range of gate voltage from -50 to 50V and temperature from 300 to 400 K, respectively uses to study the gate current conduction mechanism. Two dominant gate leakage current transport modes in SiO_2 during strong accumulation with the application of positive bias were caused by Fowler–Nordheim (FN) tunneling and Poole-Frenkel (PF) emission leakage conduction. For positively biased case, FN tunneling in the range of 30-40 V dominates the gate leakage current and Poole–Frenkel conduction attributed beyond 40 V.

Introduction

Owing to its wide bandgap physical properties, silicon carbide (SiC) is a promising semiconductor candidate for high voltage power device applications with an increased voltage and switching frequency operations compared to silicon [1, 2]. However, SiC based metal oxide semiconductor power devices with thermally grown oxide suffer from low quality SiC/SiO_2 interface, which results in low channel mobility and gate oxide reliabilities. Furthermore, this issue is more pronounced in trench MOSFETs as the oxidation growth rate depends on crystalline direction in SiC. Past works have indicated that the complex electrically active bulk and interface trap states in SiO_2 sub-oxide and at SiC/SiO_2 interface, respectively, play significant roles in carrier transport through the gate oxide resulting in the degradation of the oxide lifetime and threshold voltage instability [3,4].

Higher interface traps also affect other issues like long-term degradation of the gate dielectric and the eventual reliability of the ultra-high power (UHP) SiC transistor. Several process tuning have been used to lower the interface traps at the SiC/SiO_2 interface [5,6]. Hence, the study of the gate leakage current transport in SiC/SiO_2 MOS capacitor is of highly practical interests and relevance to understand the reliability and degradation of the gate oxide.

In this work, we explore the conduction mechanism of the gate leakage current in SiC/SiO_2 capacitor using current-voltage (I–V) measurements over a wide temperature range from 300 to 400 K. We also discuss the dominant conduction candidates for the conduction mechanism.

Results and Discussion

The SiC/SiO_2 MOS capacitors were fabricated on a 4º off-cut (0001) Si-face of 4H-SiC with 10μm thick & N-doped (10^{16} cm^{-3}) homo-epilayer deposited on highly doped n-type substrate. Pre-gate surface cleaning was performed via RCA method followed by diluted hydrofluoric acid (DHF)

Fig. 1 (a) Illustration and key process flow of SiC/SiO_2 MOS capacitors fabrication (b) Cross-sectional TEM image of the SiC/SiO_2 MOS capacitor.

dip. SiO_2 layer with a thickness of 50 nm was grown via thermal oxidation at 1350ºC in O_2 for 18 minutes, followed by post-oxidation anneal at 1300ºC in N_2 and NO gas for 30 min. The key process flow is described in Fig.1. After oxidation, the grown oxide was characterized by transmission electron microscopy (TEM) measurements. A 200 nm thick aluminum metal was evaporated on the front side using a shadow mask to create top electrode of the MOS capacitor while blanket metal was deposited on the back surface of substrate to form back contact.

Fig. 1 (b) shows the cross-sectional TEM image of the SiC/SiO_2 MOS capacitor which clearly shows 49 nm thick SiO_2 gate dielectric layer. EDX color mapping profiles in Fig.2(b-d) confirmed the distribution of C, Si & O elements in the SiC/SiO_2 MOS structure layers. Sensitive gate leakage current (I_G) is measured and plotted as a function of V_G as shown in Figs. 2(e) & 2(f) for the forward (accumulation $+V_G$) and reverse (inversion $-V_G$) bias. The substrate terminal is always grounded during forward and reverse measurements. The I_G–V_G measurements in Fig. 2(e) suggested a possible FN tunnelling signature starting after 25V in forward bias mode. To check conduction mechanism, the I–V curve with different temperature is typically plotted as $\log(I/V^2)$ versus 1/V and $\log(I/V)$ versus $(V)^{1/2}$, as shown in Fig. 3 (c) and (d).

To understand the conduction mechanism in this SiC/SiO_2 MOS capacitor, we performed a temperature dependent characterization of I_G from 300K to 400K as shown in Fig. 3(a)-3(b). Two distinct modes were identified in Fig. 3(a) – Region-I: temperature dependent I_G variation is fairly weak at gate voltage range ($30V < V_G < 40V$) and Region-II: I_G variation with temperature is very strong at gate voltage range ($V_G \geq \sim 42V$). These I_G–V_G data in regions I & II were further analyzed

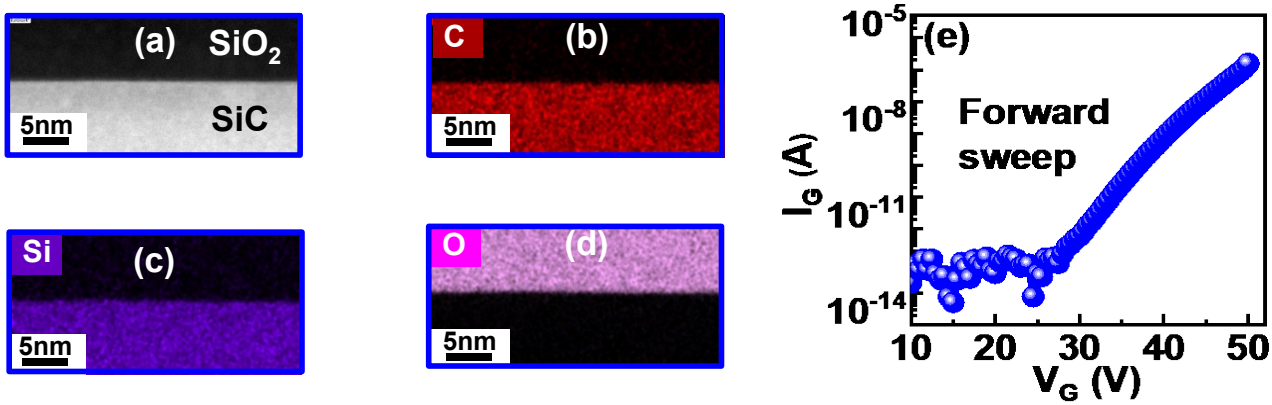

Fig. 2. (a) HRTEM image of SiC/SiO_2 interface (b-d) STEM-EDX elemental mapping confirming the elemental C, Si & O composition (e)-(f) forward and reverse sweep of I_G -V_G for the SiC/SiO_2 MOS capacitors.

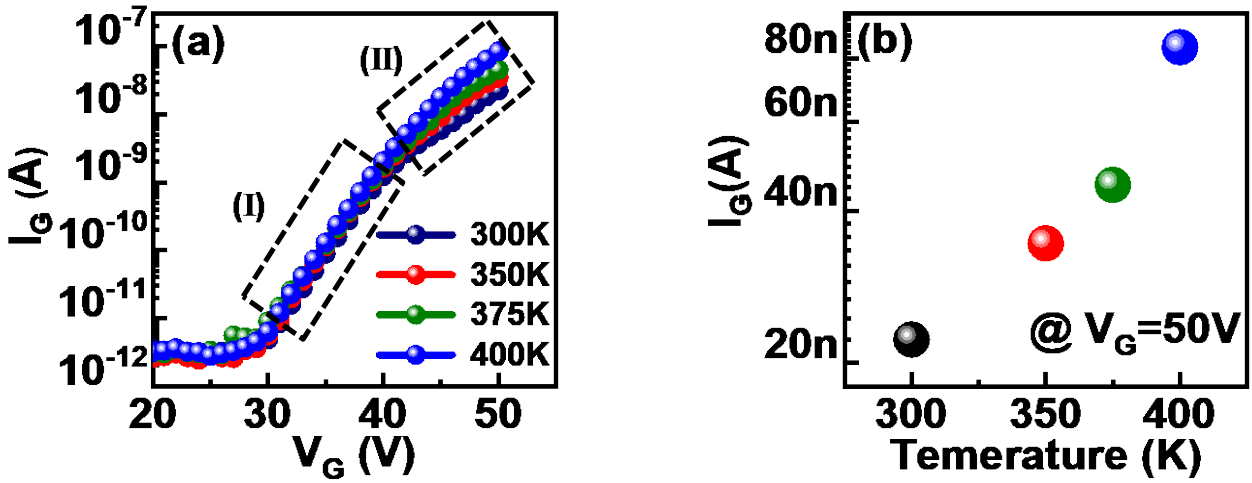

Fig. 3 (a) Forward sweep of I_G -V_G for the SiC/SiO_2 MOS capacitor measured at different temperatures exhibiting two distinct regions I & II, (b) I_G @50V for SiC/SiO_2 MOS capacitor measured at different temperature.

by replotting them into log(I_G/V_G^2) versus 1/V_G and log(I_G/V_G) versus $V_G^{1/2}$, respectively, as shown in Fig. 4 (a) & 4(b). In Fig. 4(a), the region-I replotted results (30V< V_G < 40V) clearly showed four straight overlapping lines with a common negative slope at different temperature over 30V< V_G < 40V. The results indicated the dominant gate oxide conduction mechanism is due to the FN tunneling of surface electrons from the SiC layer quantum mechanically injected into SiO_2 through the triangular energy barrier at the SiC/SiO_2 interface [7]. In Fig. 4(a), the region-II replotted results (V_G ≥ +42V) showed parallel upward shift of the four fitting curves corresponding to temperature increases from 300K to 400K which confirmed the thermally sensitive Poole-Frenkel "traps-hopping" events dominates the transport of thermal electrons in SiO_2 [8,9].

When the applied positive gate bias increases from 25V to 40V, the electrons from n-type epi SiC (doing concentration 1×10^{16}/cm3) accumulate more at SiO_2/SiC interface as a result the corresponding energy band shows more bending in Fig. 5(b). This concept is similar to the conduction mechanism of a MIM tunnel diode, in which the electrons from the metal can tunnel into the insulator film whereas hole injection probability is negligible [6]. Therefore, the conductive mechanism is dominated by FN tunneling in step (I) in Fig. 3(a). When the voltage is increased 40 to 50V as shown Fig. 5(c), the trapped electrons can enter the oxide's quasi-conduction band by the Poole- Frenkel

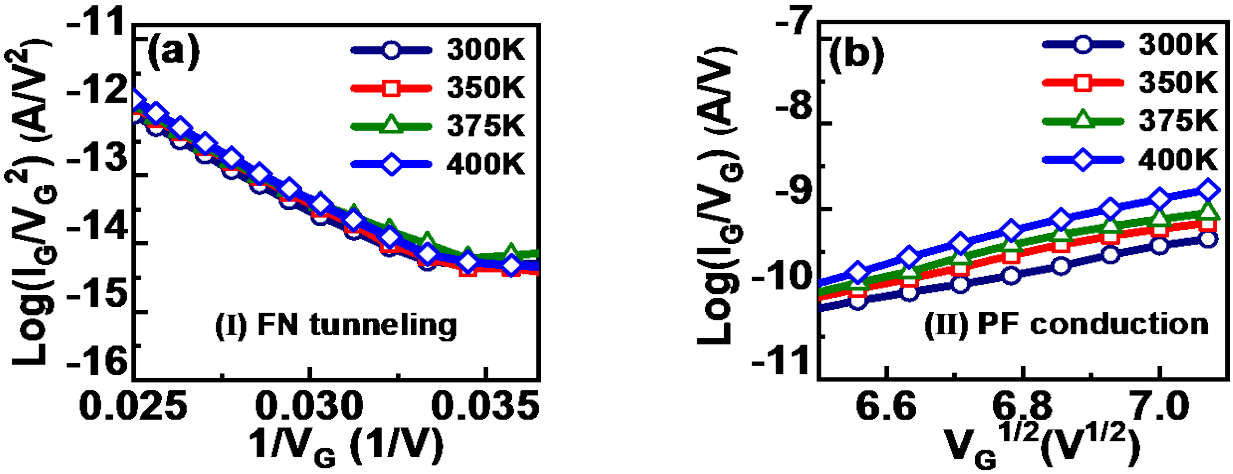

Fig. 4 (a) FN tunneling curve fitting for region-I; and (b) PF conduction curve fitting for region-II.

mechanism and flow from the oxide across the SiC/SiO_2 interface into the SiC conduction band edge. The Poole-Frenkel effect can be observed at the high electric field.

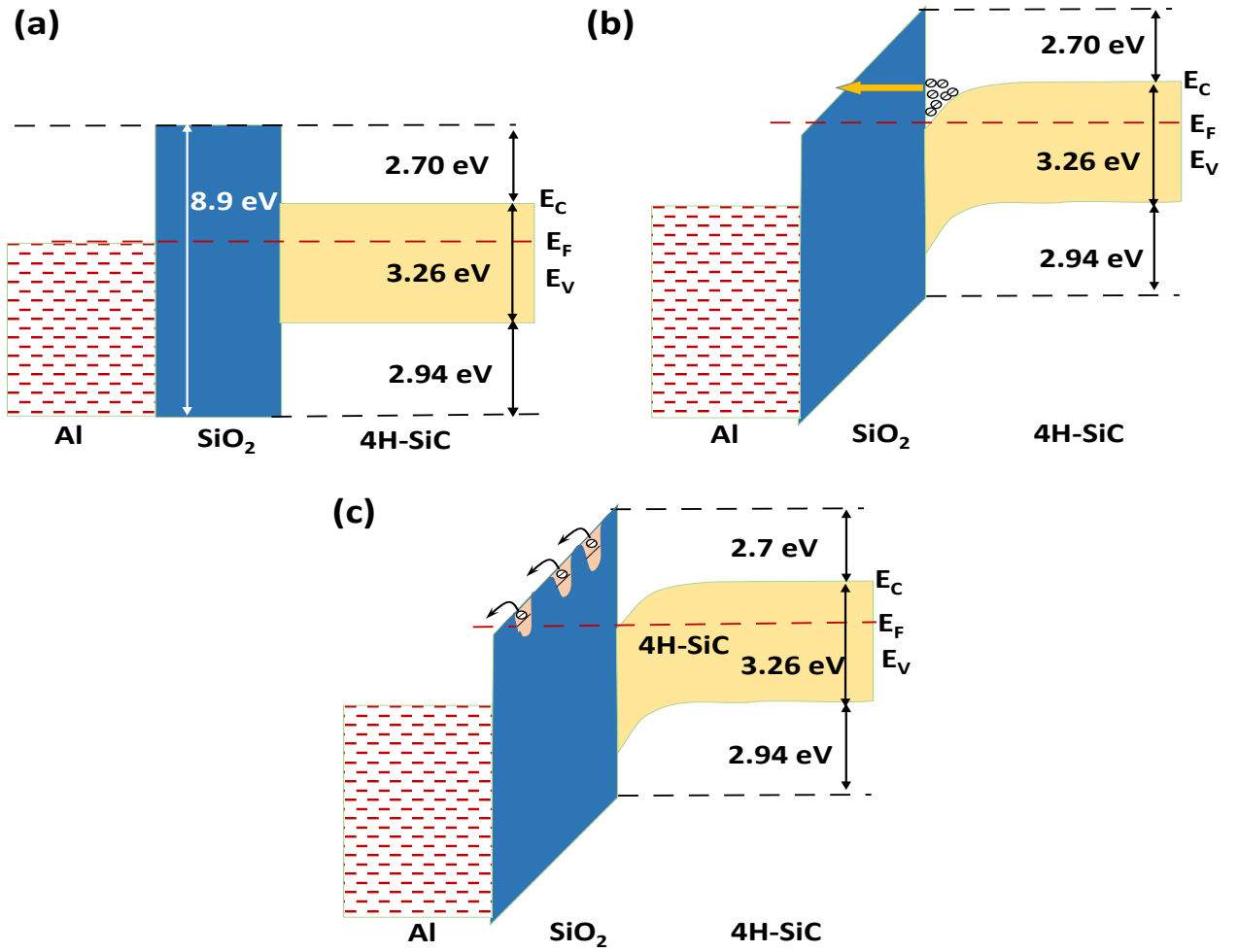

Fig. 5 Energy band diagram of SiC/SiO_2 MOS capacitor device at (a) flatband; (b) region-I Fowler-Nordheim tunneling under a positive gate voltage (20-40V); and (c) region-II Poole-Frenkel 'trap-hopping' conduction under higher positive gate voltage (>40).

Summary

In this work, we experimentally confirmed two dominant gate current transport mechanisms in 50nm thick SiO_2 using a combination of SiC/SiO_2 MOS capacitors and temperature dependent I_G-V_G analysis. The electrical characteristics over a wide temperature range from 300 to 400 K indicate that the gate leakage current flows as the sum of the FN and PF leakage currents. The outcome of this work is relevant for a better understanding of the gate oxide degradation mechanisms and the associated reliability qualification (TDDB, Q_{BD}) of SiC based ultra-high-voltage power transistor.

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