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Physical Modelling of Charge Trapping Effects in SiC MOSFETs

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Abstract. In the recent past, lots of efforts have been put into further developing SiC power MOSFETs. In addition to optimization of device geometry, i.e., vertical device structure, various post-oxidation anneals have been studied to improve carrier mobility by reducing trap density. Nevertheless, a considerable number of traps remain, which are the central origin for dynamic changes in the threshold voltage of up to several volts during DC and AC operation. To explain the threshold voltage instability, an effective two-state defect model has been recently applied. In this work, we give an overview of modeling efforts to explain the impact of defects on the device threshold voltage and discuss the hysteresis of voltage sweep and bias temperature instabilities in SiC transistors. Based on the combination of measurements and computer simulations, a list of potential defect candidates responsible for the observed threshold voltage instabilities is discussed.

Introduction

Metal-oxide semiconductor transistors (MOSFETs) made on 4H-SiC substrates exhibit superior properties, such as high blocking voltage capabilities, high thermal conductivity, etc., making them excellent devices in high-power switching applications. In the past, lots of efforts have been put into improving the performance of SiC transistors, initially focusing on lateral device structures. Nowadays, state-of-the-art SiC power MOSFETs often use a trench design, shown in Figure 1. This vertical device

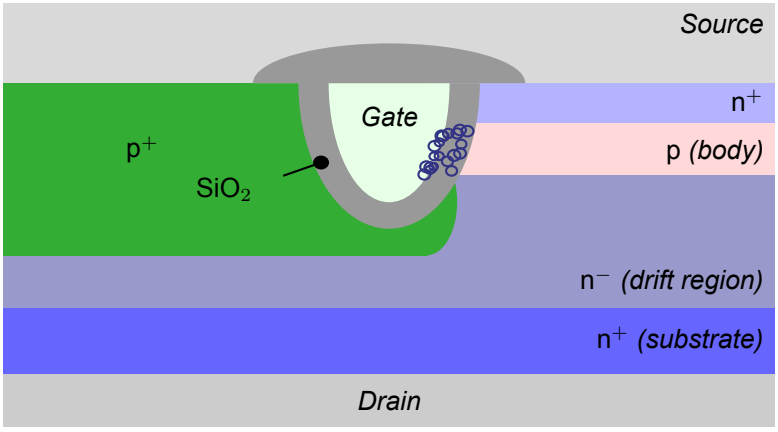

Fig. 1: The cross-section of a vertical transistor, i.e., trench MOSFET, is shown. Electrically active defects can exist at the interface between the p-body and the insulator (blue circles). Furthermore, these defects can also be located inside the insulator. Note that charge trapping at these defects can seriously affect the device's behavior during operation.

architecture has the advantage of having a high blocking voltage and comparable small on-resistance, maintaining a small chip area compared to lateral device structures [1, 2]. Besides these major advantages, vertical SiC MOSFETs exhibit higher carrier mobility due to reduced trap density in the

vicinity of the conduction band edge but larger defect densities within the SiC bandgap [3] compared to, e.g., DMOS architectures. To passivate as many of these defects as possible, various post-oxidation anneals [4, 5] have been studied in the past, i.e., in a NO [6] or NH_3 [7] enriched ambient. But still, a considerable number of traps remain, which are the central origin for dynamic changes in the threshold voltage of up to several volts during operation [8–10]. Note that in power conversion applications, which is considered the primary application for SiC devices, changes in the threshold voltage can be compensated by an increased gate overdrive bias. Nonetheless, the physical understanding and modeling of the defects and their impact on the devices are vital to enable studying device performance degradation and its impact on the behavior of circuits already during the development phase of an application [11, 12].

Modeling of the Impact of Defects on the Device Threshold Voltage

The defects located along the channel, i.e., at the interface between the SiC/SiO_2 or directly in the insulator, can capture and emit a charge carrier and thus affect the channel mobility and threshold voltage [13]. Furthermore, the defects may also give rise to trap-assisted tunneling currents [14, 15]. In order to describe charge trapping, models based on mathematical formulas, e.g., power-law-like expressions, are regularly used as they provide a simple way to replicate experimental data. But it has to be pointed out that such models cannot account for the complex behavior of charge trapping and typically lack accuracy. Such expressions, for instance, cannot explain the saturation of ΔV_{th} with increasing stress time. Another approach uses the SRH model extended by a tunneling factor (which can be calculated using the WKB approximation) to mimic the trapping kinetics of oxide and interface defects [16]. However, the SRH traps cannot account for the strong temperature activation of charge trapping [17]. An example where this is important is that at higher temperatures, the degradation is apparently lower than at lower temperatures, which is counter-intuitive [18]. Furthermore, the tunneling probability depends on the trap depth, and especially in devices with thin oxides, the transition times estimated by the model are too fast to be able to explain the slowly recovering drifts of the threshold voltage [19].

To model the charge transfer kinetics to and from a defect, an effective two-state defect model, c.f. Figure 2, which is based on the non-radiative multiphonon theory, has been established for Si technology [16, 20, 21] as well as for SiC devices [22] in the recent past. The physical defect model calculates the charge trapping dynamics of each of the defects considering a two-state system. Defect state 1 accounts for the situation where the carrier is in the carrier reservoir, i.e., the conduction band edge, while defect state 2 describes the case where the carrier is trapped at the defect site. The transitions between the two states are calculated using potential energy surfaces. In the classical limit, a transition occurs when a charge carrier overcomes the energy barrier between the minima of the parabola and the intersection point of the curves. In equilibrium, the defect state which exhibits the lowest energy is the favorable location of the carrier, as can be further seen in Figure 2 the relative energetic position of the defect in the insulator and the carrier reservoir changes when a gate bias is applied at the transistor. For instance, a positive gate bias, as is applied when a SiC device is turned on, lowers the energetic position of the trap level w.r.t. the conduction band edge, and thus a defect can be come charged very likely. When the gate bias is removed, the trap level is shifted back above the conduction band edge, and the defect can emit its charge. Note that this model has to be solved for a large ensemble of oxide defects to mimic the experimentally observed ΔV_{th} degradation. With this model in hand, for instance, the hysteresis of the threshold voltage, which can be observed when consecutive up- and down-sweeps during IV measurements are performed, can be explained [23].

Hysteresis of Voltage Sweeps

To verify the functionality of a transistor IDVG measurements are typically performed where a constant bias is applied at the drain while the gate bias is swept from a low-level to a high-level bias,

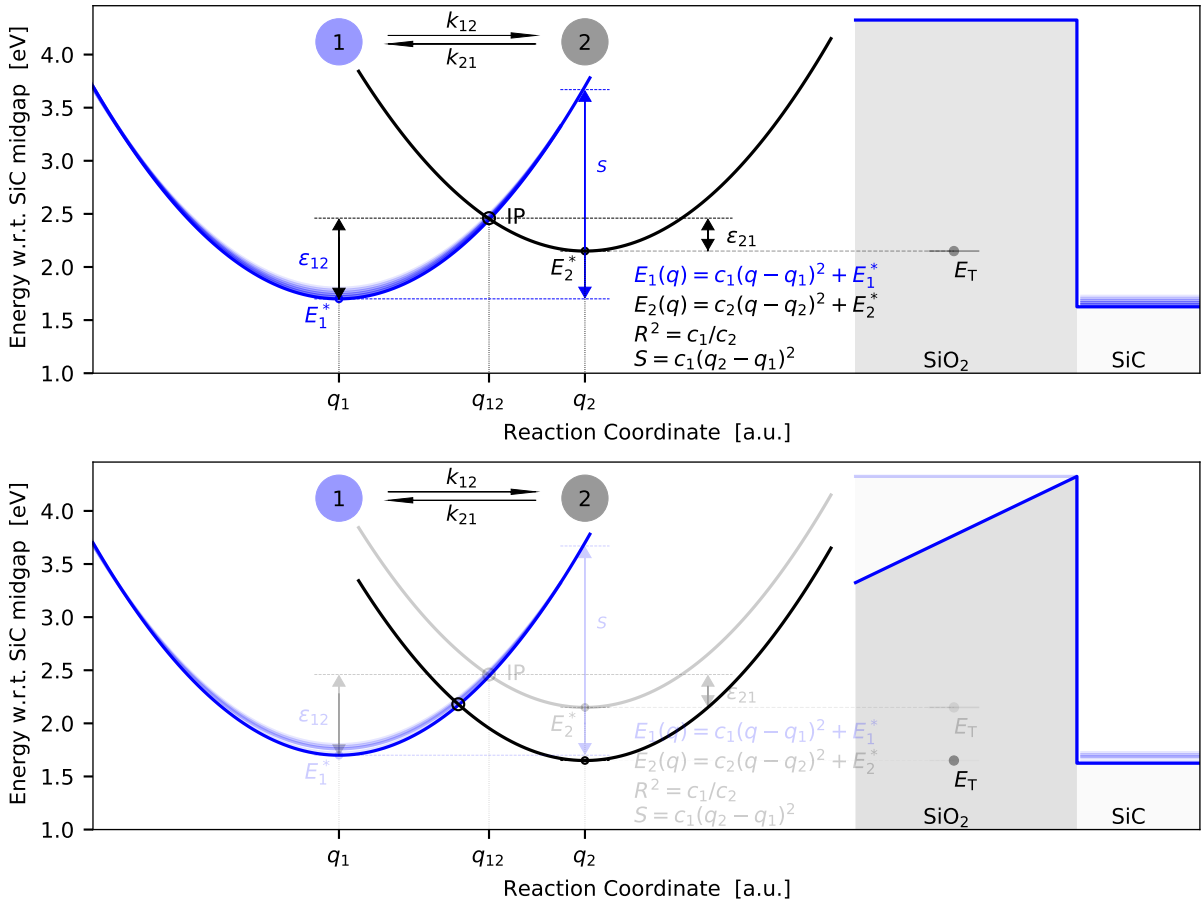

Fig. 2: An effective two-state defect model can describe the charge transfer between a carrier reservoir and the trap. **(top)** When the trap level of a defect given by E_T (in the model considered as E_2^*), is above the energetic level of the carrier reservoir, i.e., conduction band edge of SiC represented by E_1^*, the energetically favorable position of the charge carrier is in the channel. Thus, the trap remains neutral. **(bottom)** However, in the case a bias is applied at the gate of the transistor, the energetic position of E_T can be shifted below the conduction band edge, i.e., $E_2^* < E_1^*$. Now a charge carrier can overcome the energetic barrier given by the intersection point (IP), and the defect may become negatively charged.

in the case of an nMOS transistor. In a non-distorted device, the repetitive measurements of IDVG characteristics should lead to the same characteristics. Similar is the situation for measurements where consecutive up-sweep and down-sweep of the gate bias are performed. However, it can be observed that the up-sweep and the down-sweep do not follow the same path, and a so-called hysteresis of voltage sweeps can be observed. The width of the hysteresis becomes even more pronounced for technologies that exhibit an apparent trap density and can be explained as follows: During the up-sweep, the trap level of a certain number of defects becomes shifted below the Fermi level of the channel, and thus the defects can become charged. During the down-sweep, not all defects emit their charge, e.g., if their transition time is longer than the sweep rate. Thus several defects remain charged, leading to a change in the device's threshold voltage, which can be observed as the hysteresis effect. Interestingly, the hysteresis width depends not only on the sweep rate but also on the device temperature and the gate bias levels used for the experiment. As can be seen from Figure 3, the V_{th} hysteresis increases with decreasing low level of the gate bias [13]. This is consistent with the trap bands from Figure 3 as at lower bias, more traps located close to the valence band edge can trap a hole during the down-sweep, which is detrapped during the up-sweep, and by doing so contribute to the measurement signal.

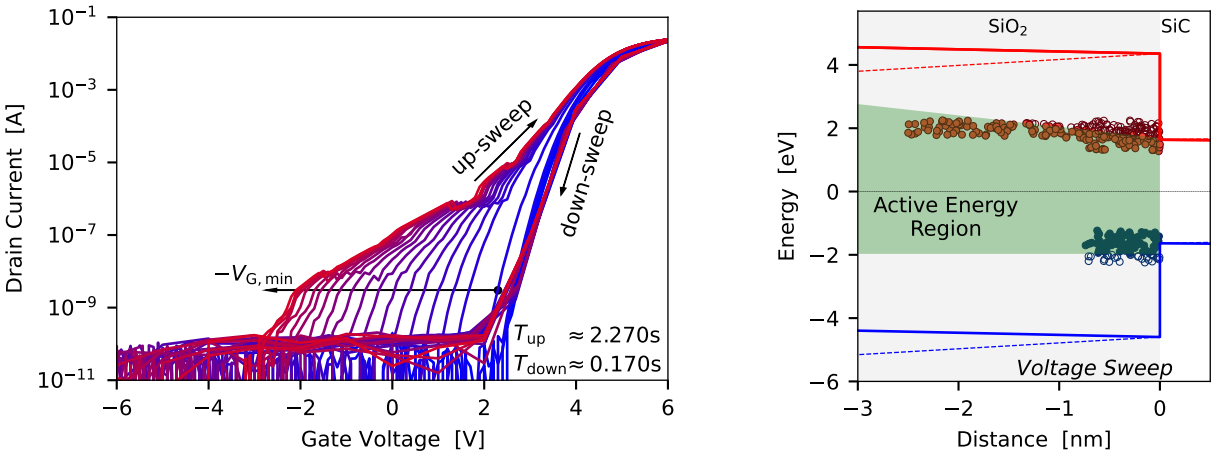

Fig. 3: (**left**) A clear hysteresis can be observed when consecutive up-sweeps and down-sweeps of the gate bias are performed. Quite interestingly, the hysteresis width increases with decreasing low-level bias. (**right**) Due to an increased gate bias range, the active energy region for charge trapping also increases, and thus, a larger number of defects can contribute to the measurement signal.

As discussed in the next section, the proposed trap bands are consistent with observing a drift of the threshold voltage when bias temperature instabilities are investigated.

Bias Temperature Instabilities

A second prominent reliability issue is the so-called bias temperature instability (BTI), which refers to the drift of the threshold voltage over time. BTI is typically explored by applying an extended measure-stress-measure (eMSM) scheme [24], shown in Figure 4. Note that in order to perform ultrafast eMSM

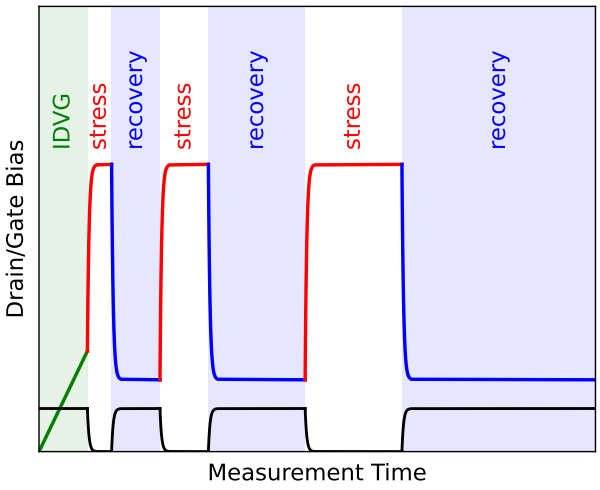

Fig. 4: The electrical measurements are often based on the measure-stress-measure (MSM) scheme. Here an initial IDVG is recorded, and afterward, consecutive stress/recovery sequences with increasing stress and recovery time are performed. The marked areas represent the parts of measurement where data points are recorded. As no drain bias is applied during the stress phase, no information about the change of the threshold voltage will be available. It must be noted that precise timing, especially for the bias transitions, is mandatory to replicate the applied bias as precisely as possible during the simulations.

measurements, advanced measurement tools are required [25, 26]. This is because the measurement delay is a critical parameter for the characterization of SiC MOSFETs [27]. As an example, a reduction of the sweep time for IV sweeps from 1 s to 20 µs leads to an increase of the measured V_{th} by a

factor of four [10]. Also, consideration of the device history is essential for the correct replication of the experimental data by theoretical simulations. Thus a pristine device has to be used when a new eMSM measurement series is started. An eMSM sequence consists of repeatedly applied stress and recovery cycles with increasing stress and recovery time, while the device temperature and bias levels are kept unchanged. During the recovery phase of such an eMSM sequence, the measurement data is recorded, converted to an equivalent drift of the V_{th}, and then employed to extract the corresponding trap distribution using our open-source reliability simulator Comphy [20]. As highlighted in Figure 5, the experimental data can be nicely explained using Comphy [20, 28], which leads to the defect bands from Figure 3 (right). So far, the DC stress eMSM case has been discussed. However, AC gate bias

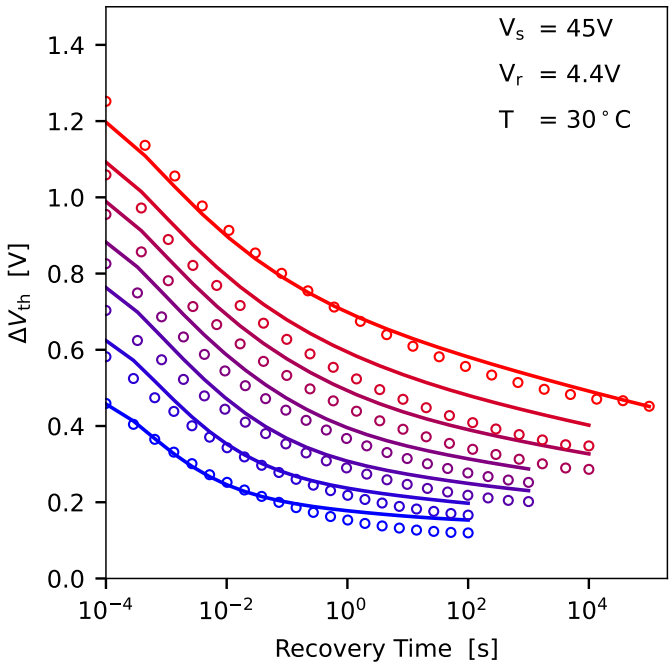

Fig. 5: The experimental DC-MSM data can be nicely replicated with the two-state defect model considering the trap ensemble shown in Figure 3 (left).

signals are more likely applied under regular device operation. Thus an AC stress pattern has been applied to the device, and the corresponding ΔV_{th} has been extracted [18] and modeled using Comphy [22]. It has to be emphasized that both DC and AC device operation can be explained with the same set of trap parameters which is a strong indicator of the accuracy of the two-state defect model employed.

Conclusion

Finally, based on the calibration of the simulations, one may link the model parameters to specific trap candidates. However, for the SiC material system, there is a large variety of potential trap candidates available, see Figure 6, that might contribute to charge trapping [9]. Interestingly, defects like polarons have been identified to likely lead to trap-assisted tunneling currents [15, 22], while BTI is likely caused by defects exhibiting larger relaxation energies, e.g., oxygen vacancies [29].

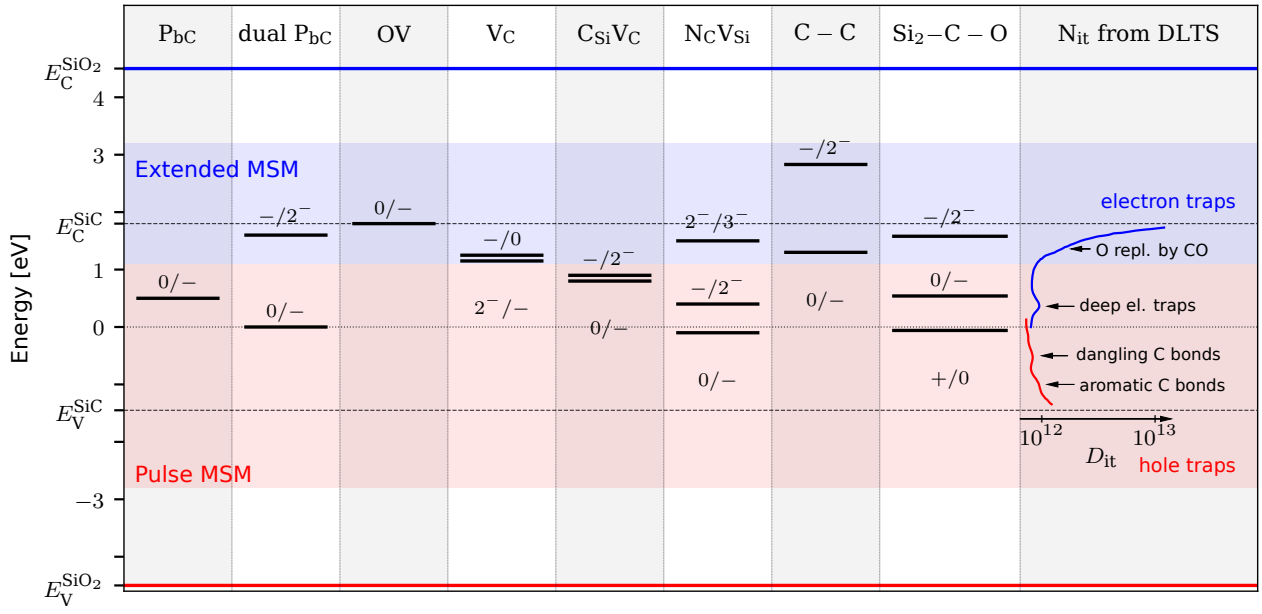

Fig. 6: A long list of defect candidates (excerpt) has been proposed in the literature, which exhibits a charge transition level (CTL) within the active energy regions for charge trapping that are accessed during experiments and operation. By varying the high-level and low-level gate bias range used for MSM measurements, the energetic region of defects that influence the measurement signal can be altered.

Acknowledgment

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