Materials Science Forum
ISSN: 1662-9752, Vol. 1090, pp 93-100
doi:10.4028/p-3w3s88

Submitted: 2022-08-26
Accepted: 2022-11-11
Online: 2023-05-31

Outlook for Dielectric/SiC Interfaces for Future Generation MOSFETs

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Keywords: metal-oxide-semiconductor, interface, channel mobility, dielectrics.

Abstract. Silicon carbide (SiC) metal-oxide semiconductor (MOS) power devices such as metal-oxide semiconductor field-effect transistors (MOSFETs) require a stable and low defect-density interface, and a high-quality dielectric, for good device performance and reliability. Notably, the interface and dielectric properties determine the threshold voltage stability, the field-effect channel mobility, and the device lifetime as limited by dielectric breakdown in both the forward on-state and reverse blocking conditions. Here we discuss the present state of SiC MOS processing and properties and point to directions for future development. Important items to address are: 1) interface passivation approaches; 2) dielectrics; 3) device design; and 4) in-depth measurements of the interface quality and reliability.

Introduction

The present state-of-the-art MOS interface for SiC power devices consists of thermally grown SiO_2 with a nitric oxide (NO) post-anneal on Si-face (0001) 4H-SiC (tilted off-axis ~4° in the [11-20] direction). This provides a stable nitrogen passivation layer [1] and good dielectric reliability [2], but with a remaining high density of interface traps (D_{IT}) near the conduction band, about two orders of magnitude higher than for Si MOS devices. Thus, the channel current is lower than the material limits [3, 4], and the threshold stability, while usable, has room for improvement. Although the channel mobility on a trench MOSFET device (a-face {11-20} or m-face {1-100}) is typically higher than that of the Si-face [5, 6] indicative of lower traps levels as shown in Fig. 1, room for improvement remains with respect to a-face or m-face interfaces due to the remaining traps contributing to threshold shift and hysteresis [6, 7]. Informative reviews of SiO_2/SiC MOS interface issues are found in Lui et al. [8] and Kimoto and Watanabe [3].

Improvements to the interface to lower trap levels and get closer to an ideal interface would bring improvements to the overall device performance; some of these are listed in table I. Note that higher mobility typically is tied to lower interface trap levels (density (D_{IT} traps/(eV*cm^2)) or total number (N_{IT}, traps/cm^2)); although mobility could be enhanced by other things as well, such as reduced interface roughness or reduced number of near-interface (oxide) traps (NIT or NIOT). Regardless, any performance benefit must come without a penalty in reliability or drift; this is the main challenge for competing processes which aim to replace the NO passivation approach. A list of relevant reliability issues to consider are listed in Table II.

Table I. List of performance benefits that a higher mobility or lower defect density would enable.

Improvement	Enabled by:
Lower on-resistance $R_{on,sp}$	High mobility
Lower $R_{on,sp}$ and improved V_T stability	Lower near-interface oxide traps (NIT or NIOT), or interface trap reduction (N_{IT}/D_{IT})
Improved Gate reliability	Relaxed gate field enabled by high mobility
Minimized short channel effects	Longer channel can be utilized with higher mobility
Longer short circuit withstand time	Channel saturation due to low N_{IT}/D_{IT} and longer channel

Table II. List of reliability issues linked to the MOS dielectric and interface passivation, also considering alternative high-k gate dielectric materials.

Reliability Issue	Concern:
Gate leakage (leading to device degradation)	-Interface elements inter-diffusing with dielectric -crystalline microstructure, defects/traps, and smaller band offsets
Gate dielectric breakdown in the on-state	-Interface elements or gate electrode inter-diffusion with dielectric -Smaller band offsets, more Fowler-Nordhiem tunneling -Breakdown field of alternative dielectrics (lower than that of SiO_2)
Threshold instability	Fixed dielectric charge, near-interface charge, interface bonding stability between dielectric and SiC
Gate integrity in blocking mode	Carrier injection and field effects on dielectric integrity, especially if barrier heights are lower

Whatever the solution for improved interface and channel properties, it will require finding the right materials and processing approaches which will allow them to be integrated into the gate processing module; for example, it may require a 'gate-last' approach such as done with high-k on Si solutions. Some solutions may be effective for the polar Si-face (0001) or C-face (000-1) channels, and others may be effective for the non-polar faces such as the a-face {11-20} or m-face {1-100} family of planes. Thus device design plays a role here that cannot be ignored.

The issue of SiC MOS channel and interface properties has been somewhat obscured by the way channel mobility has been reported. To give a clear indication of the channel current capability, the most straightforward approach is to report the field-effect mobility (μ_{FE}) [9],

$$\mu_{FE} = \left(\frac{L}{W}\right) * \left(\frac{1}{C_{ox} * V_D}\right) * \left(\frac{dI_D}{dV_G}\right) \quad (1)$$

where L and W are the channel length and width, V_D is the drain bias, Cox is the oxide capacitance per unit area, and dI_G/dV_G is the transconductance (g_m). Although this is the clearest way to present the channel electrical properties, this does not help reveal the mobility limiting mechanisms. Presently, it is understood [9, 10] that a low field-effect mobility is due to either: 1) reduced free charge in the channel due to trapped charge (which will lower the μ_{FE} value); or 2) due to the typical mobility-limiting factors of phonon scattering (μ_{PH}), coulomb scattering (μ_C), or surface roughness (μ_{SR}). These can be expressed using Matthiesson's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_B} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} \quad (2)$$

where μ_B is the bulk mobility and μ is the overall electron inversion-layer mobility. To understand the electrical properties of the channel most completely, measurements to separate out the various mobility limiting effects would ideally be performed, as in a number of reports [4, 10-13].

Interface Passivation

Alternative passivation approaches remain a potential way to improve channel mobility. It has been shown that for planar channel MOSFETs on Si-face, alternate interface passivation approaches with elements such as P [14], Ba or Sr [15, 16], or La [17] can increase the channel mobility. Shown in Fig. 2 are results for Ba passivation and a deposited SiO_2, compared to a standard thermal oxide and NO anneal [15]. It was observed by high-low C-V that the density of interface traps (D_{IT}) was reduced by the Ba passivation, and the temperature dependence of the μ_{FE} showed minimal coulomb scattering effects. A recent report has shown that the free carrier density is increased with this Ba

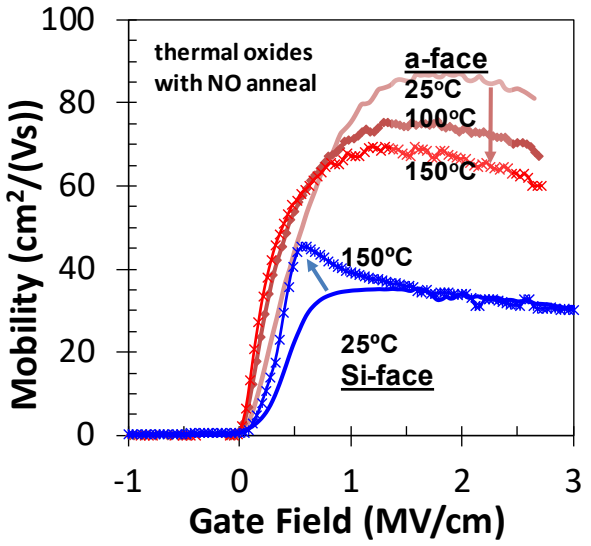

Fig. 1. Mobility comparison of ~5E15 Al-doped Si-face and 1E16 doped a-face planar SiC MOSFETs with a thermal oxide and NO passivation [6].

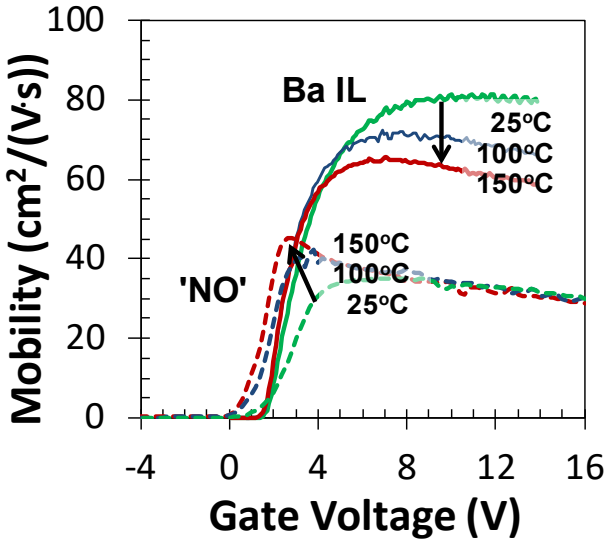

Fig. 2. Mobility comparison of ~5E15 Al-doped Si-face planar SiC MOSFETs with either NO or Ba passivation [15].

passivation process [18], which agrees with the previous findings of lower D_{IT} levels. However, the gate oxide and threshold reliability have been shown to worsen if these are used with a SiO_2 dielectric. However, these approaches have proven that an improved MOS channel performance on Si-face 4H-SiC is possible.

Future work to improve these approaches requires methods to ensure that these elements do not diffuse into the gate dielectric. Potential solutions consist of: 1) better methods of forming/depositing the passivation layer; or 2) using an alternative dielectric layer which serves as a diffusion barrier to that element. In the ideal case, the alternative higher-k dielectric would have a chemical compatibility with SiC such that an additional interface passivation would not be needed. Various approaches are shown schematically in Fig. 3. Approaches (a) (standard NO and $POCl_3$ [14] approaches) and (b) (for Ba, Sr [15,16] and La [17]) have been demonstrated; but an approach such as (c) with a dielectric diffusion barrier to the IL may be needed to allow new approaches to have good reliability. In Fig. 3(c), the first dielectric is a diffusion barrier to the IL element; the 2nd optional dielectric is needed if the properties of the first layer are not sufficient for reliability. As shown in Fig. 3(d), an epitaxial dielectric could be utilized (with or without an interface passivation layer) that would provide a low defect level, lattice-matched interface.

In addition, attempts to improve the present gate stack of SiO_2 with a N passivation (variations of process (a)) are also being actively investigated. The use a hydrogen anneal to etch/treat the surface before depositing SiO_2 and annealing in NO has shown real promise [19] on Si-face SiC, doubling the channel mobility compared to the standard thermal oxide plus NO anneal process. This needs to be studied in detail to confirm that gate quality and threshold stability is not compromised. Additional processes such as very high temperature N_2 anneals to reduce D_{IT} levels and reduce V_T hysteresis [19, 20] also may be promising directions to continue to study.

Finally, interface structure and properties can be elucidated using modeling approaches such as Monte-Carlo methods [11] or atomistic modeling approaches [21, 22]. Modeling results can often help direct or bring a more complete understanding to ongoing research efforts, and ultimately experimental and modeling results would show agreement.

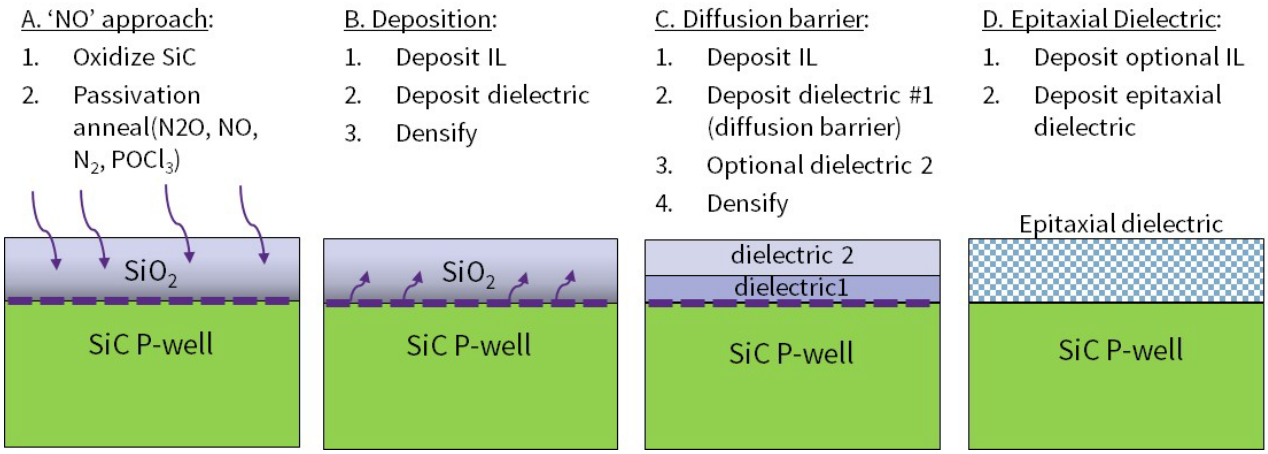

Fig. 3. MOS processing approaches for interface passivation application. Approach (a) is the standard approach; (b) has been used for Ba, Sr [15,16] and La [17]; (c) or (d) may ultimately be needed to achieve new interface properties. The H_2 anneal approach [19] is a variant of (a).

Dielectrics

Transitioning away from SiO_2 to alternative dielectrics is another potential solution for achieving improved channel properties. As learned by the Silicon device community, high-k dielectric materials selection must take into account thermodynamic stability between semiconductor and dielectric [15], and electrical properties such as dielectric constant [23, 24], band offsets [25, 26], dielectric breakdown strength [27], and related materials properties; these relate not only to performance but to reliability concerns as well. Dielectrics on SiC need a bandgap much wider than is acceptable on Si, due to the wider bandgap of SiC compared to Si. Besides the materials properties listed, the alternative dielectric should satisfy these main conditions: 1) form an interface with low trap densities (or be a diffusion barrier for passivation elements); 2) have appropriate band offsets to minimize Fowler-Nordheim tunneling; 3) remain amorphous or not have high defect density (within grains or at grain boundaries); 4) be stable under the processing conditions required for MOSFET fabrication; and 5) display low failure rates relating to time-dependent dielectric breakdown (TDDB) and threshold instability.

Ideally, for SiC with a bandgap Eg ~3.25eV, an appropriate MOS dielectric would have an Eg >7eV (example materials listed in [23, 24]) with aligned band offsets to block current flow under positive and negative gate or drain bias. Materials which have been investigated as dielectrics on SiC include Al_2O_3 [28], HfAlO [26], HfAlON [29]; related silicates and lanthanides also deserve investigation [30].

The main advantages offered by high-k dielectrics, presuming an equivalent or superior interface with SiC, are that: A) the high-k dielectric provides a higher channel charge (scaled by the dielectric constant ratio $k_{high\text{-}k}/k_{SiO2}$) for the same gate thickness and bias (as shown in Fig. 4); and B) in high-drain bias blocking mode the field on the high-k dielectric will be lower than the SiO_2 field would be, as the dielectric field (E_{ox} or E_{diel}) equals the semiconductor field (E_{SiC}) multiplied by the ratio of the dielectric constants of SiC and the dielectric (k_{SiC}/k_{diel}) [31],

$$\boldsymbol{E_{diel}} = \left(\frac{\boldsymbol{K_{SiC}}}{\boldsymbol{K_{diel}}}\right) \times \boldsymbol{E_{SiC}} \,. \tag{3}$$

Thus a higher k value indicates a lower dielectric field in drain blocking mode operation. These potential benefits are recognized [3, 31], and are being pursued by some groups [32].

The use of an alternative dielectric may require a gate electrode other than Si that is more chemically compatible; TiN is one choice used with high-k Hf-based dielectrics on Si. This opens the possibility for work function selections that may prove beneficial for threshold voltage control.

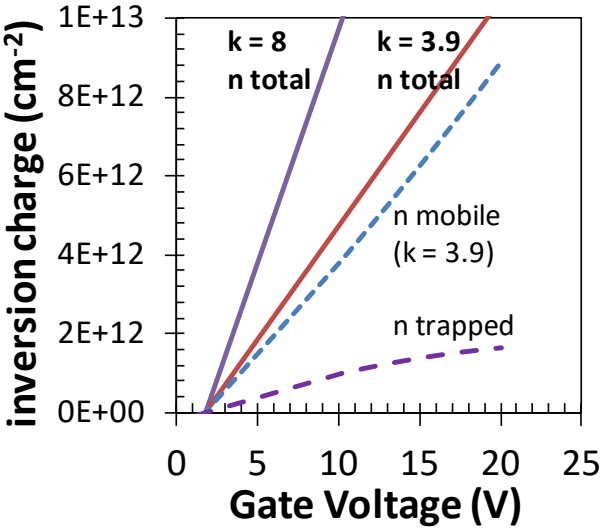

Fig. 4. Graph showing: 1) how trapped charge due to interface states will lead to a lower mobile charge density in the channel than theoretically predicted (thus lowering the field-effect mobility); and 2) a dielectric with a dielectric constant 2X that of SiO_2 will double the channel inversion charge for the same gate bias, ~doubling the output device current if no other interface effects are present.

Device Design

Device designs must also be optimized to take advantage of the improvements offered by a higher channel conduction, and the better channel saturation that could be achieved by decreasing the interface traps and carrier scattering sources. A device with higher channel mobility allows for design-related changes that can enable the improvements listed in Table I. Some improvements to reliability and stability and robustness can be realized for a MOSFET with a given $R_{DS,on}$ and blocking voltage, if the channel mobility were increased. Modifying existing devices by scaling the layout is one approach; another is to design entirely new devices which increase the channel area [33, 34], or use fully-depleted fin channels [35]. Existing device structures will clearly benefit from a high channel mobility; although radical device designs such as fully-depleted fin devices [35] could provide a solution to interface trap effects by design alone, eliminating the need for complex MOS materials and processing. In addition, changes to the doping profile of the channel can provide some benefits, such as counter-doping (summarized in [8]). Still, efforts to minimize channel defects and increase channel mobility will be generally useful for all MOS devices.

Physical modeling approaches such as TCAD can help drive device design to the optimal space; provided the models are properly informed by interface and dielectric measurements that allow the MOS properties to be fully calibrated in the model.

Interface Characterization: Performance and Reliability

Comprehensive MOS characterization approaches are needed to fully understand the present state of interface trap density and related issues (fixed traps, near interface oxide traps, surface roughness, etc.). A recent review [36] discusses many important SiC defect characterization techniques and describes the energy levels of the defects probed by each technique. SiC MOS device interfaces are difficult to fully characterize due to issues related to the wide bandgap semiconductor, and the challenges of measuring very shallow and very deep traps, needed to characterize the entire bandgap. More complete and comprehensive measurements will enable a better understanding of why alternative approaches improve or degrade channel performance.

Commonly used measurements of note for characterizing MOS interface properties include high-low C-V capacitor measurements, which can probe relatively close to the band edges [36, 37], and lateral MOSFET charge pumping [36, 38] which probe traps within the mid-gap regions. Hall measurements of the channel from gated MOS Hall structures are very valuable for separating out

the various channel electrical parameters (carrier concentration, Hall mobility), and is an important characterization to perform [4, 10]. Ultimately, measurement results from tests such as these must be correlated to the channel mobility measured from MOSFET test structures [39]. It is important to use the temperature dependence of these parameters to fully characterize the effects of any given interface passivation.

Other more specialized techniques such as scanning probe microscopy [40], deep-level transient spectroscopy (DLTS) and magnetic resonance related techniques [36, 41] can help provide additional information for a more complete understanding of the MOS region.

Finally, gate dielectric reliability must be carefully studied before a new dielectric or interface process is accepted. Rigorous testing is required to qualify any MOSFET gate processing, as discussed in recent publications [42]. Threshold voltage stability is another key MOS reliability metric [43] which must be proven out for new MOS materials and processing. Finally, threshold instability under gate switching conditions also must be examined, as recent research has demonstrated this to be an important consideration under certain device operation conditions [44, 45].

Summary

Attempts to improve SiC MOSFET channel performance need to continue for improved device performance to be realized. Previous and present research on SiC MOSFETs show that improvements are possible that would result in higher channel mobility and decreased threshold instability. Improved interface passivation, or new gate dielectrics, need to be fully characterized to ensure that performance benefits do not come at the cost of device reliability. Device design changes may also need to be considered to fully realize all potential benefits of higher channel mobility and/or the use of alternative dielectrics.

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