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Comparison of the Performance-Degrading Near-Interface Traps in Commercial SiC MOSFETs

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Abstract. This paper presents a comparison of the density of performance-degrading near-interface traps (NITs) in the most commonly available 1200 V commercial N-channel SiC power metal–oxide–semiconductor field-effect transistors (MOSFETs). A recently developed integrated-charge technique was used to measure the density of NITs with energy levels aligned to the conduction band, which degrade MOSFET's performance by capturing and releasing electrons from the channel biased in the strong-inversion condition. Trench MOSFETs of one manufacturer have lower densities of these NITs in comparison to MOSFETs with the planar gate structure, corresponding to observed higher channel-carrier mobility in trench MOSFETs. Different response-time distributions were also observed, corresponding to different spatial location of the measured NITs.

Introduction

Commercialization of SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) began in 2011, and since then they have become a preferred choice in the power electronics industry. In spite of technological advancements in the past decade, SiC MOSFETs are still unable to realize the full potential of SiC because of a high density of oxide defects at and near the SiC/SiO_2 interface [1]. These defects act as near-interface traps (NITs) for electrons, which significantly degrade the performance and adversely impacts the reliability of SiC MOSFETs [2, 3]. When the MOSFET operates at sub-threshold voltages, NITs with energy levels within the bandgap are active and capture electrons resulting in threshold voltage drift, making it a reliability issue [4]. When the applied gate voltage (V_G) is above the threshold voltage (V_T), the Fermi level crosses the bottom of the conduction band because of the quantum confinement effect [5]. At these gate voltages, the energy levels of NITs that are aligned to the conduction band continuously trap and release electrons from the MOSFET channel by tunneling [6]. This phenomenon degrades the performance of the device by reducing the effective channel-carrier mobility.

The standard characterization techniques can only quantify NITs in the sub-threshold region, even when the MOSFETs are biased at the operating gate voltage ranging from 15 V to 20 V [7–9]. However, we have recently developed an integrated-charge technique that can characterize the performance-degrading NITs in commercial MOSFETs at operating gate voltages [7]. In this paper, we compare the density of performance-degrading NITs in the most commonly available 1200 V commercial N channel SiC power MOSFETs by applying the integrated-charge technique.

Experimental Details

The investigation includes 1200 V commercial N channel SiC power MOSFETs with the most popular planar and trench gate structures from various manufacturers. The on-resistance ($R_{DS(on)}$) and the gate

capacitance (C_G) at 18 V of the MOSFETs used in this study are summarized in Table 1. $R_{DS(on)}$ was determined by standard I–V measurements given in the datasheets by the manufacturers of respective devices, whereas C_G was measured using the integrated-charge technique. $R_{DS(on)}$ and C_G were used to determine a figure of merit (FOM), which is inversely proportional to the density of performance-degrading NITs [10].

Table 1: On-resistance ($R_{DS(on)}$), measured gate capacitance (C_G) at V_G = 18 V, and figure of merit, $FOM = R_{DS(on)} \times C_G$ [10] for 1200 V commercial MOSFETs

Manufacturer	MOSFET ID	Gate Structure	$R_{DS(on)}$ [mΩ]	C_G [pF]	$FOM = R_{DS(on)} \times C_G$ [$\times 10^{-12}$ ΩF]
A	A1	Trench	90	977	89
A	A2	Trench	350	280	98
B	B	Planar	281	530	149
C	C1	Planar	280	1,635	458
C	C2	Trench	105	1,424	149.5
D	D1	Planar	282	592	167
D	D2	Planar	360	583	210
E	E	Planar	192	1,295	249

It is worth noting that C_G is different from the input capacitance, C_{iss}, provided in the datasheets. C_G is a function of V_G, however, the datasheets provide C_{iss} at $V_G = 0$ and large drain-to-source voltages [10]. Also, the gate oxide capacitance (C_{ox}) can be defined as the gate capacitance, C_G, measured at the manufacturer's recommended gate drive voltage and grounded drain and source terminals. At this operating gate voltage, the P-type body of MOSFETs is inverted at the semiconductor surface creating the channel, whereas the N-type drift region is accumulated. Consequently, the active area and thickness of the gate capacitor become equal to the gate area (A_G) and gate oxide thickness (t_{ox}), respectively. The gate oxide thickness of the device can be determined from I_G–V_G characteristics using Fowler–Nordheim tunneling, which can further be utilized to find A_G [7, 11].

To perform the measurements using the integrated-charge method, the drain, and the source of the MOSFET were connected to the ground and an external resistance, R_{EXT}, was connected in series with the gate. The series connection of the gate capacitance, C_G and R_{EXT}, was biased with an input DC voltage from 20 V and slowly stepped down to -20 V. At a specific input DC voltage, a square waveform with small voltage steps (ΔV_{step}) and time interval of $t_{step} = 1/(2f)$ was superimposed by a Tektronix AFG1022 function generator. The current in the RC circuit charges the gate capacitor during the interval t_{step} and then discharges it during the other half of the cycle. The voltage across the R_{EXT} was measured using Tektronix P6139B voltage probes with Tektronix DPO 7104 oscilloscope to obtain the current through the gate capacitor. The measured current was used to determine the charge $qN_{carriers}$ in response to the applied ΔV_{step}. This charge corresponds to an electrically active gate capacitance $C_G = qN_{carriers}/\Delta V_{step}$. To quantify the NITs with response times shorter than 500 μs, 50 μs, 5 μs, and 500 ns, square waveforms were used with frequencies of 1 kHz, 10 kHz, 100 kHz, and 1 MHz, respectively. All the measurements were performed at room temperature.

Results and Discussion

The capacitance–voltage (C–V) curves for different response times τ_{min} obtained using the integrated-charge technique are shown in Fig. 1 (a) and (b) for MOSFET D2 with planar gate structure and MOSFET A1 with trench gate structure, respectively. C_G was measured as a function of V_G for the response times (capture/release times) of 500 μs, 50 μs, 5 μs and 500 ns. A reduction in the gate capacitance is observed with shorter response times because the trapped charge is unable to contribute

to the measured gate current for the duration it is trapped, which reduces the electrically active gate capacitance. Hence, the total density of trapped charge per unit area can be determined by [12]:

$$\Delta N_{trapped}(\tau_{min}) = \frac{\Delta V_{step}}{qA_G}[C_{G-long} - C_{G-short}(\tau_{min})] \quad (1)$$

where C_{G-long} is the measured C–V curve with the reference t_{step} of 500 µs, and $C_{G-short}$ is the measured C–V curve with the shorter time steps. The total density of trapped charge was calculated for 50 µs, 5 µs, and 500 ns using 500 µs as the reference.

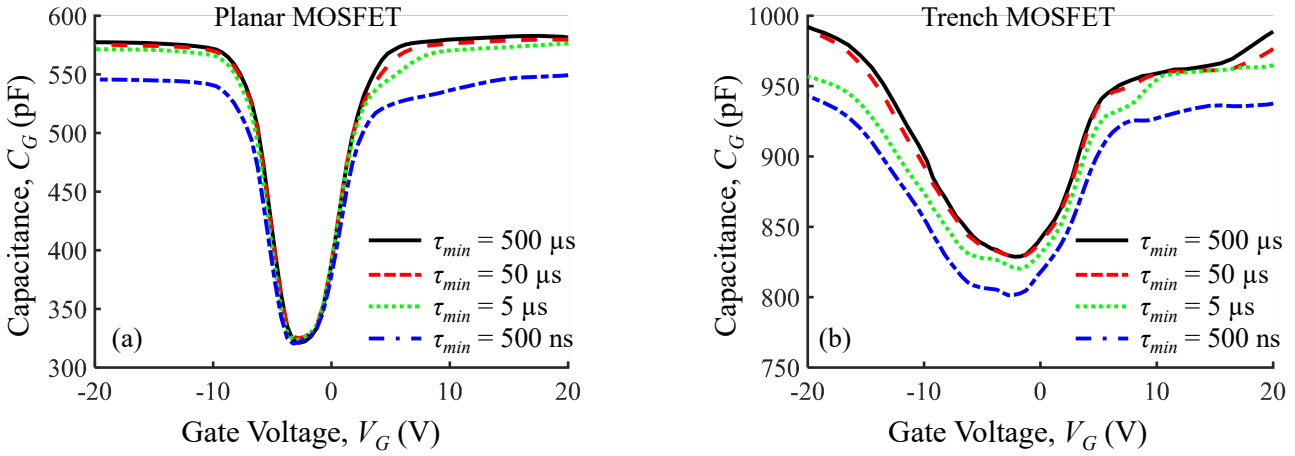

Fig. 1: Capacitance–voltage curves of 1200 V commercial N-channel SiC Power MOSFETs for MOSFET D2 with planar gate structure (a) and MOSFET A1 with trench gate structure (b).

The focus of this paper is to characterize the NITs that can trap electrons from the channel and consequently degrade the performance of the device. These NITs can trap electrons only at above-threshold gate voltages. Hence, it is important to compare the fraction of trapped electrons at above-threshold gate voltages. At a given voltage, the fraction of electrons that are trapped for a period longer than τ_{min}, in response to applied voltage step (ΔV_{step}), can be given by [12]:

$$\gamma(\tau_{min}) = \frac{\Delta N_{trapped}(\tau_{min})}{C_{ox}\Delta V_{step}/qA_G} = \frac{C_{G-long} - C_{G-short}(\tau_{min})}{C_{ox}}. \quad (2)$$

Figure 2 shows the fraction of trapped electrons for various capture/release times (τ_{min}) in the above-threshold region. The results show that more electrons are trapped for shorter response times, irrespective of the manufacturer or the type of gate structure. It is important to note that most devices exhibit no significant change in the density of NITs with increased gate voltage, which indicates fairly uniform distribution of NIT's energy levels. However, referring to Fig. 2 (a) and Fig. 2 (b), we observe that MOSFET C1 (planar) and MOSFET C2 (trench) show a higher density of NITs at low voltages compared to higher voltages. This indicates that MOSFET C1 and MOSFET C2 have a higher density of NITs with low energy levels and capture/release times between 5 µs and 50 µs .

The fraction of the total density of electrons trapped for longer than τ_{min} at the operating gate voltage, V_G, can be determined by [12]:

$$\gamma_{TOT}(\tau_{min}) = \frac{\Delta V_{step}}{V_G - V_T}\sum_{0}^{V_G}\gamma(\tau_{min}). \quad (3)$$

Figure 3 compares $\gamma_{TOT}(\tau_{min})$ for different capture/release times and for all measured MOSFETs at V_G = 18 V. It can be seen that MOSFET E and MOSFET B have higher slope compared to other devices. These means that the density of NITs in these devices is higher near the SiC/ SiO_2 interface and lower further from the interface. It can also be observed from Fig. 3 that, for manufacturer C, the trench

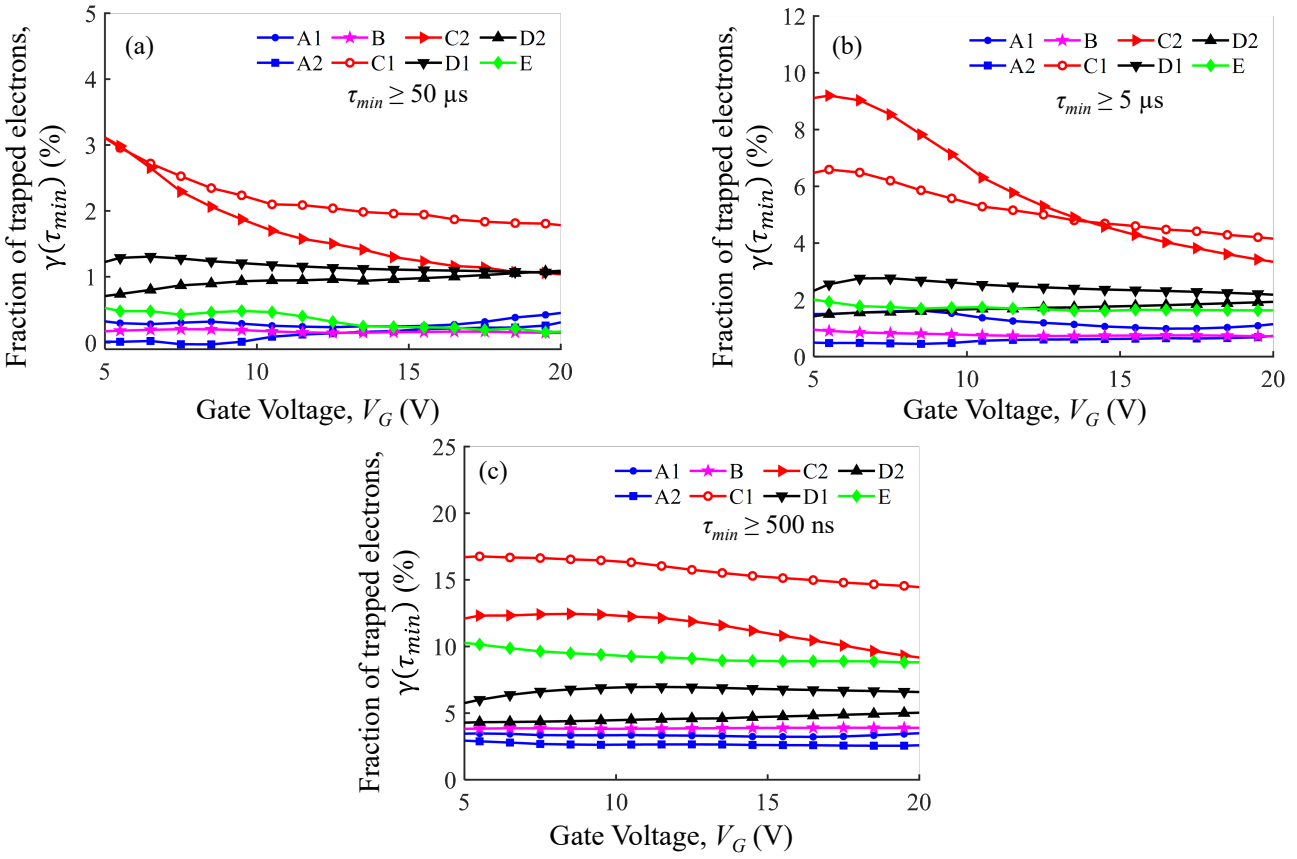

Fig. 2: The fraction of channel electrons trapped for longer than τ_{min} = 50 µs (a), longer than τ_{min} = 5 µs (b), and longer than τ_{min} = 500 ns (c).

MOSFET C2 has a lower density of NITs compared to the planar MOSFET C1. Overall, the density of the performance-degrading NITs in trench MOSFETs by manufacturer A correspond to improved performance in comparison with planar MOSFETs. These results also confirm that lower values of the figure of merit proposed in [10] correspond to lower densities of NITs and, hence, correspond to higher-quality MOSFETs.

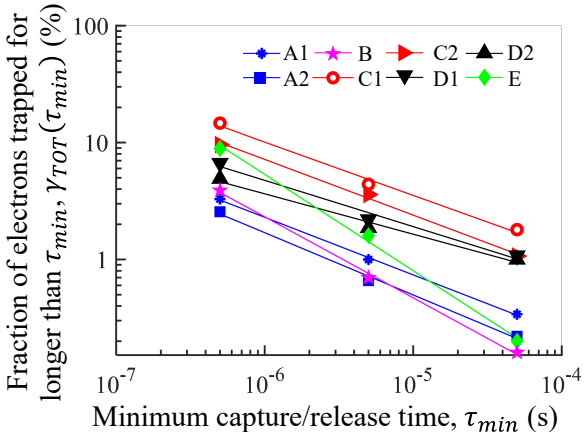

Fig. 3: The fraction of the total density of trapped channel electrons for longer than τ_{min} at V_G = 18V.

Summary

A comparative analysis of the most commonly available 1200 V commercial SiC power MOSFETs in terms of the density of performance-degrading NITs is presented in this paper. The quantification

of the NITs is performed with a recently developed integrated-charge method which is capable of characterizing NITs in the above-threshold region. The results present comparative trap-distribution profiles of the NITs in various commercial devices, which contributes to better understanding of their energy and spatial positions. The results show that up to 15% of channel electrons were trapped at the operating gate voltage for longer than 500 ns, and this fraction is expected to be higher for the shorter response times.

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