Materials Science Forum
ISSN: 1662-9752, Vol. 1091, pp 31-36
doi:10.4028/p-mqpk26

Submitted: 2022-09-03
Revised: 2022-11-16
Accepted: 2022-11-25
Online: 2023-06-05

SiC MOSFETs Biased C-V Curves: A Temperature Investigation

Ilaria Matacena[1,a*], Luca Maresca[1,b], Michele Riccio[1,c], Andrea Irace[1,d], Giovanni Breglio[1,e], Alberto Castellazzi[2,f], Santolo Daliento[1,g]

[1]Dept. of Electrical Engineering and Information Technologies, University Federico II, via Claudio, 21, 80125, Naples, Italy

[2]Kyoto University of Advanced Science, 18 Gotanda-cho, Yamanouchi, Ukyo-ku, 615-8577 Kyoto, Japan

[a]ilaria.matacena@unina.it, [b]luca.maresca@unina.it, [c]michele.riccio@unina.it, [d]a.irace@unina.it, [e]breglio@unina.it, [f]alberto.castellazzi@kuas.ac.jp, [g]daliento@unina.it.

Keywords: Gate capacitance, peak, SiC/SiO_2 interface, interface characterization.

Abstract. In this paper, SiC MOSFETs capacitance is monitored when a DC bias is applied between Drain and Source. The arising capacitance exhibits a sharp peak in the inversion region which is related to the SiC/SiO_2 interface traps properties. Temperature effects on such peak are investigated using both experimental and numerical results. The peak shifts toward lower Gate voltage as temperature increases, in agreement with the threshold voltage reduction at higher temperature.

Introduction

Silicon Carbide (SiC) MOSFETs are replacing Silicon (Si) IGBTs, due to the excellent properties of SiC, such as high thermal conductivity and high bandgap [1]. Although this technology experienced noticeable progress in last years, some challenges are still open. Among these, high density defects at the SiC/SiO_2 interface can impact the overall performance of the device [2], causing detrimental effects on threshold voltage stability [3], channel mobility [4] and leakage current amplitude. Given the importance of characterizing such interface, several techniques have been used to investigate defects properties related to this region. These techniques would preferably be non-destructive and low time consuming. Most methods exploit the information arising from capacitance measured at high and low frequency [5]. Although widely used for MOS structures, this method cannot be employed for MOSFET structures. This can be explained by considering that in the inversion region the C-V curve obtained from a MOS change accordingly to the frequency considered, since the inversion charge can follow the AC variation only for low frequencies due to the very low thermal carrier generation rate in the depletion region. On the other side, in a MOSFET structure, the channel is full of carriers coming from the Source and Drain regions. This means that the C-V curve in the inversion region does not differ at high and low frequency [6]. Thus, experimental C-V curves should be supported by numerical analysis in order to characterize the mentioned interface in the case of MOSFET structures [7]-[11]. Gate capacitance measurements are conventionally performed by connecting Drain and Source terminals [12]-[14], while the input signal is applied to Gate terminal.

In this work, we perform non-classical C-V measurements with positive biased Drain. The experimental part is performed on commercially available planar SiC MOSFETs, showing an unexpected sharp peak arising in the Gate capacitance in the inversion region. To further investigate the arising capacitance an experimental temperature analysis is also performed. The experimental results are confirmed by numerical model obtained in Sentaurus TCAD environment. Temperature analysis show that the Gate capacitance peak arising in both experimental and numerical results shifts toward lower voltage as temperature increases.

Results

Experimental setup and results. The experimental data are obtained using the setup of Fig.1a, the capacitance is measured between Gate and Source terminals, while a DC bias is applied to Drain

terminal, V_{DS}. The applied Gate voltage, V_{GS}, ranges from -10 V to 10 V, while the superimposed AC small signal has an amplitude of 100 mV and the frequency is set to 100 kHz, Fig.1b. The applied V_{DS} is swept from 0.2 V to 0.8 V in steps of 0.1 V, Fig.1c. The obtained capacitance curves are shown in Fig.2. The capacitance behavior obtained in this configuration is similar to the one obtained with conventional C-V method in the accumulation and depletion region, while a substantial difference is observed in the inversion region. As shown in Fig.2, the obtained capacitance curves exhibit a non-negligible peak centered at a voltage close to the threshold voltage. This peak is more prominent as the applied Drain voltage increases.

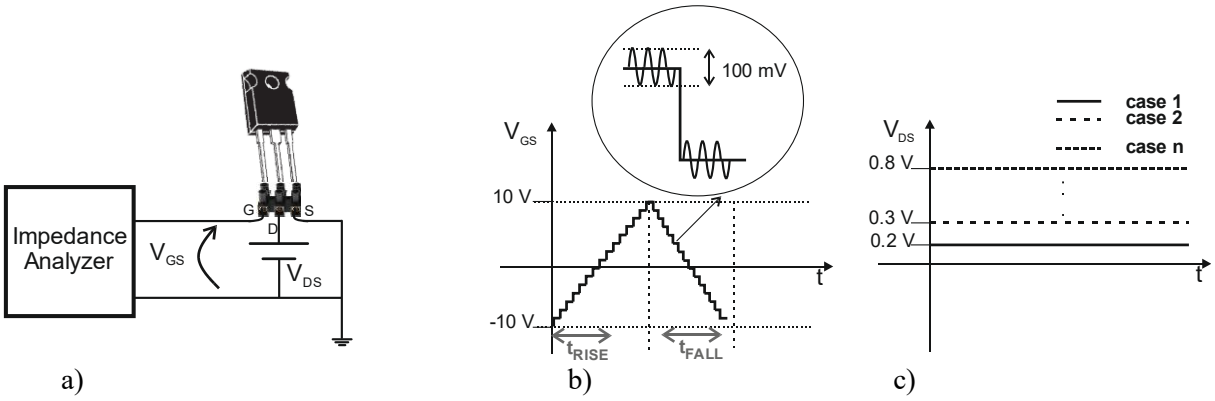

Fig. 1. a) Experimental setup used; b) Gate Voltage and c) Drain voltage applied during measurements.

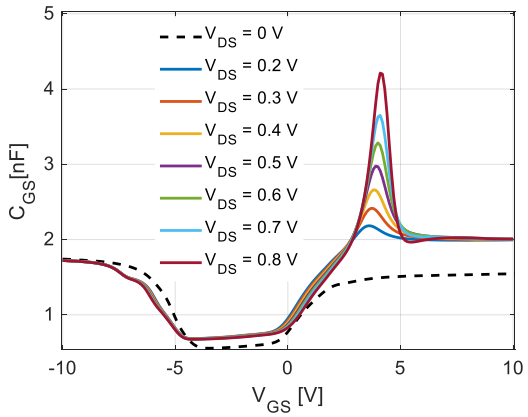

Fig. 2. Experimental C-V curves obtained from a commercial device (C2M0160120D) with V_{DS} varying.

In previous work, we related this peak shape to traps in the channel region [11] and a complex electric field/free charges dynamics is assumed to be responsible for this phenomenon. In order to gain a better understanding of the trap distribution and its effects on Gate capacitance, a temperature study is performed on the DUT. Temperature is a key parameter in interface traps characterization, since traps occupation is sensitive to temperature variation. Thus, the number of occupied traps is a function of temperature and traps concentration may change as temperature varies. This phenomenon is more evident if traps are located near the Conduction or Valence Band edges. To this aim, experimental C-V curves with positive biased Drain have been performed at different temperature values. In Fig.3, experimental results obtained from a commercial device measured at 300 K, 375 K and 425 K are shown. It can be observed that the capacitance peak shifts towards lower voltage values as temperature increases. This results is in agreement with the shift of threshold voltage to lower values at higher temperature. Measurements presented in Fig. 4 have been performed on a different device with temperature varying from 300 K to 450 K in steps of 10 K. The same trend arises also from this set of measurements, confirming the previous outcome.

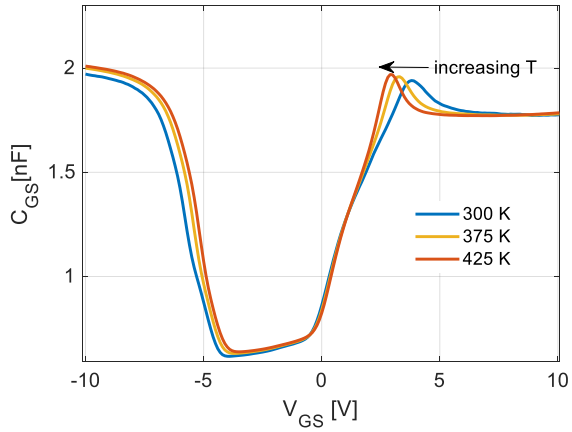

Fig. 3. Experimental C-V curves obtained at different temperature values, with a V_{DS} = 0.1 V

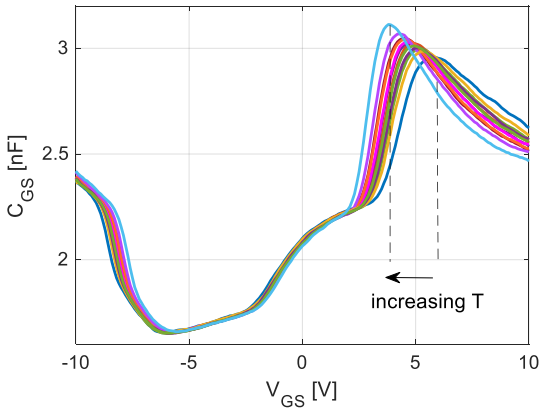

Fig. 4. Experimental C-V curves obtained at different temperature values, with a V_{DS} = 0.2 V

Numerical setup and results. A numerical framework is built in Sentaurus TCAD to carefully replicate the experimental setup. The structure simulated is presented in Fig. 5 and an AC small signal analysis is performed in order to obtain the capacitance behavior [7]. In the numerical framework it is possible to accurately describe the traps distribution in the structure. Capacitance behavior is strongly affected by traps and their complex distribution at channel interface firmly influences the threshold voltage of the overall device. This situation is even more complex when the temperature of the device changes. There are several temperature dependent parameters, among them it is worth to mention the strong temperature dependence of traps electron emission rate, which causes in some cases, such as short circuit [15], a critical threshold voltage variation. Thus, a great attention must be paid to the modelling of interface traps. In this work, trap distribution at SiC/SiO_2 interface is described with a square distribution of width $2E_{TW}$ and centered at E_{TC}, Fig. 6. The distribution is considered uniform along all the SiC/SiO_2 interface [16], since no calibration is performed on experimental data. Traps and charges existing in a SiC MOSFETs are of several types, but they can be mainly grouped into: traps located in the oxide layer and traps located at the SiC/SiO_2 interface. In the oxide layer there are fixed charges and movable ions, while near the interface there are plenty of trapped charges. Traps and defects occupy various energy levels and positions in the structure. Hence at high temperature they differently affect capacitance curves. For example, the mobile ionic charge has a large activation energy and at low temperature it does not significantly affect the device behavior. In this paper, we investigate the effects of fixed charge and interface traps on the C-V curves when a positive bias is applied to Drain terminal at different temperature values. Traps parameters chosen for each numerical result are described in the caption of the figures. All numerical results have been carried out by adopting the Arora model for mobility [17] and the Scharfetter model [18] for lifetime, while the specific SiC parameters have been chosen according to previous work [15]. In order to accurately describe temperature effects, several temperature dependent models have been considered in the numerical analysis. More in detail, the temperature dependance of the bandgap and

of the generation-recombination processes has been taken into account, as well as the bandgap narrowing phenomenon.

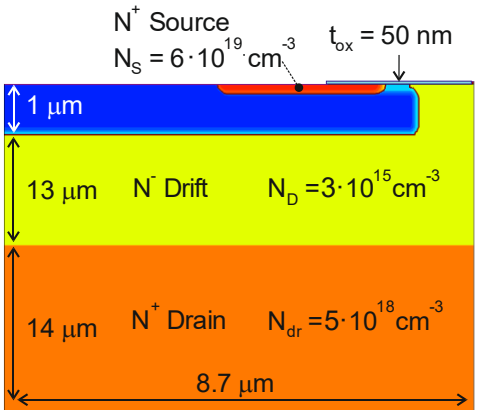

Fig. 5. Structure built in Sentaurus TCAD. The structure is not to scale.

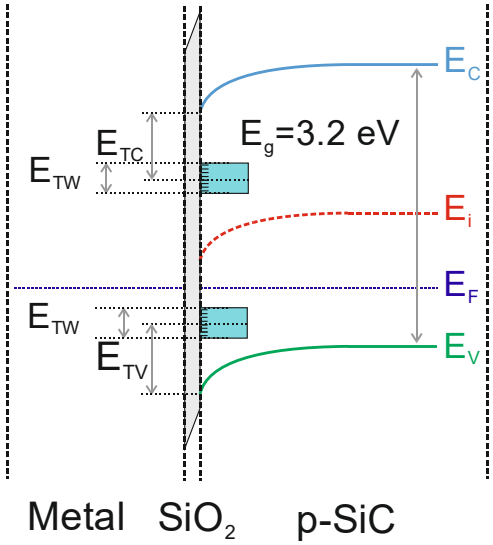

Fig. 6. Band diagram of the TCAD structure.

Numerical curves are obtained when a voltage V_{DS} = 1 V is applied between Drain and Source, Fig. 7. In this figure, the curves are carried out at different temperature values, chosen accordingly to the experimental case considered in Fig. 3. It is possible to notice that the numerical capacitance exhibits a sharp peak in the inversion region, while the behavior in the accumulation and depletion region agrees to the classic capacitance behavior obtained when no bias is applied between Drain and Source. It is evident that the peak shifts towards lower Gate voltage as the temperature increases. This result confirms the behavior found in the experimental data. Moreover, this result agrees with the threshold voltage reduction with increasing temperature.

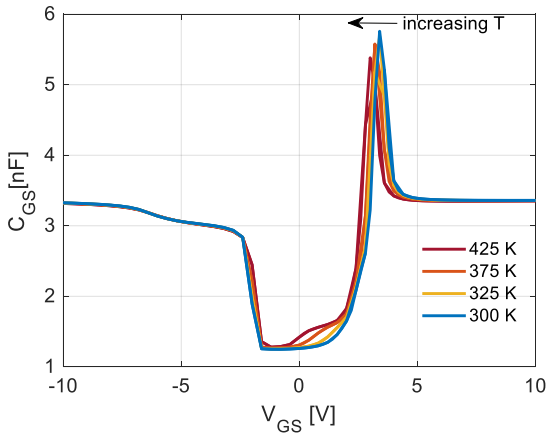

Fig. 7. Numerical C-V curves obtained at different temperature values, from structure of Fig.4. The following interface traps properties have been assigned in the channel region: $C_{FIX} = 1 \cdot 10^{13}$ cm $^{-3}$, $C_{Traps} = 5 \cdot 10^{12}$ cm $^{-3}$, $V_{DS} = 1$ V. Traps considered in this study are acceptors.

Conclusions

In this work, a non-conventional capacitance measurement method is performed by applying a DC bias between Drain and Source during the sweep of the Gate voltage. The resulting capacitance differs from classic C-V curve, exhibiting an unexpected sharp peak in the inversion region. The peak is related to the interface trap distribution and its properties can be related to interface quality. The temperature effects on the mentioned C-V curves are considered. It is found that the capacitance peak moves toward lower Gate voltage as the temperature increases. A TCAD model has been developed and the numerical results obtained using the same temperature values are in agreement with experimental findings. The shift of the peak toward lower voltage with increasing temperature coincides with the lowering of the threshold voltage with temperature.

References

[1] B. J. Baliga, Fundamentals of power semiconductor devices, Springer Science & Business Media, (2010).

[2] C. Raynaud, et al., Comparison of trapping–detrapping properties of mobile charge in alkali contaminated metal-oxide-silicon carbide structures, Applied physics letters 66, no. 18: 2340-2342, (1995).

[3] D. Peters et al., Investigation of threshold voltage stability of SiC MOSFETs, ISPSD, (2018).

[4] V. V. Afanasev, et al., Intrinsic SiC/SiO2 interface states, physica status solidi (a) 162, no. 1: 321-337, (1997).

[5] Schroder, D.K. Semiconductor Material and Device Characterization, 3rd ed.; Wiley: Hoboken, NJ, USA, 2006

[6] Hu, Chenming Calvin. "Modern Semiconductor Devices for Integrated Circuits." Part I: Electrons and holes in a semiconductor (2011).

[7] L. Maresca et al. Influence of the SiC/SiO2 SiC MOSFET Interface Traps Distribution on C–V Measurements Evaluated by TCAD Simulations. IEEE Journal of Emerging and Selected Topics in Power Electronics 9.2 (2019): 2171-2179

[8] Matacena, Ilaria, et al. "Experimental Analysis of CV and IV Curves Hysteresis in SiC MOSFETs." Materials Science Forum. Vol. 1062. Trans Tech Publications Ltd, 2022.

[9] Matacena, Ilaria, et al. "SiC MOSFET CV Curves Analysis with Floating Drain Configuration." Materials Science Forum. Vol. 1062. Trans Tech Publications Ltd, 2022.

[10] Matacena, Ilaria, et al. "Evaluation of Interface Traps Type, Energy Level and Density of SiC MOSFETs by Means of CV Curves TCAD Simulations." Materials Science Forum. Vol. 1004. Trans Tech Publications Ltd, 2020.

[11] I. Matacena, L. Maresca, M. Riccio, A. Irace, G. Breglio, S. Daliento, & A. Castellazzi, (2022). SiC MOSFET CV Characteristics with Positive Biased Drain. In Materials Science Forum (Vol. 1062, pp. 653-657). Trans Tech Publications Ltd.

[12] Wei, Jiaxing, et al. "Interfacial damage extraction method for SiC power MOSFETs based on CV characteristics." 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD). IEEE, 2017.

[13] Tsuji, Katsuhiro, et al. "Measurement of MOSFET CV curve variation using CBCM method." 2009 IEEE International Conference on Microelectronic Test Structures. IEEE, 2009.

[14] Jouha, Wadia, et al. "Physical study of SiC power MOSFETs towards HTRB stress based on CV characteristics." IEEE Transactions on Device and Materials Reliability 20.3 (2020): 506-511.

[15] G. Romano, M. Riccio, L. Maresca, G. Breglio, A. Irace, A. Fayyaz, and A. Castellazzi, (2016, June). Influence of design parameters on the short-circuit ruggedness of SiC power MOSFETs. In Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on (pp. 47-50). IEEE.

[16] Maresca, Luca, et al. "TCAD model calibration for the SiC/SiO 2 interface trap distribution of a planar SiC MOSFET." 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia). IEEE, 2020.

[17] N. D. Arora, J. R. Hauser, and D. J. Roulston, “Electron and Hole Mobilities in Silicon as a Function of Concentration and Temperature,” IEEE Transactions on Electron Devices, vol. ED-29, no. 2, pp. 292–295, 1982.

[18] J. G. Fossum, and D. S. Lee. "A physical model for the dependence of carrier lifetime on doping density in nondegenerate silicon." Solid-State Electronics 25, no. 8 (1982): 741-747.