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Investigation on Switching Characteristics of 3.3kV SiC Power MOSFETs with SiO_2/SiN Gate Stack

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Abstract This paper focuses on reporting the switching behaviour of our Silicon Carbide (SiC) power MOSFETs, rated 3.3kV – 25A. The devices are based on a gate stack formed by SiO_2/SiN and have been tested during Inductive Load Switching (ILS) in different conditions (nominal and SOA) with different chip configurations (single/multiple dies). In this contribution, the turn–on and turn–off curves are reported, along with the extracted RBSOA and switching energies.

Introduction

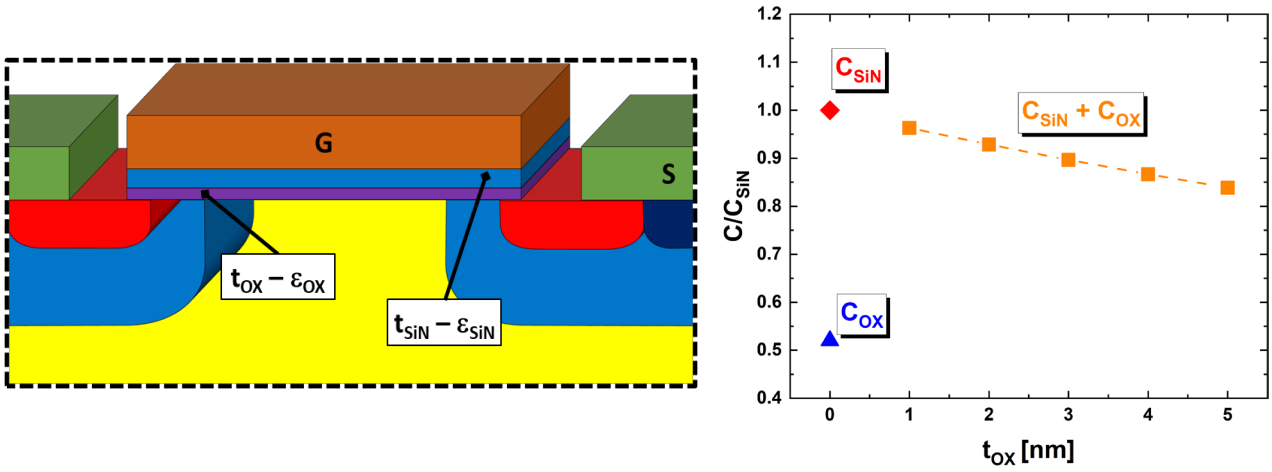
Silicon Carbide (SiC) power MOSFETs are nowadays established components in a wide range of power systems, thanks to the well–known advantages they bring compared to Silicon devices. Although the main drivers for SiC power markets are low voltage devices (900V–1.7kV), the use of 3.3kV–rated SiC power MOSFETs for medium voltage (MV) and high voltage (HV) applications (e.g. high–speed rail traction) has recently become more and more attractive [1]–[2] . One of the main factors to improve the overall performances of SiC power MOSFETs is reducing the channel resistance contribution. If on one hand this is achievable by increasing the channel density (e.g. reducing the pitch size), most of the focus in the past years has been dedicated to improve the SiC/gate–dielectric interface's quality. While high–k materials have been researched before as potential gate dielectrics in SiC technology [3]–[4], we have been the first to prove the benefits brought by the integration of high–k gate dielectrics in fully operational power SiC MOSFETs [5]–[7]. The main benefit of using such gate structure is a reduced interface state density (D_{it}), corresponding to a higher channel electron mobility and an improved threshold voltage (V_{TH}) stability.

In this work we report the dynamic behaviour of our 3.3kV SiC MOSFETs fabricated using a SiO_2/SiN gate dielectric stack technology.

Gate Technology

As mentioned before, implementing a gate dielectric based on high–k material brings along several advantages [5]–[7]. The immediate effect of a gate layer with higher dielectric constant ε_D is the larger dielectric capacitance C_D (for a given dielectric thickness t_D). This implies an increased channel carrier concentration n_S that enhances the conduction current, i.e. reducing the channel resistance. Additionally, we have also demonstrated [5] that, given an adequate process integration scheme, a high–k material considerably reduces the interface D_{it}. The first consequence of having less defects states across the semiconductor/gate interface is to lower scattering effects, resulting in an increased inversion channel mobility. Moreover, a significant reduction of the traps leads to a much more stable threshold voltage [6].

We have successfully applied our first generation of high–k gate to 3.3kV devices, showing their rugged dynamic behaviour in [8].



(a) (b)

Fig. 1: Sketch of the 2–layer gate structure (a), and dependence of the normalized dielectric capacitance as function of SiO_2 thickness (b)

On the other hand, the focus of this contribution is on the switching behaviour of our HV devices fabricated with a gate stack composed of very thin layer of standard oxide with a layer having higher dielectric constant above it. The resulting SiO_2/SiN gate structure is sketched in Fig. 1(a). The purpose of this choice, compared to our previous high–k technology, is to investigate the behaviour of the device when only higher gate dielectric capacitance is used, without benefiting from the improved and higher mobility.

In such a structure, it is easy to evaluate the whole dielectric capacitance as the series connection of the two capacitances corresponding to each of the two stacked insulating layers:

$$\frac{1}{C_{TOT}} = \frac{1}{C_{OX}} + \frac{1}{C_{SiN}} = \frac{t_{OX}}{\varepsilon_{OX}} + \frac{t_{SiN}}{\varepsilon_{SiN}}$$
$$\rightarrow \frac{1}{C_{TOT}} \approx \frac{1}{C_{SiN}}, for\ t_{OX} \ll t_{SiN} \quad (1)$$

It can then be approximated to the capacitance of the layer with higher dielectric permittivity when the SiO_2 layer is much thinner than the one on top (1). Fig. 1(b) depicts the dependence of the total dielectric capacitance for different oxide layer thickness. Predictably, the thinner the SiO_2 becomes, the closer the whole capacitance value is to the pure SiN case.

The electric field in the semiconductor, for a given applied gate voltage V_G, could also be derived using Gauss' Law and considering the effect of the SiO_2 interlayer:

$$E_{SiC} = \frac{C_{SiN}}{C_{OX} + C_{SiN}} \cdot \frac{V_G}{t_{OX}} \cdot \frac{\varepsilon_{OX}}{\varepsilon_{SiC}} \quad (2)$$

That can be manipulated as:

$$E_{SiC} = \underbrace{\frac{C_{OX}}{C_{OX} + C_{SiN}}}_{S} \cdot \underbrace{\frac{V_G}{t_{SiN}} \cdot \frac{\varepsilon_{SiN}}{\varepsilon_{SiC}}}_{E'_{SiC}} \quad (3)$$

The equation can be read as the equivalent of the field in the semiconductor as if no buffer was present E'_{SiC}, multiplied by a scaling factor S dependent on the layers' capacitances. It is easy to understand through (1)–(3) that the SiO_2 layer behaves as a buffer layer and can be designed to modulate the input capacitance and the surface electric field in the semiconductor by varying the thickness t_{OX}.

Dynamic Characterization

Devices were assembled on substrates in different configurations, namely with single and up to 4× parallel chips and investigated during standard Inductive Load Switching (ILS) test.

As first step, the devices have been tested in nominal conditions, meaning V_N = 1.8kV and I_N = 25A/device; for all the tests the temperature has been set to T = 150°C and the double–pulse tester had a fixed stray inductance of L_σ~90–100nH. Similar to what was shown for a high–k gate in [8], also the proposed SiO_2/SiN bilayer allows to drive the gate with voltage swings wider than commercially available devices. In all the results reported here, a Si–like driving voltage of V_{GS} = ±15V was used.

The turn–off waveforms in case of single and four devices in parallel are reported in Fig. 2. For this analysis, the gate resistor and the stray inductance were not scaled for parallel devices, implying that the R_G/chip and L_σ/chip are higher for the substrates with four MOSFETs. This is reflected for example in the larger overshoot for the drain voltage in Fig. 2(b) due to the higher parasitic inductance. Also, the expected influence of the gate resistor on the switching speed dV_{DS}/dt is clearly spottable. The more pronounced oscillations on the current waveforms are not chip–related, produced by the experimental setup itself.

The MOSFETs' voltage and current limitations were then explored by gradually increasing the test current and voltage values, reaching twice the nominal current and a voltage of 2.6kV. The respective turn–off waveforms with I_D ranging from I_N to 2×I_N are plotted in Fig. 3(a-b). From the mentioned curves it is also possible to extract the corresponding Safe Operating Areas (SOA) as depicted in Fig. 3(c). It is worth to mention that the substrates with parallel chips still display rather clean waveforms and reasonable voltage oscillations, despite the fact that both voltage and current are beyond nominal values. That proves a balanced current sharing between devices given by an engineered substrate design oriented to the minimization of parasitic components.

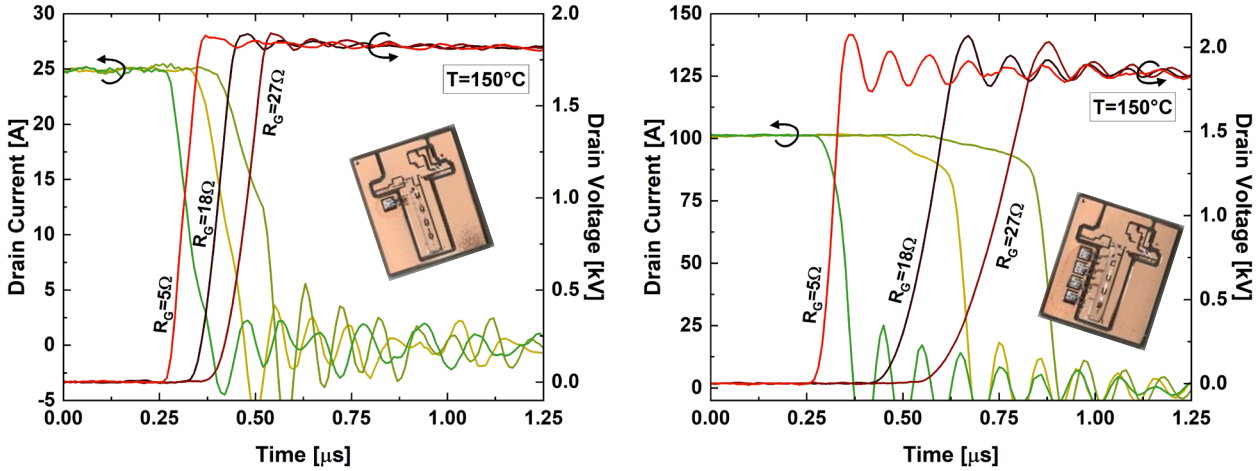
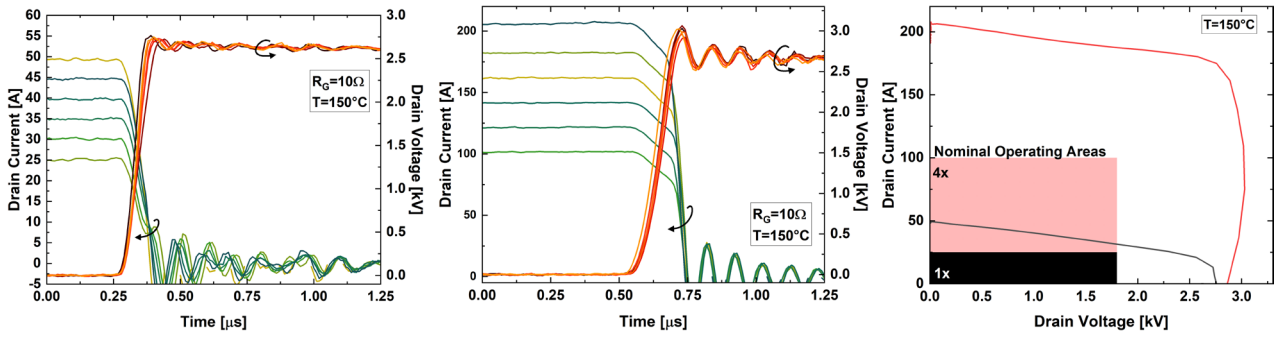


Fig. 2: Turn–off waveforms for substrates with 1× (a) and 4× (b) devices, at different R_G values (V_N = 1.8kV, I_N = 25A/die, V_{GS} = ±15V, T = 150°C)

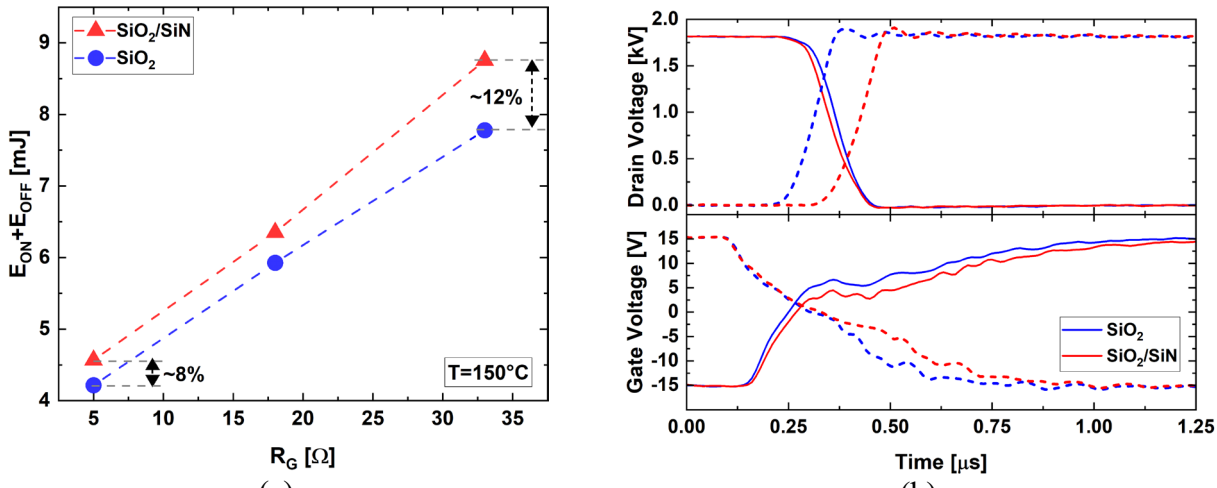


(a) (b) (c)

Fig. 3: Turn–off waveforms for substrates with 1× (a) and 4× (b) devices, at different current values; RBSOA extracted from the switching I–V (c) (V_{SOA} = 2.6kV, I_{SOA} = 50A/die, V_{GS} = ±15V, T = 150°C)

For a more comprehensive investigation, the switching behaviour of MOSFETs with the proposed SiO_2/SiN structure has been compared to devices with same design but fabricated with our standard SiO_2 gate dielectric. In Fig. 4(a), the total switching energy E_{ON} + E_{OFF} per chip, calculated in nominal conditions (V_N = 1.8kV, I_N = 25A), is reported for different values of R_G. As could be expected, the SiO_2/SiN–based devices exhibit marginally higher energy losses due to the increased input capacitance. Nevertheless, the increase in energy for the considered case is still moderately small (~12% max) and, if needed, could be reduced with lower gate resistor values. As already stated, it is in principle possible to modify the dielectric capacitance by adjusting the bilayer design, following a trade–off between conduction performances and switching losses. Also, the turn–on and turn–off voltage transients are virtually the same for both dielectric combinations as per Fig. 4(b) for the case of R_G = 33Ω.

At last, the dynamic transfer characteristics I_DV_{GS} were extracted from turn–on gate voltage and drain current waveforms for both families of fabricated devices at different values of $V_{GS,OFF}$, and the resulting curves are plotted in Fig. 5. The standard SiO_2 shows appearance of dynamic hysteresis as a more negative gate off–voltage is used, while the proposed stack already improves this aspect.



(a) (b)

Fig. 4: Comparison of switching energy (a) and voltage waveforms (b) for SiO_2 and SiO_2/SiN stack (V_N = 1.8kV, I_N = 25A, V_{GS} = ±15V, T = 150°C)

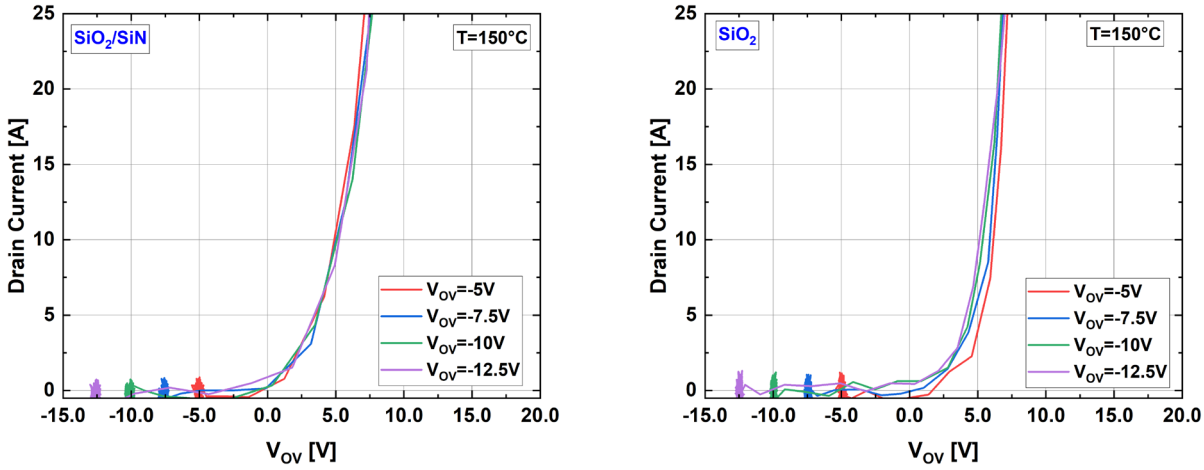


Fig. 5: Dynamic $I_D V_{GS}$ for SiO_2 (a) and SiO_2/SiN stack (b) (V_N = 1.8kV, I_N = 25A, V_{GS} = ±15V, T = 150°C)

Conclusion

This work has described the dynamic behaviour of our 3.3kV SiC power MOSFETs fabricated with a SiO_2/SiN bilayer gate structure. Such devices have been characterized with typical double pulse tests, considering both single and parallel devices operations. The nominal (V_N = 1.8kV, I_N = 25A/die) and RBSOA (V_{SOA} = 2.6kV, I_{SOA} = 50A/die) operations have been proven for different gate resistors. The switching energies were afterwards compared with standard gate oxide, demonstrating that the increased input capacitance given by the higher dielectric constant, could have limited effect on the dynamic losses.

References

[1] K. Sato, H. Kato, T. Fukushima, *Development of SiC applied traction system for Shinkansen high-speed train*, International Power Electronics Conference 2018, pp. 3478-3483.

[2] T. Fukushima, Ext. Abstracts of Int. Conf. on Silicon Carbide and Related Materials 2019, 2019 (Kyoto), PL-1-02.

[3] L. Lipkin and J. Palmour, Insulator Investigation on SiC for Improved Reliability, IEEE Transactions on Electron Devices, Vol. 46, No. 3, March 1999, p. 525

[4] T. Hosoi, S. Azumo, Y. Kashiwagi, S. Hosaka, K. Yamamoto, M. Aketa, H. Asahara, T. Nakamura, T. Kimoto, T. Shimura, and H. Watanabe, *Reliability-aware design of metal/high-k gate stack for high-performance SiC power MOSFET*, 29th ISPSD, 2017.

[5] S. Wirths, Y. Arango, A. Prasmusinto, G. Alfieri, E. Bianda, A. Mihaila, L. Kranz, M. Bellini, L. Knoll, *Vertical 1.2 kV SiC power MOSFETs with high-K/metal gate stack*, 31st ISPSD, 2019

[6] S. Wirths, Y. Arango, A. Mihaila, M. Bellini, G. Romano, G. Alfieri, M. Belanche, L. Knoll, E. Bianda, E. Mengotti, *Vertical power SiC MOSFETs with high-k gate dielectrics and superior threshold voltage stability*, 32nd ISPSD, 2020

[7] S. Wirths, E. Mengotti, J. Bettega, M. Belanche, O. Lopez-Sanchez, E. Bianda, A. Mihaila, Y. Arango, M. Bellini, G. Romano, L. Knoll, *Threshold Voltage Stability Study on Power SiC MOSFETs Using High-k Dielectrics*, PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management 2020, pp. 1-8

[8] G. Romano, S. Wirths, A. Mihaila, Y. Arango, A. Ruiz, L. Knoll, *Rugged Dynamic Behaviour of 3.3kV SiC Power MOSFETs with High-k Gate Dielectric*, 33rd ISPSD, 2021