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Measurement and Analysis of Body Diode Stress of 3.3 kV SiC-MOSFETs with Intrinsic Body Diode and Embedded SBD

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Abstract. SiC MOSFETs display reliability issues related to the quality of SiO_2/SiC interface and bulk material due to the presence of near interface traps and point and extended material defects [1]. These material related issues give rise to a degradation of device reliability and ruggedness. One of them are basal plane dislocations (BPDs) introduced in the drift-layer during the epitaxial growth process which causes a s.c. bipolar degradation. Growth and movement of BPDs fueled by recombination energy has a very significant impact on conduction loss and on-resistance degradation. For 3.3 kV voltage capability, the probability of the appearance of BPDs is greater because the drift region is about three times larger compared to 1.2 kV devices [2-3]. We present measurement results and analysis of bipolar degradation in 3.3 kV MOSFETs with conventional body diode and embedded Schottky barrier diode (SBD). The measurements were performed applying 50 % and 80 % of rated current with duty cycle 80 %, under total time of 100 hrs at constant case temperature of 54 ℃. The 3rd-quadrant performance of both types of MOSFETs in pre-stress conditions was characterized at 25 and 150 ℃ with different gate biases of -10 V, 0 V, and +17 V. To evaluate the bipolar degradation, the diode conduction characteristics were measured at 25 ℃ after different stressing times by diode conduction the MOSFET output characteristics were measured at 25 and 54 ℃ before and after stressing the intrinsic body diode and embedded SBD. No V_{SD} shift was observed in diode conduction characteristics. The results indicate that the MOSFETs were fabricated on appropriate material with a sufficiently low number basal plane dislocation (BPD). The on-state resistance with V_{GS} = +17 V was decreased by temperature due to increased JFET resistance rather than bipolar degradation. On the other hand, the on-state resistance with V_{GS} = +11 V was impacted by the increased temperature and V_{TH} instability.

Introduction

Compared to commercial Si power IGBTs, SiC MOSFETs have a smaller size, low on-resistance and a high breakdown voltage due to 10 times higher electric field strength. These device and material characteristics result in significant benefits in various power electronic applications.

Currently, SiC MOSFETs are being used in applications such as electric vehicles, and stability and reliability are attracting attention as very important factors. However, SiC has many various defects such as a deep level traps inside the energy bandgap, stacking fault defects called basal plane dislocation (BPDs), and threading edge dislocation (TEDs). The 3.3 kV devices are expected to have higher probability of stacking faults than the 1.2 kV. It is because 3.3 kV devices have 3 times larger thickness of the drift layer than 1.2 kV devices.

From the application point of view, the intrinsic body diode built into the MOSFET protects the MOSFET in half-bridge configuration by allowing reverse current to flow during the MOSFET off-state. However, SiC body diode contributes significantly to the turn-on loss due to recovery charge. An external Schottky Barrier Diode (SBD) can be used to reduce turn-on losses due to elimination of recovery charge. The implementation of embedded SBD in the MOSFET allows not only reduction of the turn-on losses but also reduction of the SBD area [4].
In addition, MOSFETs with embedded SBD can avoid voltage drop due to bipolar degradation that can occur in intrinsic body diodes. In this contribution, the body diode stress test was performed on the intrinsic body diode and the embedded SBD structure to measure and analyze the electrical characteristics of the 3.3 kV MOSFETs [5,6, and 7].

Experimental

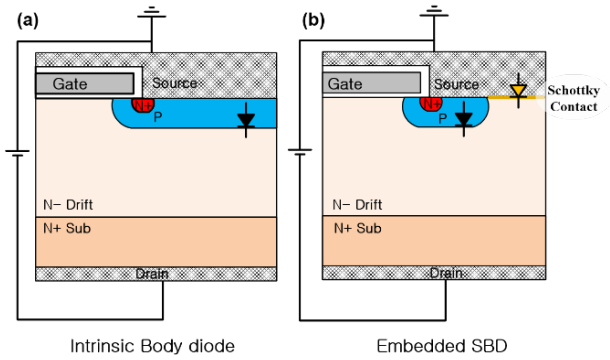

Fig. 1. Schematic cross-sections of SiC MOSFETs with (a) intrinsic body diode and (b) embedded SBD

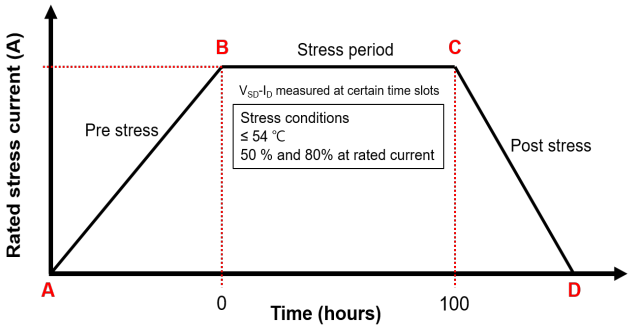

Fig. 2. Body diode bipolar degradation measurement method, and measurement point A to D.

Figure 1 shows two types of 3.3 kV/50 A SiC-MOSFET integrated diode structures. To measure the bipolar degradation in these two types of SiC-MOSFETs, we applied 50 and 80 % of rated current to the body diode and observed the MOSFET diode characteristics in the third quadrant. During the body diode stress test, we applied V_{GS} = -10 V to prevent the channel current from flowing. Then we observed electrical performance changes in output and transfer characteristics due to bipolar degradation and body diode stress in MOSFETs.
Figure 2 shows the stress measurement sequence over time. Measurement points A and D measure the electrical characteristics of V_{DS}-I_D and V_{GS}-I_D before and after bipolar stress at room temp, and measurement points B and C measure V_{SD}-I_S, V_{DS}-I_D, and V_{GS}-I_D at the beginning and end of current stress. Table 1 summarizes the stress and electrical characteristics conditions for bipolar degradation observation.

Table 1. Stress conditions and electric characteristics conditions for bipolar degradation observation

Condition	Intrinsic body diode	Embedded SBD
Temperature [°C]	≤ 54	≤ 54
Duty cycle [%]	80	80
Rated current [%]	50 and 80	80
Applied gate voltage to MOSFET	V_G = -10 V	V_G = -10 V
V_{DS}-I_D characteristics for gate voltage	V_{GS} = 11, 13, 15, and 17 V	V_{GS} = 11, 13, 15, and 17 V
V_{GS}-I_D characteristics	V_{DS} = 10 V, I_D = 5 uA	V_{DS} = 10 V, I_D = 5 uA

Experiment

Figure 3 shows the result of time depending bipolar degradation of intrinsic body diode, and embedded SBD. Characteristics were observed when 50 and 80 % (25 and 40 A) and 50 % (25 A) of rated current with 80 % duty cycle was applied to the intrinsic body diode and embedded SBD, respectively. V_{SD} shift was measured over time to monitor bipolar degradation during 100 hrs of a stress time.

Figure 4 shows the measurement of pre- and post-stress output characteristics of the intrinsic body diode and embedded SBD, respectively. The measurements were performed at 25 and 54 ℃ to observe the degradation of $R_{DS,on}$ with V_{GS} = +17 V and +11 V, respectively. The on-state resistance measured with V_{GS}=+17V was increased by increased channel resistance at 54ºC compared to a room temperature. It is because other scattering mechanisms in the channel region are dominantly higher than thermal emission of electrons from interface traps at temperatures above room temperature [8]. On the other hand, the on-state resistance measured with V_{GS} = +11 V was affected by increase of JFET resistance with temperature and V_{TH} instability due to charging of interface traps by electrons [9]. The experiment clearly shows that the change of R_{on} was caused by a high density of interface traps in the channel, which gives rise to V_{TH} instability and other temperature-dependence mechanisms are predominantly occurred rather than bipolar degradation.

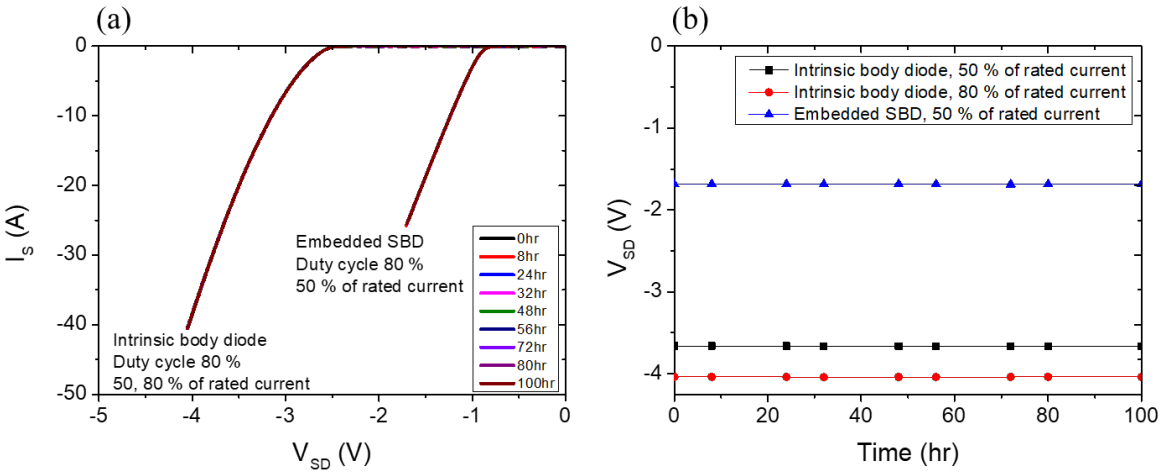

Fig. 3. (a) Diode conduction characteristics after conduction stress with 50 and 80 % of rated current measured at 54 ℃, and (b) V_{SD} measurements after time-dependent bipolar degradation.

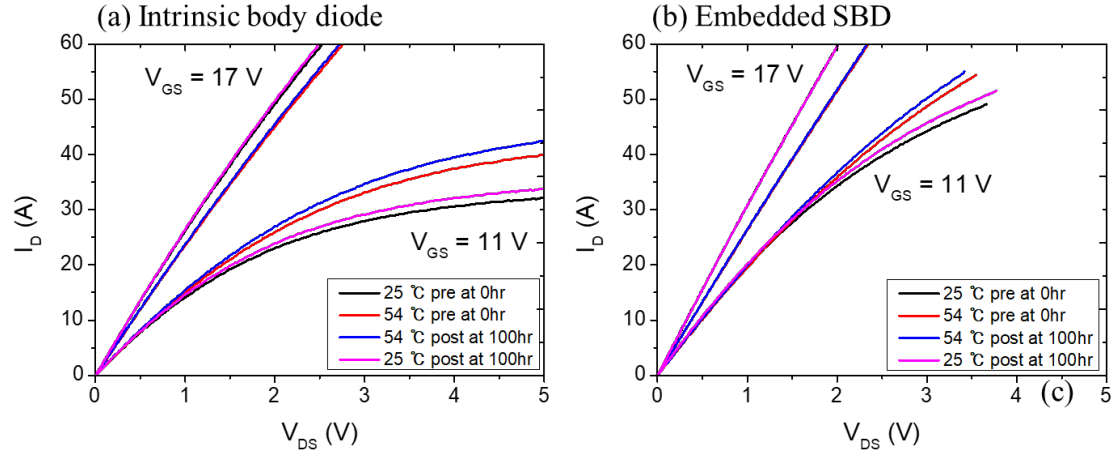

Fig. 4. MOSFET output characteristics measured at 25 and 54 ℃ before and after conduction stress of the (a) intrinsic body diode, and (b) embedded SBD.

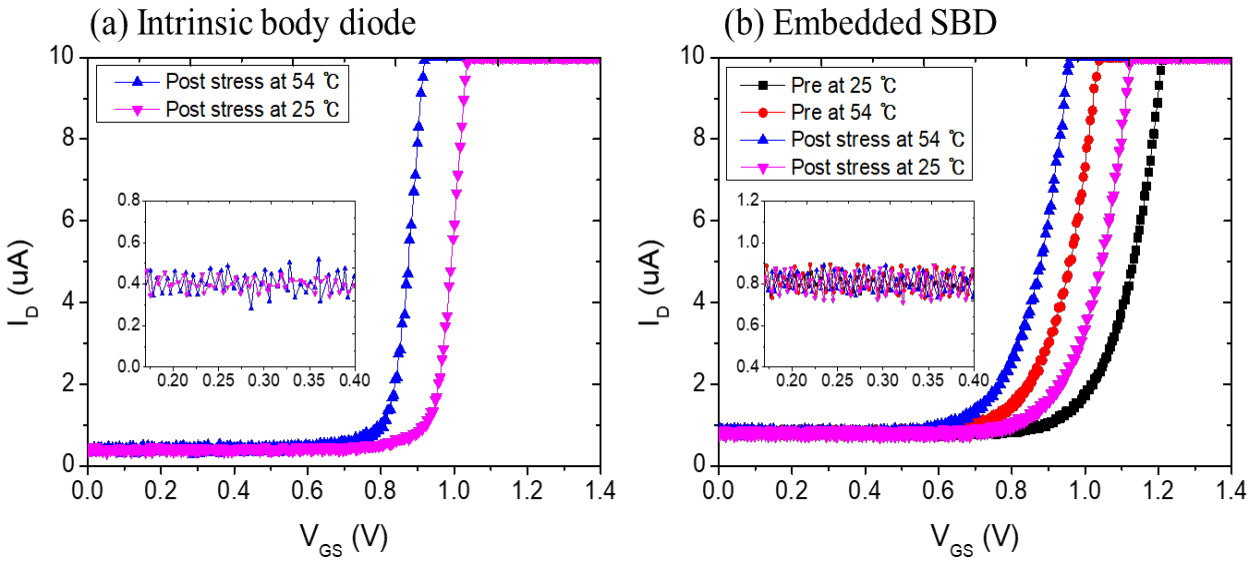

Fig. 5. Results of transfer characteristics were measured before and after conduction stress of the (a) intrinsic body diode and (b) embedded SBD.

In Figure 5, the MOSFET transfer characteristics were measured before and after conduction stress of the body diode and embedded SBD. The threshold voltage shift towards lower values and drain leakage current flowing through the channel even with applied V_{GS} = -10 V is clearly seen. This leads to negative V_{TH} shift caused by electron trapping at the interface traps [9] and decreased stress current density in the intrinsic body diode and embedded SBD.

Summary

The investigation of the bipolar degradation has demonstrated that this effect can be masked by side effects such as the threshold voltage shift and by temperature dependances. More work is required with focus on experiment conditioning to provoke distinct bipolar degradation and separation of the effects related to the subthreshold current flow.

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