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Impact of Turn-Off Gate Voltage and Temperature on Threshold Voltage Instability in Pulsed Gate Voltage Stresses of SiC MOSFETs

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Abstract. Bias temperature instability (BTI) in SiC MOSFETs has come under significant academic and industrial research. Threshold voltage (V_{TH}) shift due to gate voltage stress has been demonstrated in several studies investigating gate oxide reliability in SiC MOSFETs. Results have shown positive V_{TH} shift occurring due to electron trapping (PBTI) and negative V_{TH} shift occurring due to hole trapping (NBTI). In this paper, V_{TH} shift is studied for unipolar and bipolar gate pulses with frequencies ranging from 1Hz to 100 kHz. The turn-OFF voltage for the unipolar V_{GS} pulse is 0V. In the case of the bipolar V_{GS} pulses, two turn-OFF voltages are investigated, namely $V_{GS\text{-}OFF}$ = -3V and $V_{GS\text{-}OFF}$= -5V. V_{TH} shift is measured after 1000 seconds with recovery times in the range of 20 milliseconds and preconditioning is performed before V_{TH} measurement. These measurements have been performed at 25°C and 150°C on a commercially available SiC Planar MOSFET and a SiC Trench MOSFET. The results show that -3 V is enough for de-trapping sufficient electrons while -5V results in increased NBTI which is accelerated by higher temperatures.

Introduction

Power semiconductor devices are required to pass high temperature gate bias (HTGB) stress tests which comprise of 1000 hours of gate voltage bias at a high temperature. The Threshold voltage (V_{TH}) is required to remain strictly within defined limits specified by the datasheet [1]. For silicon MOSFETs and IGBTs, this is routine. Although the latest generation of SiC MOSFETs have passed this reliability tests, measurements still show considerable V_{TH} shift compared to silicon devices. Gate oxides in SiC MOSFETs are reported to have lower breakdown voltages and are less robust under short circuit conditions [2, 3]. This is due to higher fixed oxide and interface trap density resulting from the oxidation of SiC to form the gate oxide [4]. The presence of carbon atoms during thermal oxidation of SiC means dangling bonds at the oxide interface which become interface traps that can hold both positive and negative charges thereby shifting the flat-band (and threshold) voltage [4, 5]. In high frequency applications where the SiC MOSFET experiences large dI_{DS}/dt and dV_{DS}/dt, to prevent short circuits resulting from Miller capacitance coupling, SiC MOSFETs are usually turned-OFF with a negative gate voltage. This means that the gate oxide traps holes and electrons in rapid succession as the device is switched at high frequencies.

Previous studies have shown that threshold voltage shifting due to positive and negative bias temperature instability is a significant challenge in SiC MOSFETs [6, 7]. Another important consideration regarding gate reliability measurements in SiC MOSFETs is the recovery time, which is the time duration between the removal of the V_{GS} stress pulse and the measurement of V_{TH}. The

MOSFET V_{TH} recovers towards its pretest value as the stress pulse is removed since trapped charges are released. In positive HTGB where the V_{TH} shift is positive due to electron trapping, the trapped electrons are released after the V_{GS} is set to zero. Furthermore, the recovery of the V_{TH} can be accelerated by applying a negative V_{GS}. Hence, the measurement of V_{TH} during HTGB tests in SiC MOSFET must follow a defined procedure with a predefined recovery time and preconditioning.

Until recently, mainly unipolar constant gate stresses were investigated as has historically been the case when testing silicon devices on high temperature gate bias. Some studies have shown the impact of pulsed gate voltage stresses on threshold voltage shift in SiC MOSFETs [8]. It has previously been demonstrated that using a turn-off gate voltage of – 5V is capable of mitigating positive V_{TH} shift from PBTI during pulsed stresses of SiC MOSFETs at 100 kHz switching frequency [9]. This paper investigates the comparative effectiveness between turn-off gate voltages of -3 V and -5 V in suppressing PBTI. Pulsed PBTI experiments are performed over a frequency range from 1 Hz to 100 kHz on two commercially available SiC MOSFETs at 25°C and 150°C. Preconditioning is performed prior to the classic measure-stress-measure sequence to ensure a known state of charge prior to measurement [10]. A recovery time of 20 milliseconds is used in the measurements and the duty cycle of the pulses is set at 50%.

Experimental Measurements

The experimental set-up shown in Figure. 1 comprises of Source Measuring unit (SMU) 2602B from Keithley for measuring threshold voltage, a gate driver with adjustable turn-off voltages, a small electric heater for setting the junction temperature and relays for controlling the circuit and switching from stress-mode to measurement mode. The devices under test (DUT) are commercially available 1200V SiC power MOSFETs. A Planar MOSFET and a Trench MOSFET from well-known device manufacturers have been selected.

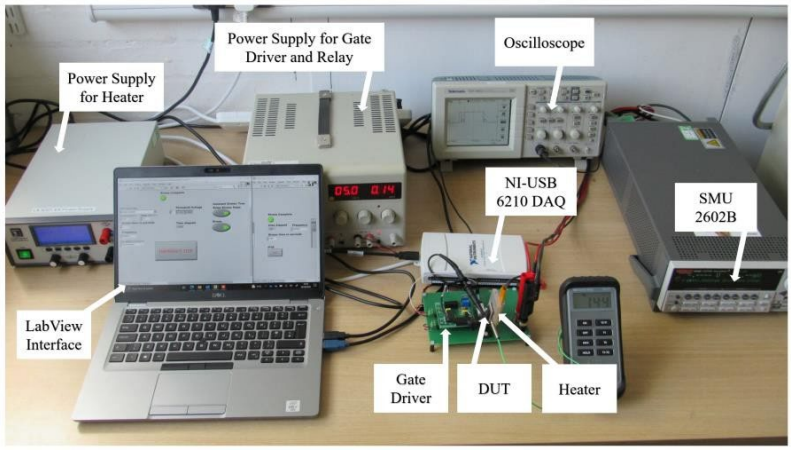

Figure 1(a). Experimental set up for gate stress measurements

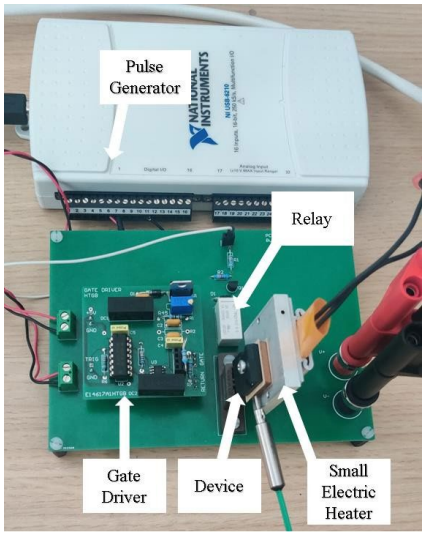

Figure 1(b). Custom designed PCB for pulsed gate stresses application and V_{TH} measurements

During stress mode, the MOSFET drain-source is shorted, and the gate-source is connected to the gate driver as shown in Figure. 2 (a). TTL pulses are generated using a National Instruments board model NI-USB-6210 and are connected to the gate driver board input. The duty ratio of the pulses is 50% and the on-state gate voltage ($V_{GS\text{-}ON}$) is set as the recommended gate voltage for the DUT. The off-state gate voltage ($V_{GS\text{-}OFF}$) is varied (0V, -3V, -5V). In Figure. 2 (b), the measurement mode is shown. Here, the gate and drain terminals are shorted and 1 mA is sourced through the DUT from the SMU which measures the V_{TH} as the V_{DS}. The test sequence is shown in Fig. 2(c). The switching frequency of the gate pulse is varied from 1 Hz to 100 kHz logarithmically.

A preconditioning pulse is recommended, [10] to define a state of charge in the gate oxide before

V_{TH} measurement. Measuring V_{TH} after the V_{GS} stress before preconditioning gives an indication of the peak voltage while the measurement after preconditioning yields the permanent V_{TH} shift. The charges trapped by the SiC MOSFETs have varying time constants with short time constant charges released quickly after stress removal and longer time constant charges contributing to the permanent V_{TH} shift in the device.

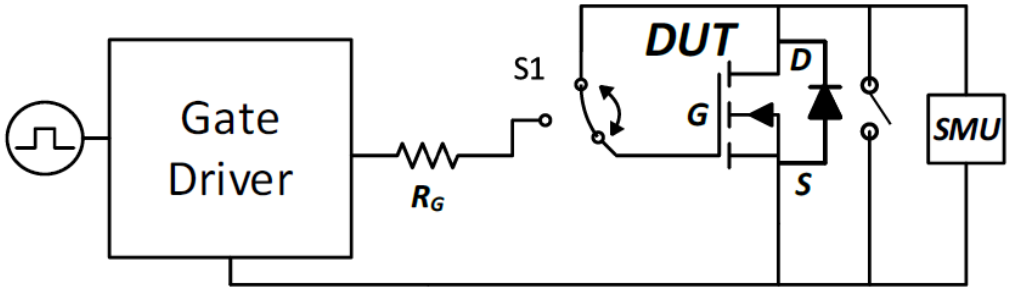

Figure 2 (a) *VTH* Measurement Mode.

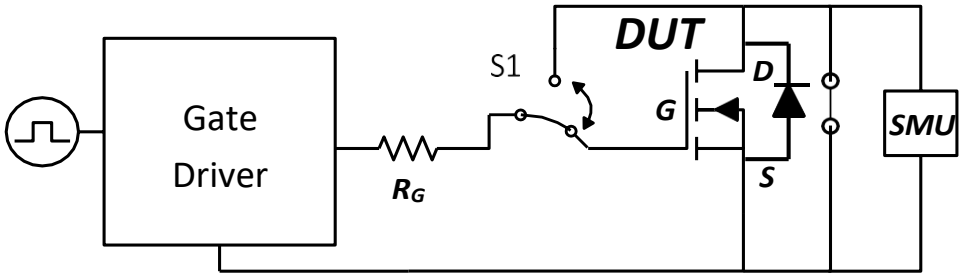

Figure. 2 (b) MOSFET stress mode.

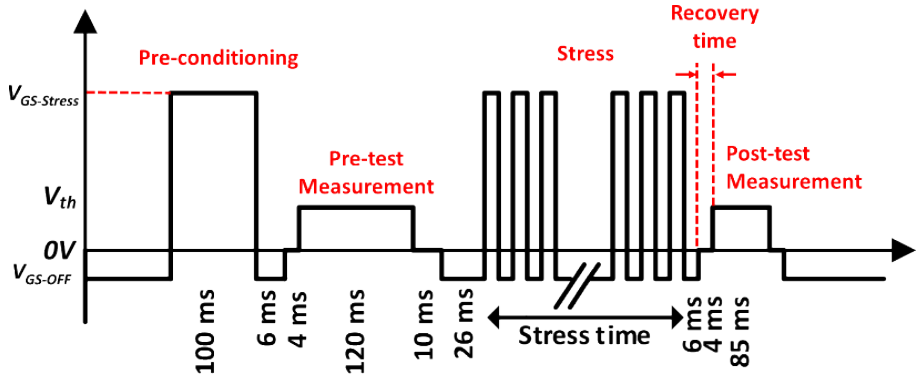

Figure. 2 (c) Test Sequence

Experimental Results

A) Pulsed Stress Test.

Figure 3 shows the results of 1000 seconds of positive HTGB measurements with a V_{GS} pulse frequency of 60 kHz, a duty cycle of 50% and using the pulse sequence defined in Figure 2(c). Figure 3(a) shows the results for the unipolar test ($V_{GS\text{-}OFF}$ = 0V) while Figure 3(b) shows that for the bipolar test ($V_{GS\text{-}OFF}$ = -3 V). Both tests in Figure 3 have been performed with a silicon MOSFET from IXYS with datasheet reference IXFK20N120 for comparison. The results in Figure 3 shows that the V_{TH} shift from the bipolar V_{GS} pulse is smaller compared to that of the unipolar V_{GS} pulse. The difference in V_{TH} shift between the unipolar and bipolar stress pulses is more apparent in the Planar MOSFET (device A) than in the Trench MOSFET (device B). It is clear that the V_{TH} shift in the silicon MOSFET is negligible compared to those in the SiC MOSFET.

Figure 4 shows the impact of the switching frequency on the V_{TH} shift with the unipolar V_{GS} pulse and two bipolar V_{GS} pulses ($V_{GS\text{-}OFF}$ = -5 V and -3 V). The V_{TH} shift is calculated for each frequency step. The result show that the overall V_{TH} shift increases with frequency between 1 Hz and 1 kHz for

all V_{GS} stresses. Beyond 1 kHz, the V_{GS} shift is constant and independent of frequency. When $V_{GS\text{-}OFF}$ = -5 V, the overall V_{TH} shift becomes negative. When $V_{GS\text{-}OFF}$ = -3 V, the V_{TH} shift is close to zero for most of the switching frequencies. This indicates that -3 V is an optimal turn-OFF voltage as far as minimizing V_{TH} shift is concerned.

Figure 5 shows the impact of temperature on the V_{TH} vs Frequency characteristics of the SiC Planar MOSFET (device A) and the SiC Trench MOSFET (device B). The overall negative shift in V_{TH} is increased at 150°C indicating either faster electron release with increasing temperature, more hole trapping with increasing temperature or a combination of both.

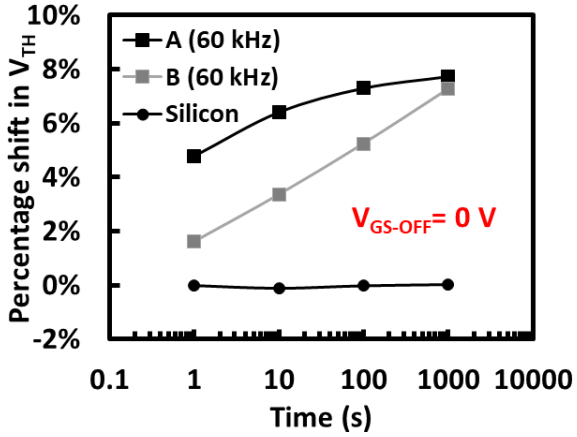

Figure. 3(a) V_{TH} shift vs time for 60 kHz unipolar V_{GS} pulse with duty cycle = 50%

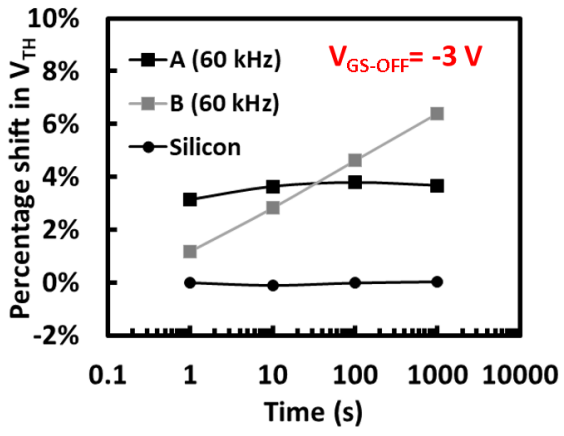

Figure. 3(b) V_{TH} shift vs time for 60 kHz bipolar V_{GS} pulse with duty cycle = 50%

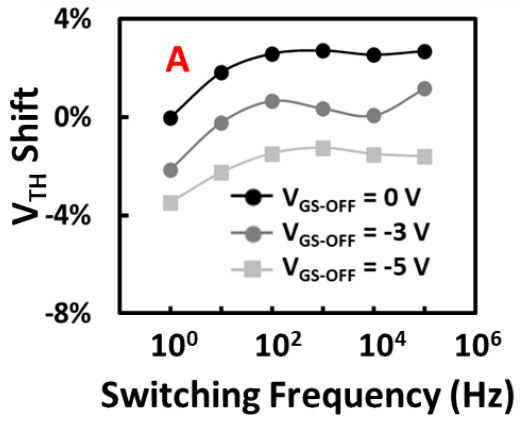

Figure. 4(a) V_{TH} shift vs switching Frequency. $V_{GS\text{-}OFF}$ = -3V and -5V (Device A)

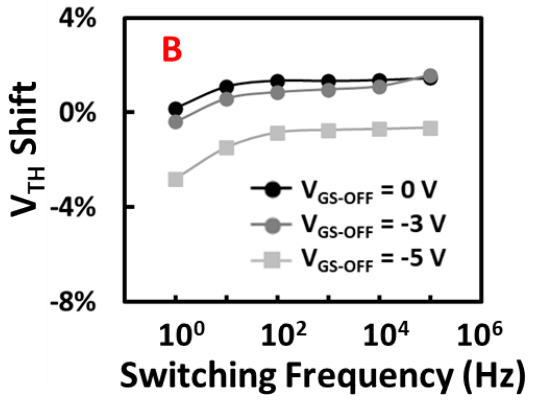

Figure. 4(b) V_{TH} shift vs switching Frequency. $V_{GS\text{-}OFF}$ = -3V and -5V (Device B)

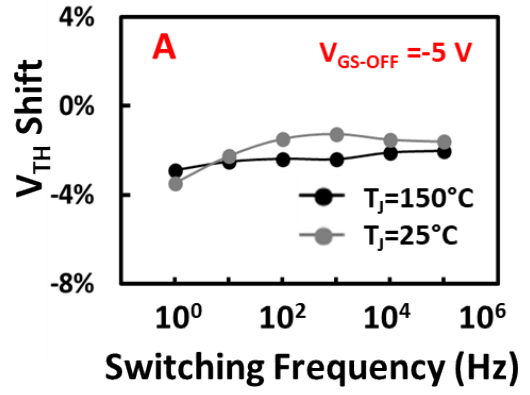

Figure. 5(a) V_{TH} shift vs switching Frequency for pulsed PBTI at 25°C and 150°C (Device A)

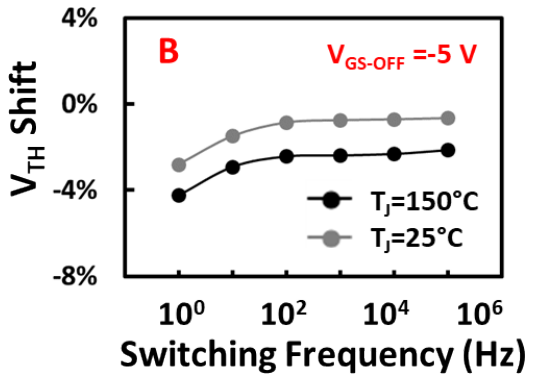

Figure. 5(b) V_{TH} shift vs switching Frequency for pulsed PBTI at 25°C and 150°C (Device B)

B) Accelerated Stress Tests

By applying a constant gate voltage of 30V (significantly more than the rated gate voltages) to the gate of the power MOSFETs, the ΔV_{TH} has been accelerated. 30V was applied to the gate of the SiC MOSFETs for 1000 seconds and the ΔV_{TH} has been measured at different points after the stress removal. The objective here was to understand the V_{TH} recovery of the devices. The initial shift of the V_{TH} is higher compared to the V_{GS} stress at the rated voltage due to the higher electric fields imposed on the gate oxide. These tests have been performed at 25°C and 150°C junction temperatures. Figure 6(a) shows the results of the recovery measurements at 25°C while Figure 6(b) shows the similar plot for measurements done at 150°C. Measurements were also performed on a silicon MOSFET for benchmarking. The shifts reported in the SiC Trench MOSFET (device B) are higher than those in SiC Planar MOSFET (device A). It is also clear that the time constant of the trapped charge in device B are larger since it takes a longer time to recover. It should be noted that these measurements were performed without preconditioning, hence, what is under observation is V_{TH} shift due to charges with short time constants.

Figure 7(a) shows the results of an oxide breakdown test. Here, the V_{GS} is swept upwards until the leakage current through the gate exceeds 1µA. Figure 7(b) shows the leakage currents through the gate of the MOSFETs with V_{GS}=30 V applied for 1000 seconds at 25°C and 150°C. It is clear from Figures 7(a) and 7(b) that the gate oxide of the SiC Planar MOSFET is generally more robust with demonstrated a higher breakdown voltage and less leakage current at high gate voltages.

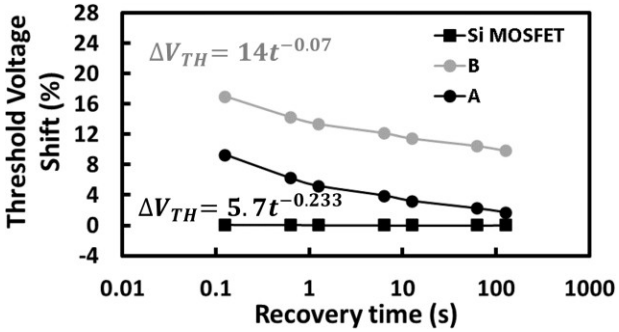

Figure. 6(a). V_{TH} recovery plots showing V_{TH} shift vs time for both devices after 1000 seconds of 30 V stress at 25°C

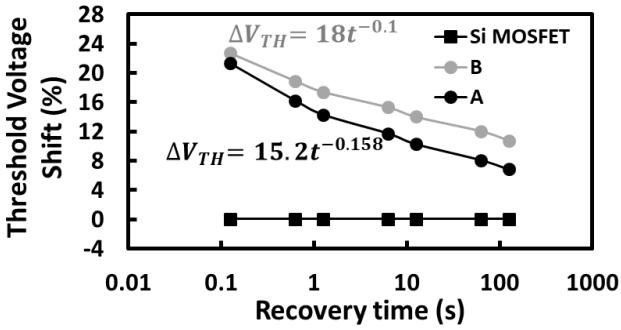

Figure. 6(b). V_{TH} recovery plots showing V_{TH} shift vs time for both devices after 1000 seconds of 30 V stress at 150°C

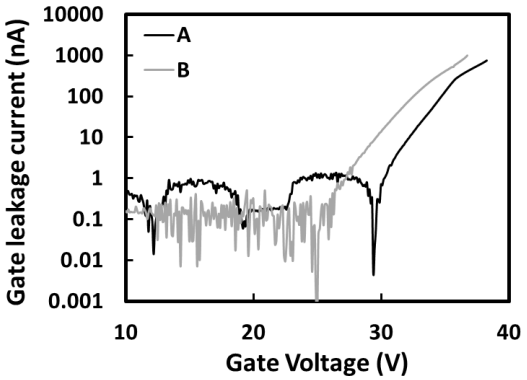

Figure. 7(a) Oxide breakdown test for both devices

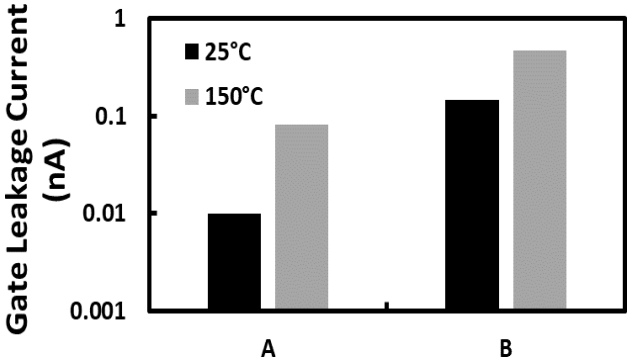

Figure. 7(b) Leakage current for both devices at V_{GS}=30 V

Conclusions

Bias temperature instability measurements have been performed on SiC Planar and Trench MOSFETs. Pulsed V_{GS} measurements are performed over a frequency range between 1 Hz and 100 kHz. For the pulsed stresses, different turn-OFF V_{GS} voltages (0 V, -3 V and -5 V) are tested so as to investigate the impact on overall V_{TH} shift. The results show an increase in the measured V_{TH}

shift with frequency up to 1 kHz with V_{TH} shift becoming independent of frequency after 1 kHz. This was the case for both the Planar and Trench MOSFETs. When $V_{GS\text{-}OFF}$ = -5 V is used in the pulsed stress test, there is an NBTI problem with a net negative shift in V_{TH}. This is because hole trapping/electron release occurs faster at $V_{GS\text{-}OFF}$= -5 V and dominates the overall V_{TH} shift. When $V_{GS\text{-}OFF}$=-3 V, the net V_{TH} shift is close to zero. For the pulsed V_{GS} stresses with $V_{GS\text{-}OFF}$ = -5 V, as the junction temperature is increased to 150°C, the magnitude of the V_{TH} shifts increases thereby causing more NBTI. When accelerated stress tests are performed with V_{GS} = 30 V, the V_{TH} shift increases with the Trench MOSFET more than the Planar MOSFET and the recovery occurs with longer time constants. Similar measurements were performed with silicon MOSFETs which showed negligible shifting thereby indicating that BTI remains present in SiC MOSFETs to a much larger extent compared to silicon devices.

Acknowledgements

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References

[1] ECPE Guideline AQG 324 “Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles”. Release no.: 03.1/2021, May 2021.

[2] J. O. Gonzalez, R. Wu, S. Jahdi and O. Alatise, "Performance and Reliability Review of 650 V and 900 V Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs," in IEEE Transactions on Industrial Electronics, vol. 67, no. 9, pp. 7375-7385, Sept. 2020.

[3] E. Bashar et al., "Comparison of Short Circuit Failure Modes in SiC Planar MOSFETs, SiC Trench MOSFETs and SiC Cascode JFETs," 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2021, pp. 384-388.

[4] T. Aichinger, G. Rescher, and G. Pobegen, “Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs,” Microelectron.Rel., vol. 80, pp. 68–78, 2018.

[5] V. V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, “Intrinsic SiC/SiO2 interface states,” Phys.Status Solidi (a), vol. 162, no. 1, pp. 321–337, 1997.

[6] K. Puschkarsky T. Grasser T. Aichinger W. Gustin and H. Reisinger "Review on SiC MOSFETs high-voltage device reliability focusing on threshold voltage instability" IEEE Trans. Electron. Devices vol. 66 no. 11 pp. 4604-4616 Nov. 2019.

[7] J. Orti Gonzalez and O. Alatise, "Impact of BTI-Induced Threshold Voltage Shifts in Shoot-Through Currents From Crosstalk in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 36, no. 3, pp. 3279-3291, March 2021, doi: 10.1109/TPEL.2020.3012298.

[8] A. K. Ghosh, O. O. Awadelkarim and J. Hao, "Studies of AC BTI Stress in 4H SiC MOSFETs," 2021 IEEE International Integrated Reliability Workshop (IIRW), 2021, pp. 1-4.

[9] E. Murakami, T. Furuichi, T. Takeshita, and K. Oda, "Suppression of PBTI of SiC-MOSFETs under 100 kHz Gate-Switching Operation by Using a Gate Off-Voltage of -5 V," Materials Science Forum, vol. 924, pp. 711-714, 2018,

[10] G. Rescher, G. Pobegen, T. Aichinger, and T. Grasser, “Preconditioned BTI on 4H-SiC: Proposal for a nearly delay time-independent measurement technique,” IEEE Trans. Electron Devices, vol. 65, no. 4, pp. 1419–1426, Apr. 2018