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Small-Signal Impedance and Split C-V Characterization of High-κ SiC Power MOSFETs

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Abstract In this work, the improvement of SiC power MOSFET performance achieved using high-κ gate-dielectrics instead of the standard SiO_2 is investigated by means of advanced gate-impedance characterization. The benefit of using high-κ gate-dielectrics with high dielectric constant is demonstrated by comparing SiC MOSFETs with pure high-κ, a stack of SiO_2/high-κ, as well as pure SiO_2. Namely, the fabricated high-κ SiC MOSFETs show a superior performance to SiC MOSFETs with SiO_2/SiC interface with respect to channel resistance and interface quality. The proposed characterization approach is non-destructive and applicable to packaged power devices.

Introduction

In comparison to Si device technology, threshold voltage instability due to traps at the SiO_2-SiC interface has turned out to be a characteristic feature of SiC power MOSFETs [1]. It has been recently shown that high-κ gate dielectrics replacing native SiO_2 represent a promising solution for improving the performance of vertical SiC power MOSFETs with respect to threshold voltage hysteresis and threshold voltage shift under gate stress [2]. An improved interface quality furthermore enables achieving lower specific on-state resistance [3]. In this paper split C-V and small-signal impedance characterization of pure high-κ, SiO_2/high-κ and pure SiO_2 SiC power MOSFETs are compared, in order to analyze the impact of gate-dielectrics on the device performance.

Analyzed Gate-Dielectrics SiC Power MOSFET Samples

Planar-gate 1.2 kV SiC power MOSFET samples with high-κ- (K1, K1b, K2, K2b) and high-κ/SiO_2 dielectrics (S1, S2) from Hitachi Energy, and three Wolfspeed 1.2 kV SiC power MOSFETs with SiO_2 dielectric both from Gen 2 and the improved Gen 3 technology (M1, M2, M2b) are selected for the analysis, see Table 1. The K1, K1b and S1 samples have the same chip and cell layouts, $i.e.$ same active area, termination region, pitch-size and gate layout, they differ only for the gate-dielectric stack. The same applies for the K2, K2b and S2 samples. All samples have comparable on-state resistances however different pitch sizes. A direct comparison of the fabricated high-κ to SiO_2 reference samples and the selected commercial SiC power MOSFETs with respect to voltage-/frequency-dependent gate impedance is shown in the following.

Table 1: Planar gate 1.2 kV SiC Power MOSFET samples used for analysis.

Name	Type	$R_{ds,ON}$ $[m\Omega]$ $(@V_{gs} = 15V)$	pitch size $[\mu m]$
K1	high-κ (Hitachi Energy)	21	10.5
K1b	high-κ (Hitachi Energy)	25	10.5
K2	high-κ (Hitachi Energy)	24	14.5
K2b	high-κ (Hitachi Energy)	26	14.5
S1	high-κ/SiO_2 (Hitachi Energy)	33	10.5
S2	high-κ/SiO_2 (Hitachi Energy)	38	14.5
M1	SiO_2 (Wolfspeed, 2nd Gen)	33	9.1
M2	SiO_2 (Wolfspeed, 3rd Gen)	20	6.1
M2b	SiO_2 (Wolfspeed, 3rd Gen)	27	6.1

Small-Signal Impedance Characterization

Small-signal impedance measurements are performed to extract datasheet device characteristics such as internal gate resistance and capacitance-voltage behavior. Split C-V characterization on the other hand is typically used to measure the reverse power MOSFET capacitance, C_{rss}. In this paper, the gate impedance is measured to evaluate the internal gate resistance as function of frequency and gate bias, while split C-V measurements at different frequencies are performed to evaluate the gate-drain C_{dg} and gate-source C_{sg} capacitances, separately. Furthermore, the channel R_{ch} and drift resistance R_{drift} (= R_{jfet} + R_{epi} + R_{sub}) components of the total on-state resistance are extracted based on the split C_{dg} and C_{sg} measurements as described in [4]. All measurements are performed using a Keysight E4990A impedance analyzer for the SiC power MOSFET samples specified in Table 1.

Split C-V gate characterization: Results

From the split C-V measurements, C_{dg} and C_{sg} components can be either extracted using a series (C_s-R_s) or parallel (C_p||G_p) equivalent model, where the peaks observed in the series $C_{sg,s}$ and $C_{dg,s}$ can be correlated to the transconductance g_m extracted from the transfer-characteristic I_d-V_{gs} as described in [4]. The C_{sg} and C_{dg} of K1, S1, M1 and M2 measured at $f = 30$ kHz are shown in Fig. 1. Comparing $C_{dg,s}$ and $C_{sg,s}$ of K1, S1, M1, and M2 SiC power MOSFETs, higher peaks within $C_{sg,s}$ and $C_{dg,s}$ of K1 point out to higher transconductance for high-κ- than for high-κ/SiO_2 and pure SiO_2-interface. Furthermore, an improvement of SiC power MOSFET technology from Wolfspeed from Gen2 to Gen3 with respect to g_m can be clearly observed by comparing M1 and M2.

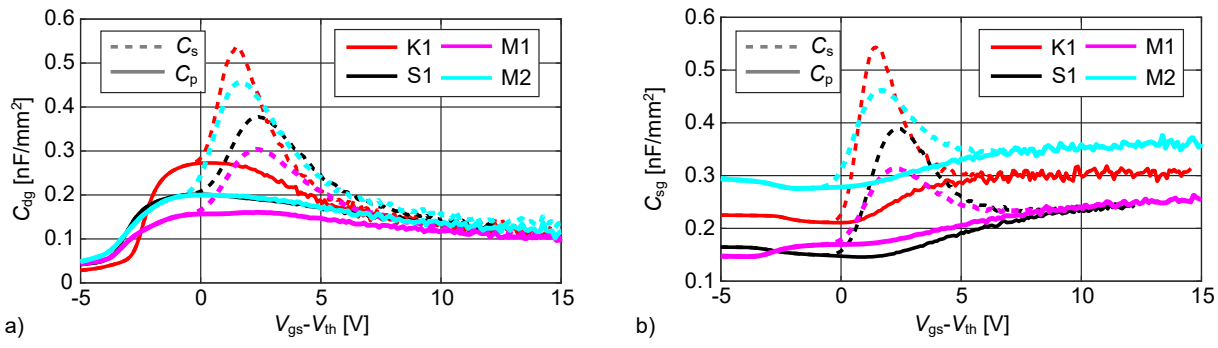

Fig. 1: Measured a) C_{dg} and b)C_{sg} of SiC power MOSFET samples K1, S1, M1 and M2.The results are normalized by device active area and shifted by treshold voltage V_{th}.

Extraction of on-state resistance components: Results

Since the parallel capacitances $C_{sg,p}$ and $C_{dg,p}$ carry only the information about MOSFET capacitances and not about g_m, $C_{sg,p}$ and $C_{dg,p}$ are used to evaluate the R_{ch}/R_{drift} ratio as shown in Fig. 2a). The total drain-to-source on-state resistance $R_{ds,ON}$ is evaluated from I_d-V_{gs} measurements at $V_{ds} = 50\,\text{mV}$, thus allowing the evaluation of individual components R_{drift} and R_{ch} as function of V_{gs}. The R_{drift} and R_{ch} results normalized by device active area are shown in Fig. 2b). First, a dependence of R_{ch} and R_{drift} on the pitch size can be extracted from Fig. 2b) by comparing K1 and K2 SiC power MOSFETs. Second, the proposed characterization method clearly points to reduced R_{ch} and R_{drift} of SiC power MOSFETs K1 and K2 with pure high-κ gate-interface than in the case of S1 and S2 with high-κ/SiO_2-stack. Another interesting observation is that R_{ch} of K1 and M2 are comparable despite a smaller pitch of M2 that can be explained by (1) increased C_{ox}, *i.e.* higher transconductance of the MOSFET g_m, and (2) an improved channel mobility due to higher interface quality.

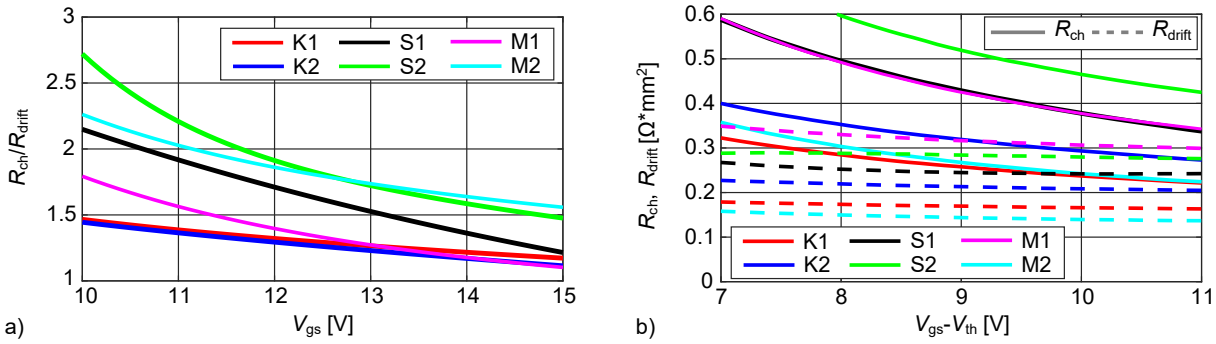

Fig. 2: Extracted a) R_{ch}/R_{drift} ratio and b) R_{drift} and R_{ch} components normalized by device active area and shifted by V_{th} of SiC power MOSFET samples K1, K2, S1, S2, M1 and M2.

Internal Gate Resistance R_{gg} Characterization

Internal gate resistance R_{gg} is extracted as the real part of the measured gate impedance Z_{gg}. The measured R_{gg} of K1 at the gate-source voltage $V_{gs} = 0\,\text{V}$ and $15\,\text{V}$ is presented in Fig. 3a). Typically, in datasheets only R_{gg} at $f = 1\,\text{MHz}$ and $V_{gs} = 0\,\text{V}$ is provided. However, R_{gg} is V_{gs}- and f-dependent and three regions as highlighted in Fig. 3a) can be distinguished: 1) very high R_{gg} at low frequency decreasing with f, 2) R_{gg} approximately constant in the mid-frequency range below few MHz, and 3) the high-frequency range above $10\,\text{MHz}$ with R_{gg} decreasing. Region 1 can be related to dielectric-SiC interface traps; Region 2 to the resistance of the polysilicon gate and metal-gate runner, and Region 3 represents the distributed behavior of the polysilicon gate layout that becomes dominant at fast switching transients [5]. The equivalent model shown in Fig. 3b) can be used to describe this behavior, where C_{gg} represents the input gate-capacitance, $R_{g,int}$ stands for the resistance of the polysilicon gate and G_p models the dielectric "leakage". With smaller G_p and higher C_{gg}, Region 2 of $R_{gg}(f)$ is extended in the lower frequency range, while higher G_p and smaller C_{gg} shorten Region 2. Since G_p can be high for SiC power MOSFETs because of the high defect density at the SiC-dielectric interface, R_{gg} at 1 MHz can often include the effect of traps and hence, $R_{gg,1MHz}$ can be misleading for evaluating the actual internal gate resistance. The measured $R_{gg}(f)$ at $V_{gs} = 0\,\text{V}$ of SiC power MOSFET with high-κ and high-κ/SiO_2-stack K1, K1b, K2, K2b, S1 and S2 are shown in Fig. 4a), while $R_{gg}(f)$ of commercial SiC power MOSFETs M1, M2, and M2b are presented in Fig. 4b). In the frequency region between $\approx 20\,\text{MHz}$-$100\,\text{MHz}$, R_{gg} of K1, K1b and S1 SiC power MOSFETs overlap, c.f. Fig. 4a), which corresponds to Region 2 marked in Fig. 3. Namely, as K1, K1b and S1 are only different with respect to dielectric-semiconductor interface, the measurements confirm that R_{gg} in Region 2 is determined only by the polysilicon and metal resistance of the gate layout. On the other hand, it can be seen that the quality of the dielectric-semiconductor interface affects Region 1 of R_{gg}, *i.e.* a

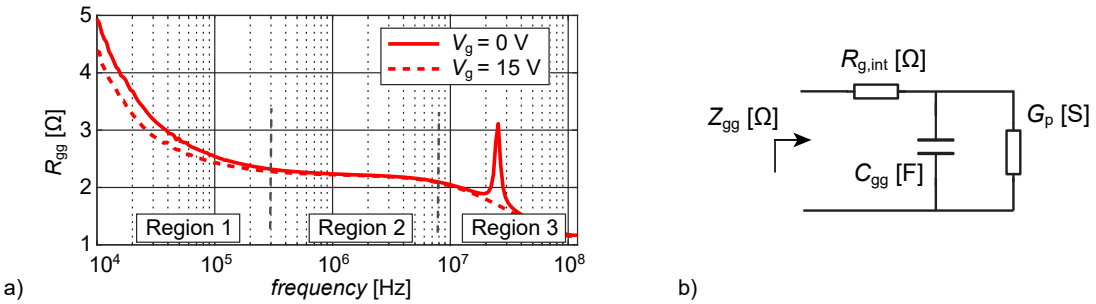

Fig. 3: Frequency dependent internal gate impedance $Z_{gg}(f)$: a) real part of Z_{gg}, $R_{gg}(f)$ for K1 at $V_{gs} = 0$ V and 15 V, b) an equivalent lumped model of Z_{gg}.

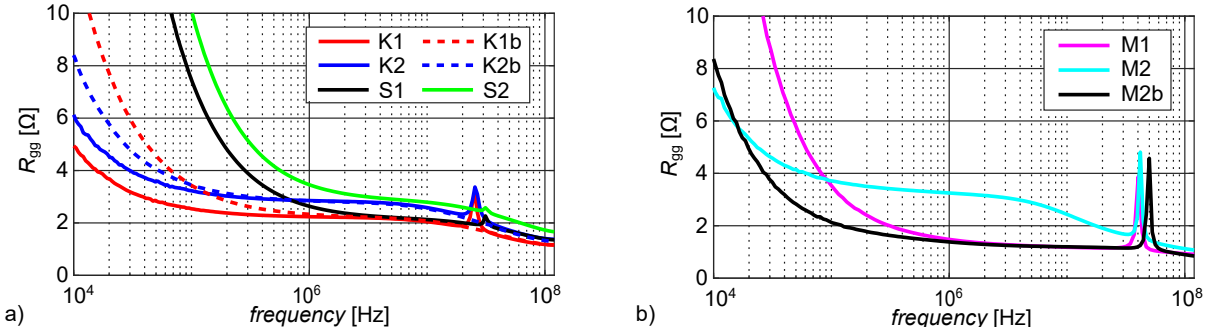

Fig. 4: Measured $R_{gg}(f)$ at $V_{gs} = 0$ V: a) K1, K1b, K2, K2b, S1 and S2, b) M1, M2, and M2b.

higher interface quality leads to a smaller G_p in the model shown in Fig.3b), however this effect can not be fully distinguished from the C_{gg} variation between samples due to different dielectrics. K1 with an improved high-κ dielectric in comparison to K1b, obtained with a better deposition approach, has the smaller G_p than both K1b and S1, which can be related to reduced dielectric and interface-traps. Similarly, K2 has the smaller G_p than K2b and S2 SiC power MOSFETs. Furthermore, it can be seen that pitch size also affects the equivalent lumped R_{gg} in Region 2. The measurements in Fig. 4b) suggest that $G_{p,M2}$ and $G_{p,M2b}$ are smaller than $G_{p,M1}$, i.e. Region 2 is shifted towards lower frequencies, however gate design parameters affecting C_{gg} also have an influence on Region 1.The clear distinction between these two concurring effects impacting Region 1 is under further investigation.

R_{gg} as function of gate-source Voltage V_{gs}

In the next step, R_{gg} was characterized as function of gate-source voltage V_{gs}. $R_{gg,M1}(V_{gs} - V_{th})$ normalized by the device active area (mm^2) is shown in Fig. 5a) for $f = 30$ kHz, 100 kHz, 1 MHz and 10 MHz. Sweeping V_{gs} is expected to reveal the impact of traps at different energy levels in the bandgap on the R_{gg}. At high frequencies, $i.e.$ 10 MHz, the traps are ineffective and the R_{gg} is independent from V_{gs} and only determined by the gate-layout as discussed for Fig. 3a). $R_{gg}(V_{gs} - V_{th})$ normalized by the device active area (mm^2) of K1, K2, S1, S2, M1, and M2 are presented in Fig. 5b) and Fig. 5c), without and with scaling with the pitch size, respectively. The lower peaks amplitude of the high-κ samples and M2 further support the conclusion of higher interface quality of these samples and/or higher C_{gg}. Interestingly, M1 shows a peak in the positive $V_{gs} - V_{th}$ range suggesting the presence of different interface traps closer to the conduction band, which have been removed in the latest Wolfspeed device generation. The scaling by the pitch size is necessary to make more meaningful comparison of different devices, namely in Fig. 5c) the peak amplitude for the same technology are equalized independently on the cell pitch: K1-K2 and S1-S2. The V_{th} hysteresis of K1, S1, M1 and M2 is shown in Fig. 5d). M2 presents a significant V_{th} hysteresis despite the smaller $R_{gg}(V_{gs})$ peak shown in Fig. 5c) and the small C_{ox} of SiO_2, that can lead to the conclusion that the defects affecting $R_{gg}(V_{gs})$ differ from the

defects impacting the V_{th}-hysteresis [6]. It should be noted that pure high-κ dielectric shows negligible hysteresis in comparison to SiO_2/high-κ and pure SiO_2 samples.

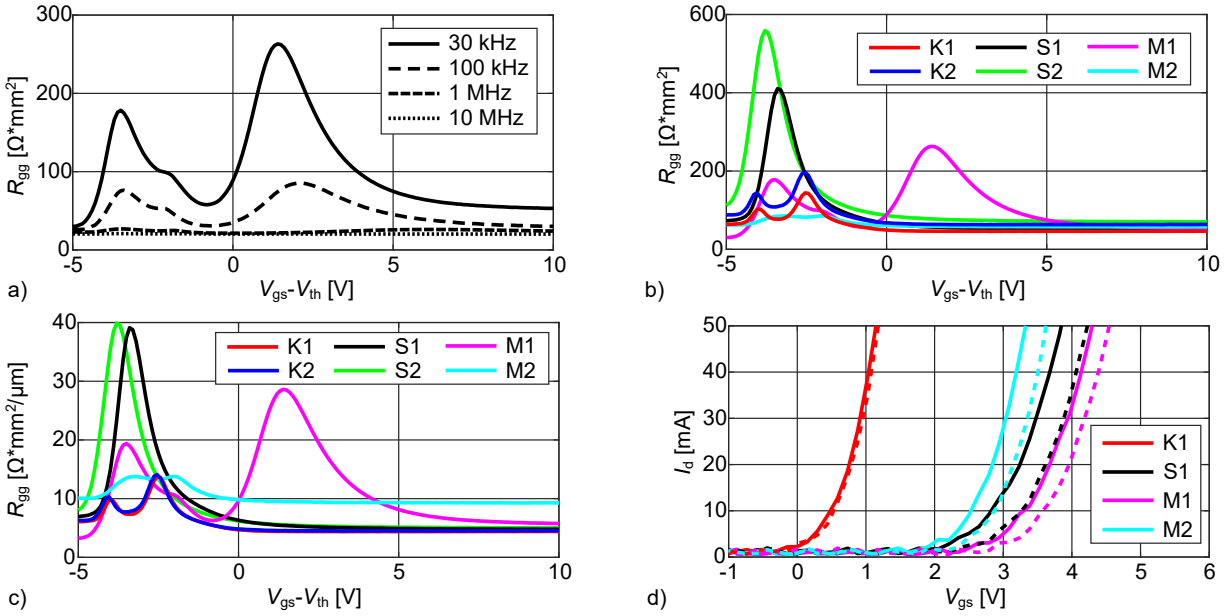

Fig. 5: Measured $R_{gg}(V_{gs} - V_{th})$ normalized by the device active area (mm^2) of a) M1 at different frequencies, b) K1, K2, S1, S2, M1, and M2 at $f = 30\,kHz$, c) K1, K2, S1, S2, M1, and M2 at $f = 30\,kHz$ scaled with pitch size; d) the measured I_d-V_{gs} hysteresis ($@V_{ds} = 50mV$, $V_{gs} = [-5V, 15V]$) of K1, S1, M1 and M2, upward (solid) and downward (dashed) sweep.

Summary

This work reveals the benefit of high-κ gate dielectrics for SiC power MOSFETs and also demonstrates that the standard small-signal impedance measurements can be extended for more precise information on device performance and application-relevant characteristics. The presented gate impedance characterization can be adopted as non-destructive investigation approach to analyze the device quality with special focus on the SiC/gate-dielectric interface for packaged semiconductor devices.

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