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Lifetime Projection of Bipolar Operation of SiC DMOSFET

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Abstract. We show the superior threshold voltage V_{th} and on resistance R_{on} stability of a SiC DMOS technology at bipolar gate-drive operation. Therefore, the defect parameters of a two-state non-radiative multi-phonon model to capture the charge trapping kinetics of oxide and interface defects is calibrated within our simulation framework Comphy by data extracted from measure-stress-measure (MSM) sequences. An extrapolation of the device degradation at operating conditions renders bias temperature instabilities (BTI) a minor threat to on-state loss increase.

Introduction

A widely-known characteristic of planar SiC DMOSFET power switches is their bipolar gate driving operation with a small negative off-state gate bias V_{G} [1]. By employing physical modeling, we show that it reduces the long-term shift of both the threshold voltage ΔV_{th} and the on-state resistance ΔR_{on}.

These parameter drifts, commonly described under the term bias temperature instabilities (BTI), originate mainly from perturbations of the channel electrostatics due to accumulation of charge trapped at defects near the channel/oxide interface. A detailed understanding of the charge trapping kinetics and its temperature and V_{G} dependence is vital for predicting the impact of BTI, i.e. device stability, at time-scales and operating conditions not easily accessible by experiments. Therefore, we employ a two-state non-radiative multi-phonon (NMP) model [2] as implemented in our simulation environment Comphy [3]. This framework relies on physical material and defect parameters and hence captures the charge trapping dynamics in considerable detail, while also allowing to extrapolate the V_{th} degradation of SiC MOSFETs to end-of-lifetime for arbitrary operating conditions [4, 5]. Here, we investigate the charge trapping dynamics leading to the superior stability at bipolar V_{G} operation which results in minor static on-state loss enhancement, even after as long as 10 years.

Simulation

Within our model, the two defect charge states are treated as classical one-dimensional harmonic oscillators as depicted in Figure 1. The capture $\tau_{\text{c}}\left(V_{\text{G}}, T\right)$ and emission $\tau_{\text{e}}\left(V_{\text{G}}, T\right)$ time constants are then determined by activation energy barriers given by the intersection point of the potential energy curves (PECs). A large data set measured on a commercially available DMOSFET [6] consisting of long-term DC and short-term AC MSM sequences is used to extract defect parameters by employing an efficient, effective single defect decomposition (ESiD) algorithm [7]. Together with a regularization scheme it yields defect parameters (E_{T}, E_{R}), c.f. Figure 1, and densities (N_{T}) that are within physical bounds as defined by ab-initio computations for likely defect candidates. Details about the used material parameters and calibration of device electrostatics are provided in [5].

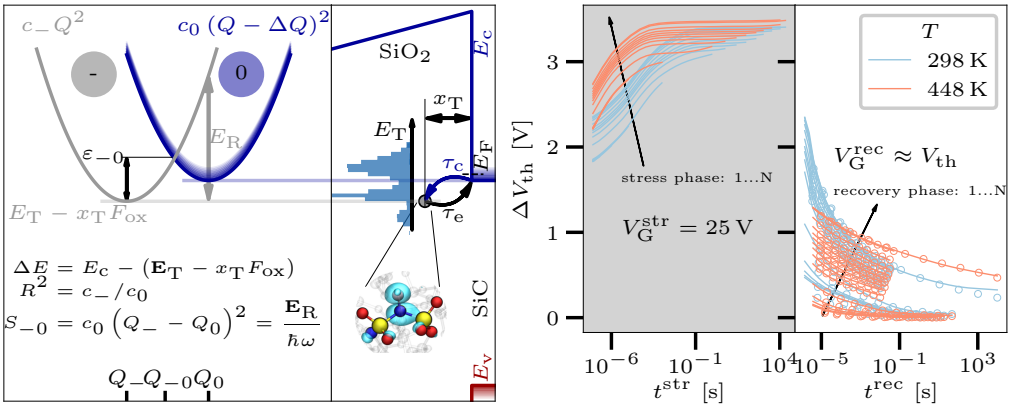

Fig. 1: PECs of a defect for its "0" and "-" state are shown together with the extracted E_T distribution. The energy barriers $\varepsilon_{0-/-0}$ determine $\tau_{c/e}$ **(left)**. MSM data **(circles)** is interpolated by the Comphy simulation **(lines)** using the ESiD method for optimized defect parameter extraction (**right**).

Figure 1 shows the resulting long-term DC ΔV_{th} data for standard operating conditions and accelerated V_G and T stress conditions. Defect properties have been extracted for defect bands accounting for interface/near-interface traps (NITs) and border traps [5]. The former exhibit fast and symmetrical τ_c and τ_e, that are responsible for the majority of fast degrading and recovering ΔV_{th}. The (τ_e, τ_c) distributions for unipolar operation are presented in a capture emission time (CET) map [8] in Figure 2, showing a strong asymmetry of τ_c and τ_e, which leads to hysteresis in the transfer characteristics $(I_D(V_G))$ [9]. By applying a negative off-state bias V_G^L, the τ_c and τ_e distribution is shifted towards faster τ_e, as can be seen in Figure 2.

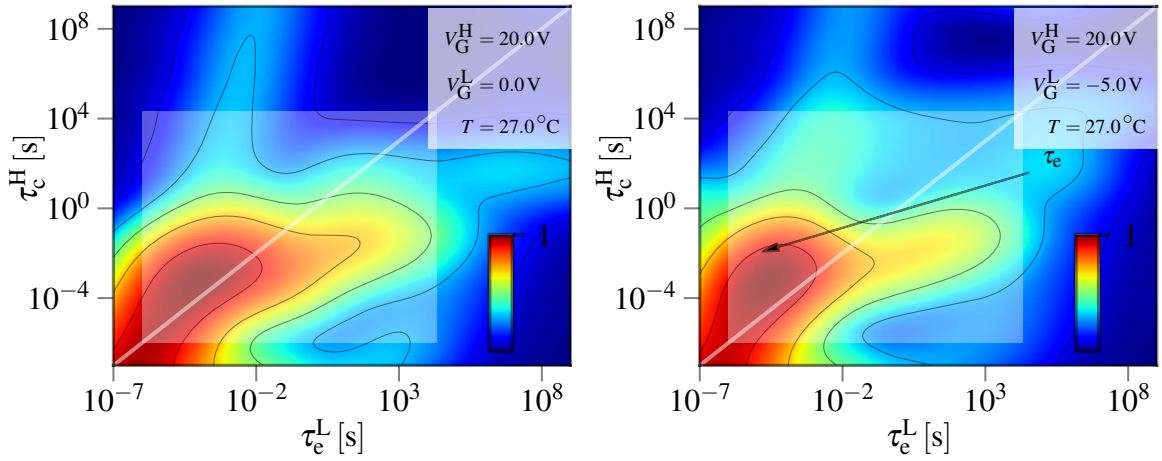

Fig. 2: A CET map at unipolar gate bias operation shows a wide distribution of τ_c (V_G^H) and τ_e (V_G^L) **(left)**. The experimental time window is highlighted **(white)**. The CET map with bipolar V_G shows a shift towards faster τ_e of the electron traps which is the responsible mechanism for the reduced overall degradation (**right**).

Results

In Figure 3 the fraction of defects with τ_c within the experimental window at the applied stress conditions is shown to be larger than the fraction of defects that can be charged after up to 10 years at operating (V_G, T), which justifies the extrapolation up to this period. The computed parameter extrapolation employing an analytical expression for defect occupation for AC gate signals [3] shows the improved stability for bipolar V_G compared to unipolar AC operation. The ΔR_{on} shown in Figure 4 as a function of the overdrive voltage $V_{ov} = V_G - V_{th,0}$ has been derived from an initially measured $I_D(V_G)$

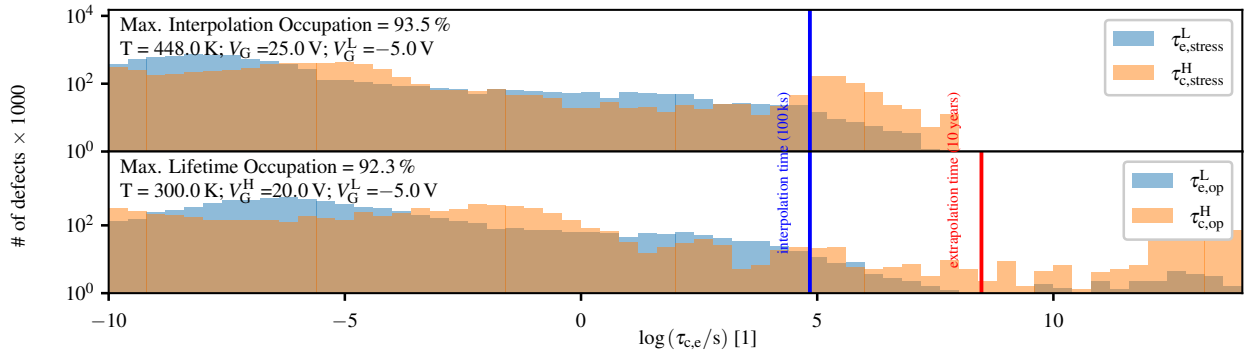

Fig. 3: A histogramm of $\tau_c\,(V_G^H)$ and $\tau_e\,(V_G^L)$ at stress conditions (**top**) shows a larger occupation of defects after the interpolation time, compared to a 10 year extrapolation at operation (V_G, T) (**bottom**) (compare τ_c). Therefore, the acceleration due to stress (increased (V_G, T)) justifies the extrapolation at operation conditions.

curve with a minor dependence on the sweep time, start and end bias, and method of the measurement, e.g. pulsed or continuous, as discussed in [10]. However, for ΔR_{on}, this difference is negligible

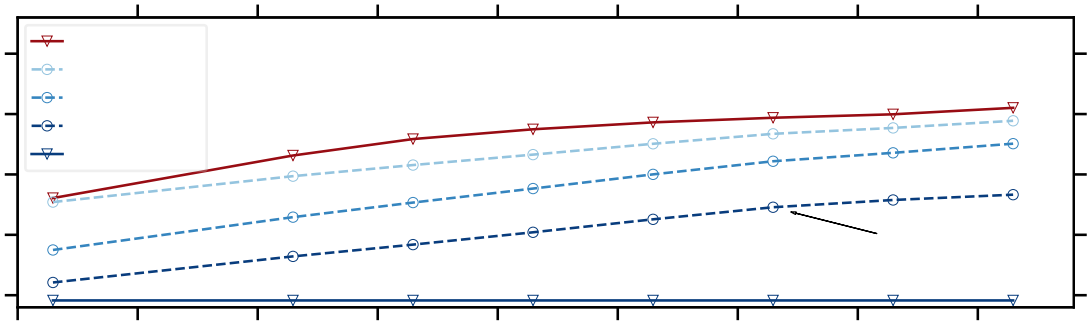

Fig. 4: ΔV_{th} and ΔR_{on} show about 30 % reduced static on-state losses after 10 years of bipolar AC operation, compared to the unipolar AC mode at a duty cycle of $d = 0.5$. The readout gate bias V_G^{read} and time-delay t^{read} after stress to calculate V_{th} and R_{on} are selected to comply with fast experimental drain current extraction.

at the recommended V_G (given in [6]). Note that, even after 10 years, the ΔR_{on} leads to less than 30 % on-state loss increase, at $\Delta V_{th} > 1$ V. Finally, the duty cycle dependence of ΔV_{th} given in Figure 5 shows good stability over the whole range, except for the DC operation points, exhibiting only minor differences for modified conversion gate drive voltage pulse widths compared to Figure 4.

Summary

In summary, our calibrated simulations predict an on-state loss reduction of about 30 % at bipolar V_G operation compared to using unipolar V_G gate-drive signals. These results render BTI induced degradation under the recommended operation conditions a minor power conversion efficiency threat.

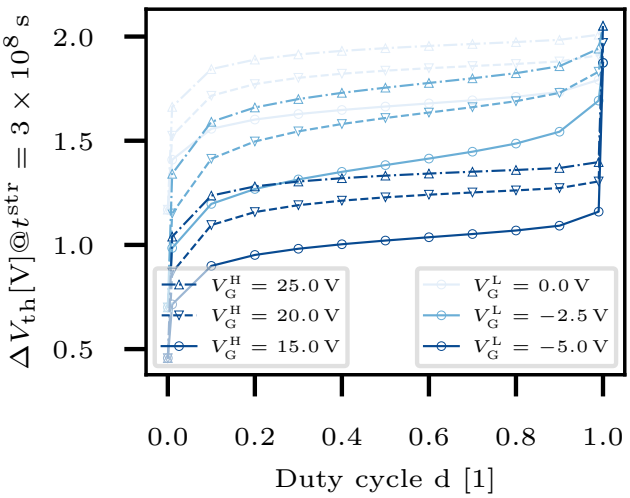

Fig. 5: Duty cycle dependence of ΔV_{th} is shown for the same readout parameters as in Figure 4, with stable ΔV_{th} over d, and lowest degradation for $V_{\mathrm{G}}^{\mathrm{L}} = -5$ V.

Acknowledgment

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